



THE COMPUTER ENGINEERING RESEARCH CENTER

THE VLSI SEMINAR SERIES

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Improving Place-and-Route Results by Optimizing Steiner-tree Length in Placement

Abstract

Despite many years of research in Place-and-Route technologies, only recently have placement optimizations been viewed from the perspective of routing. To this end, we demonstrate that Steiner-tree Wirelength (StWL) correlates with Routed Wirelength (rWL) much better than the more common Half-Perimeter Wirelength (HPWL) objective and the Minimum Spanning Tree (MST) objective. We then develop a new technique to optimize StWL in global and detail placement without a significant runtime penalty. This new optimization, along with congestion-driven whitespace distribution, improves overall Place-and-Route results, making the use of HPWL unnecessary. Our placer ROOSTER outperforms all published academic results in Place-and-Route, and compared to Cadence placement tool Amoeba-place achieves a 26% reduction in routed wirelength (after NanoRoute) as well as a 3% reduction in via counts.

Additionally, our empirical results provide ample evidence that the fidelity of net length estimates is more important than their accuracy in Place-and-Route. The new data structures that make our min-cut algorithms fast can also be useful in multi-level analytical placement.

At the end of the talk, I will briefly describe our ongoing work on incremental placement and floorplan repair.

Biography

Igor L. Markov is an assistant professor of Electrical Engineering and Computer Science at the University of Michigan. He received his M.A. in Mathematics and Ph.D. in Computer Science from UCLA. Prof. Markov's interests are in combinatorial optimization with applications to the design and verification of integrated circuits, as well as in quantum logic circuits. In 2001, Prof. Markov was awarded the DAC Fellowship and received the IBM University Partnership Award. Prof. Markov received the 2004 IEEE CAS Donald O. Pederson paper-of-the-year award and the 2004 ACM SIGDA Outstanding New Faculty Award. He won the best paper award at DATE 2005, as well as the NSF CAREER and the Synplicity Inc. Faculty Awards.

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**Coffee and cookie will be served. For more information about the VLSI Seminar Series,
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