



THE COMPUTER ENGINEERING RESEARCH CENTER
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Circuits and Design Methodologies for Scaled CMOS Technologies

Abstract

As CMOS scales to its physical limits with subwavelength lithography, it becomes increasingly challenging to fabricate integrated circuits with sufficient yield and affordable cost with improved performance. Below 65nm feature sizes, as well as beyond the life of CMOS, it becomes increasingly apparent that circuits must be constructed from simpler, more regular structures and geometry patterns than those presently used today. In this presentation we describe the use of regular logic and circuit fabrics for defining the underlying silicon geometries onto which scaled CMOS circuits should be mapped. While one might expect some area and performance penalty with such regularity enforcement, our work has found that with careful selection of the regular circuits and supporting design methodology, we can mitigate and ultimately eliminate such penalties. We will show implementation examples for digital, analog and RF circuits and technologies.

Biography

Larry Pileggi is the Tanoto professor of electrical and computer engineering and the Director of the Center for Silicon System Implementation at Carnegie Mellon University. He began his career as an IC designer for Westinghouse Research, where in 1986 he was recognized with the corporation's highest engineering achievement award. In 1989 he received his Ph.D. in Electrical and Computer Engineering from Carnegie Mellon University and began his academic career as a faculty member at the University of Texas at Austin. In 1995 he joined the faculty at Carnegie Mellon University. His research interests include various aspects of digital and analog design and electronic design automation. He has received various awards including the 1990 and 1999 Best CAD Transactions Paper Awards, a 2003 DAC best paper award, a 2004 ICCAD best paper award, an NSF Presidential Young Investigator Award, the 1991 and 1999 Semiconductor Research Corporation Technical Excellence Awards, and an SRC 1993 Invention Award. He is a co-author of two books, has published over 200 refereed conference and journal papers, and holds 13 U.S. patents. He is a fellow of IEEE.

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Coffee and cookie will be served. For more information about the VLSI Seminar Series, please visit <http://www.cerc.utexas.edu/vlsi-seminar/>