



THE COMPUTER ENGINEERING RESEARCH CENTER

THE VLSI SEMINAR SERIES

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Built-In Soft Error Resilience for Robust System Design

Abstract:

Robust systems are expected to operate correctly in the presence of hardware failures, software malfunctions, malicious attacks and human errors. One design approach for such systems is to rely on conservative design, and limited use of fault-tolerance techniques. The conservative design approach imposes significant power and performance penalties. Hence, most future systems, not just high-end mainframes, will require built-in mechanisms for error correction, diagnostics, self-recovery and repair. Classical fault-tolerance techniques have limited applicability because they are very expensive, and often inadequate.

In this talk, I will describe a new Built-In-Soft-Error-Resilience (BISER) technique for designing robust systems protected from radiation induced soft errors. In the past, soft errors were of concern especially for space applications. However, in sub-65nm technologies, soft error protection is necessary for terrestrial enterprise systems as well. The new BISER technique corrects most flip-flop soft errors resulting in 20-fold reduction in flip-flop soft error rate. The speed and area penalties are negligible, and the chip-level power penalty is roughly 5-8%. In comparison, classical redundancy techniques introduce 40-100% power, performance and area overheads. A simple extension of the BISER technique corrects most soft errors in combinational logic.

Biography:

Subhasish Mitra is an Assistant Professor in the Electrical Engineering Department of Stanford University. Prior to joining Stanford, he was a Principal Engineer at Intel Corporation where he was responsible for developing enabling technologies for robust system. His research interests include robust system design, VLSI design and test, CAD, fault-tolerant computing and computer architecture. He received Ph.D. in Electrical Engineering from Stanford University. Prof. Mitra has published more than 70 technical papers in leading conferences and journals. His X-Compact technique for test compression is being used by more than 40 Intel products. He has recently been awarded the Donald O. Pederson Award for the best paper published in the IEEE Transactions on CAD, a Divisional Recognition Award from the Intel Mobility Group, a Best Paper Award at The Intel Design and Test Technology Conference, and the Intel Achievement Award, Intel's highest honor.

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Coffee and cookie will be served. Please visit for more information:

<http://www.cerc.utexas.edu/vlsi-seminar/>