



THE COMPUTER ENGINEERING RESEARCH CENTER

THE VLSI SEMINAR SERIES

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Design in the Nanometer Regime: From Devices to System Architecture

Abstract:

Scaling of technology over the last few decades has produced an exponential growth in computing power of integrated circuits and an unprecedented number of transistors integrated into a single die. However, scaling is facing several problems – severe short channel effects, exponential increase in leakage current, increased process parameter variations, and new reliability concerns. Hence, reliable, low-power designs require a shift in design paradigm. We believe that /device aware circuit and architecture design/ along with statistical design techniques can provide large improvement in power dissipation while providing the required reliability and yield. In this talk I will present device aware CMOS design to address power and reliability problems in scaled technologies for different application domains – high-performance with power as constraint and ultra-low power with reasonable performance. Design techniques at different levels of abstraction (device, circuit, architecture) will be addressed. Different Si and possible non-Si device options will be considered for the nanoscale technology regime.

Biography:

Kaushik Roy received his B.Tech. degree from IIT, Kharagpur, India, and his Ph.D. degree from the Electrical and Computer Engineering Department of the University of Illinois at Urbana-Champaign in 1990. He joined the Electrical and Computer Engineering faculty at Purdue University, West Lafayette, IN, in 1993, where he is currently a Professor and holds the Roscoe H. George Professorship of Electrical & Computer Engineering. His research interests include VLSI design/CAD for nanoscale silicon and non-silicon technologies, low-power electronics for portable computing and wireless communications, VLSI testing and verification, and reconfigurable computing. Dr. Roy has published more than 350 papers in refereed journals and conferences, holds 8 patents, and is the co-author of two books on low power CMOS VLSI design (John Wiley & McGraw Hill).

Dr. Roy received a NSF Career Development Award in 1995, IBM faculty partnership award, ATT/Lucent Foundation award, 2005 SRC Technical Excellence Award, SRC Inventors Award, and best paper awards at the 1997 International Test Conference, the 2000 International Symposium on Quality of IC Design, the 2004 IEEE International Conference on Computer Design, the 2003 IEEE Latin American Test Workshop, the 2003 IEEE Nano and System Society Outstanding Young Author Award (Chris Kim). Dr. Roy is a Founding Technical Advisor of Zenasis Inc. and Research Visionary Board Member of Motorola Labs (2002). He has served on the editorial board of IEEE Design and Test, IEEE Transactions on Circuits and Systems, and IEEE Transactions on VLSI Systems. Dr. Roy is a Fellow of IEEE.

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