



THE COMPUTER ENGINEERING RESEARCH CENTER  
**THE VLSI SEMINAR SERIES**



**Brian A. Moore**  
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## **Hundreds of Cores: Verification Challenges Beyond Quad-core CPUs**

### **Abstract**

Silicon technology scaling will continue to support higher levels of integration towards many-core processors architectures and Tera-Scale computing trends. Additionally, higher levels of silicon variation will require more sophisticated validation and test technologies in support of runtime reliability. This talk reviews these technology trends and the significant advances in design and validation that are required.

### **Biography**

Brian Moore is Director of Validation Research in Intel's Microprocessor Technology Lab. Moore is responsible for directing validation research for Intel's future microprocessors on technology that spans pre-silicon functional validation, post-silicon validation and in-situ runtime validation to support system reliability. Moore joined Intel in 1984, working on the design and validation of the iWarp multicomputer and subsequent interconnect components and protocols for Intel supercomputers, including managing the design and validation of the interconnect components in the Tera-FLOP Supercomputer "ASCI Red". Moore completed a two-year relocation to Israel working on a precursor to the Centrino processor, and recently he managed the formal verification research in Intel's Design & Test Technology group. Previous to joining Intel, Moore worked for Westinghouse International on the Fast Flux Test Facility breeder reactor program and for Rockwell International in the Radioactive Waste Isolation Project. He received a B.S.E.E and M.S.E.E. degrees from Brigham Young University in Utah, graduating in 1986.

**Thursday, February, 15, 2007, ACES 6.304, 5:30 pm**

Coffee and cookie will be served. For more information about the VLSI Seminar Series, please visit

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