



THE COMPUTER ENGINEERING RESEARCH CENTER
THE VLSI SEMINAR SERIES

Dr. Steve Burns
Intel Corporation

**Comparative Analysis of Conventional and Statistical Design
Techniques**

Abstract

We explore the power benefits of changing a microprocessor path histogram through circuit sizing based on statistical timing analysis and optimization (STAO) versus a deterministic timing approach that uses statistical design to establish a global guard-band followed by conventional optimization (SDGG). Using an analytical modeling approach, we quantify the differences in total power between the two approaches while maintaining an equivalent performance distribution. For a relative one sigma random within-die (WID) stage delay variation of 5% representative microprocessor critical paths, the analysis indicates that the STAO approach enables 2% power reduction over the SDGG approach. To achieve a 4% and 6% power reduction through the STAO approach, the process variation needs to increase by a factor of $2\times$ and $4\times$, respectively.

Biography

Steve Burns is a Senior Principal Engineer in Intel Corporation's Strategic CAD Labs based in Hillsboro, OR. Steve has been working in this group for 11 years in the areas of: timing and race analysis for pulsed domino circuits, algorithms and methodology for sizing and power optimization of large synthesis and data-path blocks, new transformation-based design environments, and advanced synthesis algorithms and methods. He currently provides technical leadership to a team of researchers in advanced synthesis algorithms and flows based in Moscow. Before joining Intel, Steve was an Assistant Professor of Computer Science at the University of Washington after receiving a M.S. and PhD. in Computer Science from the California Institute of Technology—and before that he received a B.A. in Mathematics from Pomona College. While at Caltech and the University of Washington, Steve performed research in the area of asynchronous circuit design and CAD tools to enable their design.

Wednesday, February, 28, 2007, ACES 2.402, 5 pm
Coffee and cookie will be served. For more information about the VLSI Seminar Series,
please visit <http://www.cerc.utexas.edu/vlsi-seminar/>