



THE COMPUTER ENGINEERING RESEARCH CENTER
THE VLSI SEMINAR SERIES

Charles J. Alpert
Austin Research Laboratory,
IBM

The Nuts and Bolts of Physical Synthesis

Abstract

Physical synthesis takes an unplaced netlist attempts to place the netlist while simultaneously performing timing closure. It combines optimizations like placement, buffering, repowering, cloning, legalization, routing, etc. under one roof. This talk will discuss why physical synthesis remains a critical problem in VLSI design and describe the building blocks behind a physical synthesis flow. It will discuss issues related to the interactions of the different techniques and technology scaling related issues.

Biography

Chuck received the B.S. and B.A. degrees from Stanford University in 1991. He received the Ph.D. degree in Computer Science from UCLA in 1996. He currently works as a Research Staff Member at the IBM Austin Research Laboratory, serving as the technical lead for the design tools group, primarily working on physical synthesis algorithms and flows. Chuck has published over 80 conference and journal papers, has been awarded 20 patents, and has received the Best Paper Award from the ACM/IEEE Design Automation Conference three times. He is also a co-editor for the forthcoming book, the Physical Design Handbook. Chuck has served as the chair for the Tau Workshop on Timing Issues and the International Symposium on Physical Design. He also serves as an associate editor of IEEE Transactions on Computer-Aided Design. For his work in mentoring SRC funded research, he received the Mahboob Khan Mentor Award in 2001. Chuck was named an IEEE Fellow in 2005.

Wednesday, March, 7, 2007, ACES 6.304, 5 pm
Coffee and cookie will be served. For more information about the VLSI Seminar Series,
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