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Statistical Techniques for Robust Digital Design

Abstract

This presentation will describe practical considerations in incorporating statistical timing into a 65 nm ASIC design methodology. Model-to-hardware correlation and robust design techniques will be stressed. Some of the key research initiatives that were required to achieve such a design flow will be described, along with a list of interesting, open and relevant research problems.

Biography

Chandu Visweswariah received a Ph.D. in Computer Engineering from Carnegie Mellon University in 1989 and has been a Research Staff Member at the IBM Thomas J. Watson Research Center since. He presently manages a circuit and interconnect analysis group. He has developed circuit simulation, circuit optimization and statistical timing tools which are widely used in IBM. He is the author or co-author of one book and over 50 publications; he holds 12 U.S. patents with 16 more in the pipeline. In 2002, he was a visiting faculty at the Eindhoven University of Technology. In 2003 he won an IBM Corporate award for his work on formal circuit optimization. He won a Best Paper award at DAC 2004 and he was profiled in the EE Times "Great Minds, Great Ideas" 2005 project focusing on disruptive innovation. His team won the EDN "Innovation of the Year (EDA Tools Category)" and "Innovator of the Year" awards in 2006 for their work on statistical timing. Two of Chandu's papers were selected for the "Best of ICCAD" compendium of the 40 best papers in the first 20 years of the ICCAD conference. Over the years, Chandu has won two IBM Best Paper Awards, a Supplemental Patent Issue Award, two Outstanding Technical Achievement Awards, seven Research Division Awards and a Blue Chip Award. Chandu is a Fellow of the IEEE.

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