



THE COMPUTER ENGINEERING RESEARCH CENTER
THE VLSI SEMINAR SERIES

Dr. Shawn Searles
Fellow, AMD

An Integrated Quad-Core AMD Opteron™ processor

Abstract

This talk is going to be about the next generation AMD Opteron™ processor that integrates 4-enhanced performance x86 cores (quad-core) each with 512kB L2 cache and an enhanced 128-bit FPU. The cores are integrated with a shared 2MB L3 cache and an enhanced on-chip memory controller that supports up to 4 16-bit HyperTransport™ links and dual-channel 128-bit DDR2/DDR3 interface. The design contains over 450 million transistors fabricated in a 65nm SOI CMOS process with dual stress liners and embedded SiGe for PMOS source/drains. The design utilizes 11-layers of copper interconnect that include advanced low-K dielectrics. The SoC chip was designed to facilitate maximum reuse of functional components and to provide flexibility to create targeted variations. The talk will discuss various circuits used to implement this Microprocessor as well as talking about some of the design challenges and how they were overcome.

Biography

Shawn Searles received his B.Sc.EE from the University of Manitoba in 1987, M.Eng from Carleton University in 1989 and his Ph.D. from the University of British Columbia in 1995. From 1987 to 1992 he worked at Bell Northern Research on SONET systems and Northern Telecom on compact transistor models. From 1995 to 2001 Shawn worked at Intel Corp. on Pentium II, III and IV microprocessors. From 2001 to 2003 Shawn worked at Accelerant Networks on PAM-4 and PAM-2 SERDES that achieved data rates between 5Gb/s and 12Gb/s per lane. From 2003 to the present Shawn has been a Fellow at Advanced Micro Devices (AMD) working on K8 microprocessor designs. Shawn's areas of interest include physical layer hardware design, dynamic circuit design, register-file and cache designs, mixed-signal circuits, statistical analysis methods for modelling of within-die variation and modelling of non-linear phenomena.

Wednesday, March, 28, 2007, ACES Auditorium, 3–4:30 pm
Coffee and cookie will be served. For more information about the VLSI Seminar Series, please visit <http://www.cerc.utexas.edu/vlsi-seminar/>