



THE COMPUTER ENGINEERING RESEARCH CENTER

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Combining Circuits + Architecture to Combat Variability in Nanoscale CMOS

Abstract

Variability is poised to severely degrade performance and power scalability of circuits and systems in nanoscale CMOS technologies. Process, voltage, and temperature variations are well-known effects that occur across wide temporal and spatial scales. With aggressive technology scaling, traditional worst-case design techniques incur too much overhead. Higher-level solutions, combined with innovations at the circuit level, offer a holistic approach that should combat and mitigate the detrimental effects of variability. This talk presents a broad perspective of how circuits and architecture can be combined to address variability in different contexts.

Random and systematic variation can introduce skew between clock phases in a high-speed interleaved transmitter. Instead of applying circuit-level patches, we treat offsets as a form of internal inter-symbol interference (ISI) and show how a look-up table (LUT) based equalizer can compensate internal clock timing and transmitter current mismatch to improve signal integrity. In addition to mixed-signal transceiver blocks, process variation can degrade power and performance of digital systems. We investigate two techniques to combat variability—voltage interpolation and variable latency—applied to a 6-stage floating-point unit (FPU). Experimental results from a 130nm FPU test chip demonstrate how these techniques can compensate for random and correlated device-level variations without compromising performance. Besides process variation, voltage variation can also degrade performance scalability and incur large power overheads. Hence, we investigate the potential for energy savings offered by temporally fine-grained, per-core DVFS using integrated on-chip switching regulators. Our analysis suggests energy savings are possible through fast, per-core DVFS despite the overheads associated with lower-efficiency on-chip regulators.

Biography

Gu-Yeon Wei joined Harvard University in January 2002 and is currently an Associate Professor of Electrical Engineering. Prior to joining Harvard, he spent 18 months at Accelerant Networks in Beaverton, Oregon. Professor Wei received his BS, MS, and PhD degrees in Electrical Engineering all from Stanford University in 1994, 1997, and 2001. His current research interests are in the areas of mixed-signal VLSI circuits and systems design for high-speed/low-power wireline data communication, energy-efficient computing devices for sensor networks, and collaborative software + architecture + circuit techniques to overcome variability in nanoscale IC technologies.

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