



THE COMPUTER ENGINEERING RESEARCH CENTER

**THE VLSI SEMINAR SERIES**

**Minsik Cho**

ECE Dept., The University of Texas at Austin

## **Physical Synthesis for Nanometer VLSI and Emerging Technologies**

### **Abstract**

The unabated silicon technology scaling makes design and manufacturing increasingly harder in nanometer VLSI. On one hand, major design objectives such as timing, power, and noise are often conflicting with each other in modern designs with multi-million gates, resulting in complex design closure. On the other hand, design closure no longer guarantees historical yield norm, requiring ever-challenging manufacturing closure. The conventional contracts between design and fab through design rules are breaking down, due to deep sub-wavelength lithography and growing process variations. However, the semiconductor industry has no choice but to live with the current 193nm lithography for at least another 5 years. Therefore, design/manufacturing integration and co-optimization will be in greater demand than ever. Furthermore, the emerging bio/nano technologies require design and manufacturing closures as well, since the complexity of such bio/nano systems will increase considerably in the near future while their manufacturing technologies may be still immature. Physical synthesis is the key design implementation stage to address such grand challenges in design/manufacturing closures for not only silicon but also bio/nano technologies, because it directly interfaces with both high level designs and low level manufacturing technologies. In this talk, I will present some recent works in the area of physical synthesis for nanometer VLSI design/manufacturing closures, as well as the emerging biochip technologies. In particular, I will focus on various routing aspects in VLSI and biochip designs, since interconnect optimization is a key to the success in terms of routability, noise, manufacturability, and so on. First, I will describe an award-winning global router, BoxRouter, in the design closure perspective. Next, I will present a systematic model-based DFM routing framework to improve printability and minimize random defects in the manufacturing closure perspective. Then, I will discuss digital microfluidic biochip routing, to envision the roles of physical synthesis for future technologies. Last, I will conclude this talk with some future directions.

### **Biography**

Minsik Cho received B.S. degree in Electrical Engineering from Seoul National University, Seoul, Republic of Korea in 1999, and M.S. degree in Electrical and Computer Engineering from University of Wisconsin Madison in 2004. He is currently a Ph.D. candidate (expected to graduate in May 2008) in Electrical and Computer Engineering at The University of Texas at Austin.

He was with Intel during the summer of 2005, and IBM T.J. Watson Research Center during the summer of 2006 and 2007. His current research interests include design/manufacturing closures in nanometer VLSI physical synthesis, design automation for bio/nano technologies, DFM/DFR integration with Test/Diagnosis, design optimization for analog/mixed-signal design, and CAD on future computing platforms.

Minsik Cho has received Korean Information Technology Scholarship in 2002, Best Paper Award Nominations at ASPDAC 2006 and DAC 2006, IBM Ph.D. Scholarship in 2007, ACM/IEEE ISPD Routing Contest Awards in 2007, and SRC Inventor Recognition Award in 2008.

**Friday, March, 21, 2008, ACES 2.402, 3:30–4:30 pm**

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