

Physical CAD Changes to Incorporate Design for Lithography and Manufacturability

Louis K. Scheffer

Cadence Design Systems, Inc.

The next few process generations (65 nm and below) will have serious lithography and manufacturing constraints since the feature size is shrinking much more rapidly than the wavelengths used in manufacturing the chips. This paper starts with a quick tutorial on the Design for Manufacturability problems of these process generations, concentrating primarily on the limitations of optical lithography. The remainder of the talk covers the changes to physical design tools, such as placement and routing, that are needed to cope with these problems.