

## **Managing Cross-talk Noise in UDSM Designs**

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### **Abstract**

Cross-talk from capacitive coupling is one of the prime signal integrity concerns in ultra deep sub-micron designs. Finding closure on noise violations is becoming increasingly tedious. Moreover, timing closure with noise-induced uncertainty poses many difficulties due to the excessive pessimism in today's noise analysis techniques. In this talk, we will discuss the challenges in identifying realistic noise violations and share some of our experiences in evolving an effective noise closure methodology.

### **Biography**

Rajendran Panda holds a B.E.(Honors) in Electrical Engineering from Madurai University, India, an LL.B. (Bachelor of Laws) from Bangalore University, India, and a Ph.D. in Computer Science from University of Illinois, Urbana-Champaign. For over 12 years, he was a practicing Electrical Engineer, working on design, engineering, and construction of numerous projects in power utility, instrumentation and plant automation. Now he is with Motorola, Austin, where he manages the development of a number of CAD tools for back-end design analysis and optimization. His current research interests are in the areas of power and signal integrity, circuit reliability, and low power design techniques.

*Coffee and cookie will be served. For more information about the UT-Austin VLSI Seminar Series, please visit the web. <http://www.cerc.utexas.edu/vlsi-seminar/>*