

Challenges & Opportunities in Nano Scale VLSI Design

Dr. Kevin Zhang
Intel Corporation

March 10, 2004, 5:30pm
Location: ACES 6.304

Abstract

As the technology scaling drives the feature size of transistor below 100nm, it has become increasingly difficult to maintain the conventional scaling trend in performance & density while meeting power requirements in VLSI design. In this talk, many key challenges facing today's high-speed microprocessor design, ranging from CMOS technology scaling, high-performance digital circuits, on-chip power management, and embedded memory are discussed. Some innovative technology and design solutions are presented.

Biography

Kevin Zhang is a Senior Principal Engineer and Senior Design Manager at Portland Technology Development, Intel Corporation. He is currently responsible for Intel's future high-speed and low-power SRAM and other embedded memory development for both microprocessor and communication products. Prior to his current position, he managed the low-power development group for mobile products at Intel. He also worked on multi-Ghz CPU core design for Intel's Pentium 4 processor.

Zhang received his BS and PhD in EE from Tsinghua University, Beijing and Duke University, NC, respectively. He has over 30 publications and has been issued over 25 US patents.

Coffee and cookie will be served. For more information about the UT-Austin VLSI Seminar Series, please visit the web. <http://www.cerc.utexas.edu/vlsi-seminar/>