

ANURAG KUMAR

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Summary

Skilled in VLSI IC design and tool development. Experience in EDA tool development. *Currently seeking an intern position for Summer 2008.*

Education

- University of Texas at Austin
PhD. student, Computer Engineering, GPA 3.89/4 August 2007 – present
- Indian Institute of Technology, Kharagpur, India
B.Tech., Electrical Engineering, GPA 8.98/10 August 2002 – May 2006

Work Experience

Atrenta India Private Ltd. (July 2006 – July 2007)

- Involved in the development of Spyglass-CDC – a tool for detection of Clock Domain Crossings.
- Implemented and modified algorithms for formal and functional verification of synchronization schemes like two-flop, common mux, mux-enable, FIFO and handshake schemes.
- Implemented algorithms for verification of glitch prone circuits and data stability.

Research Experience

UT Design Automation Group, UT Austin (August 2007 – present)

- Designed algorithms for fault tolerant Routing for Microfluidic chips.
- Designed algorithms for DNA microarray placement to minimize border length and secondary structure conflicts.

School of Computing, National University of Singapore (May 2005 – July 2005)

- Developed algorithms for detection and classification of human activities for multimedia surveillance application.
- Developed a new technique for Foreground/background segmentation in a given video stream.

Design of Optimal Signal Classifiers (B.Tech. Thesis)

- Formulated an optimal time-frequency representation along with Support Vector Machine method for classification of non-stationary signals like EEG using Stochastic Genetic Algorithm.
- Designed a method involving partition of auto-correlation space using Singular Value Decomposition for feature extraction of stationary signal.

Term Projects

- Monte-Carlo simulation for SRAM reliability analysis due to process variation
- Model order reduction for emulation based verification
- Design of synchronous serial port and integration with ARM processor
- Design and optimization of 16-bit ALU
- Layout of a 4-bit Memory cell and Delay Model of 1Kb Memory
- Speech Recognition Using Neural Networks (using Conjugate Gradient Method)
- Software Design to estimate the optimized number of transmission lines to transfer a given power over a given distance
- Radio-frequency Identification for fraud detection in health care drug distribution system
- Verilog Implementation of second order Kalman Filter

Graduate Coursework

VLSI-1	Optimization issues in VLSI-CAD	Simulation methods for CAD-VLSI
Dependable Computing	Optimization in Engineering Systems	

Technical Skills

Programming Languages	C, C++, Verilog, VHDL, Perl
Tools	Matlab, Visual Basic, Visual C++, Hspice, Spectre, Cadence Virtuoso, VCS, DesignVision, PrimeTime, Spyglass
Operating systems	Linux, Windows

Awards, Honors and Certifications

Awarded **Microelectronics and Computer Development (MCD) fellowship**, 2007-2009 (University of Texas at Austin).

Chosen the **Best Out-going Academician** -2006 (Nehru, IIT Kharagpur).

Awarded **Merit Based scholarship** for four years of study in IIT Kharagpur.

Represented IIT Kharagpur at **Indo-German Winter Academy-2004**, sponsored by DAAD, Germany.

Research Publications

- Kumar, A. Routray, A. K. Pradhan, B.K.P.Nayak “**Design of Support Vector Machines with Time Frequency Kernels for Classification of EEG Signals**”, International Conference for Biomedical Engineering’05, Singapore

- P. K.Atrey, V. Kumar, A.Kumar, M. Kankanhalli, “**Experiential sampling based foreground/background segmentation for video surveillance**”, International Conference for multimedia and expo-2006, Toronto

Miscellaneous

Date of Birth: 6 March, 1983

Visa Status: F-1 (Student) Visa

Citizen: India