

Ashutosh Chakraborty

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Objective

Application for Intel's 2009-2010 PhD Fellowship.

Education

- **University of Texas at Austin** Austin, TX
Ph.D. Student, Electrical & Computer Engineering GPA 3.91/4.00 2006-present
– Advisor: Prof. David Z. Pan
– Area of research: Algorithms for high-performance circuit design exploiting strained silicon devices.
- **University of Texas at Austin** Austin, TX
M.S.E.E., Electrical & Computer Engineering GPA 3.87/4.00 Jun. 2008
– Relevant courses: VLSI Fabrication, Semiconductor Microlithography, VLSI 1, Physical Design Automation, VLSI Optimization Algorithms, Nanometer IC Design, VLSI Testing, Engineering Programming Languages, Analog Integrated Circuit, Dependable Computing, Logic Synthesis
– Masters Report : “*Analysis and Control of Clock Gating Aggravated NBTI Induced Clock Skew*”
- **Indian Institute of Technology (IIT)** New Delhi, India
B. Tech., Electrical Engineering Sep. 1998 - May. 2002
– Relevant courses: Data Structures in C++, Discrete Mathematics, Microprocessor Design, Circuit Theory, Information Theory, Satellite Communication, Analog Integrated Circuits, Computer Networks
– Thesis: “*A MOS Approach to CMOS Double-Edge-Triggered Flip-Flop Design*”.
– Received **best undergraduate thesis award** (given to one thesis in the whole department)

Research Experience

- **UT Design Automation Group, UT Austin** Austin, TX
Member and Research Assistant Aug. 2006 - present
– Researched layout optimization based on active area dependent mobility of Strained e-SiGe Devices.
– Developed mechanical stress dependent gate sizing and repeater insertion for high performance designs.
– Developed algorithm for congestion aware buffer insertion during placement for timing closure
– Designed algorithms for high-quality cell placement for Structured ASICs
– Developed NBTI aware gated-clock skew analysis technique and optimization methodology
– Demonstrated a congestion aware global router with progressive capacity control/congestion massaging
- **Politecnico di Torino** Torino, Italy
Research Assistant and Graduate Student Aug. 2004 - Aug. 2006
– Designed algorithms for preserving design regularity from logic synthesis to physical design.
– Developed algorithms for cross-channel data redundancy based low power LCD bus encoding.
– Proposed clock-tree synthesis approach to dynamically control thermally induced clock skew.
– Won **Govt. of Italy's federal fellowship** for graduate studies.
- **IBM Solution Research Center** New Delhi, India
Graduate Trainee Jun.-Aug. 2002 & Aug.-Dec. 2001
– Designed static and dynamic low-power meta-stability aperture enhanced flip-flop
– Designed a new flip-flop design by fusing NMOS/CMOS design styles for faster performance

Industry Experience

- **Mentor Graphics Corporation** Noida, India
Senior Member Technical Staff (SMTS) Aug. 2002 - Aug. 2004
– Designed and developed QT based front-end interface for proprietary hardware emulation product connecting distributed machines with hardware emulator (Group of four engineers).
– Implemented Concurrent Messaging System to be used as the common communication protocol among all interacting tools from synthesis down to waveform extraction from emulator.
– Enhanced VHDL co-simulator product to support acceleration of user defined primitives.
– Imparted training on unix-internal (pipes, sockets, RPC) to new recruits.

Co-op/Internships

- **Advanced Micro Devices (AMD)** Austin, TX
Summer Intern (CAD Group) Jun. 2006 - Aug. 2006
– Developed a transistor level threshold voltage assignment tool for constrained timing optimization.
- **Mentor Graphics Corporation** Noida, India
Summer Intern (Emulation Group) May 2001 - Aug. 2001
– Optimized Verilog Cross Compiler (VCC) for runtime and to support 64-bit operating system.

Major Graduate School Course Projects

- **VLSI Fabrication:** Developed performance models for Hybrid Crystal Orientation fabrication technique.
- **VLSI 1:** Designed hardware Co-Dec for encoding LCD Bus data for reduced power consumption.
- **Nano IC Design:** Developed optimal secondary V_{th} value selection methodology for dual V_{th} design styles.
- **Physical Design:** Congestion driven global router based on global capacity reduction.
- **VLSI Testing:** Implemented a very fast concurrent fault simulator.
- **Logic Synthesis:** Developed SATisfiability based global routing tool for routing congestion analysis.
- **Programming Languages:** Developed *Valarray* container with expression templates in C++.
- **Analog Design:** Designed a 100dB, 128 μ W, 120dB CMRR folded-cascode OpAmp using 180nm technology.

Awards and Achievements

- First Prize in placement contest for structured ASICs (*by eASIC Corp, 2008*) [\$25000]
- Rajiv Bhambhavle best under-graduate thesis award - (*by IIT Delhi 2002*) [Rs 1000]
- Fellowship for graduate studies - (*by Govt of Italy 2004-2005*) [€22000]
- Travel grant for CAD-athalon programming contest - (*by ACM 2006, 2007, 2008*) [\$2000]
- Employee Achievement Award - (*by Mentor Graphics Corporation 2003*) [Rs 30000]
- Tuition Assistance (*by UT ECE Department, 2006*) [\$7200]

Teaching Experience

- Guest lecturer for graduate course *VLSI Physical Design Automation* (Fall 2008) in ECE Department at University of Texas at Austin.
- Teaching assistant for undergraduate course *Data Structured in Java* (Fall 2006 & Spring 2007) in ECE Department at University of Texas at Austin.

Publications (Journals, Conferences and Thesis)

- J1 “A MOS Approach to CMOS DET Flop-Flop Design”: P. Varma, B.S. Panwar, *Ashutosh Chakraborty*, Dheeraj Kapoor **TCAS 2002**, Vol 49, No.7. pp 1-4
- J2 “Implementation of a Thermal Management Unit for Canceling Temperature-Dependent Skew Variations”: *Ashutosh Chakraborty*, et al.: **Integr. VLSI Journal 2008**, Vol 41, No. 1, pp. 2-8.
- J3 “Dynamic Thermal Clock Skew Compensation Using Tunable Delay Buffers”: *Ashutosh Chakraborty*, et al.: **TVLSI 2008**, Vol 16, No. 6, pp. 639-649.
- J4 “ECO Placement for Stress Aware Timing Optimization for Si-Ge Devices”: *Ashutosh Chakraborty* and David Z. Pan (under preparation)
- C1 “Low-Voltage, Double-Edge-Triggered Flip Flop”: Pradeep Varma, **Ashutosh Chakraborty**, **PATMOS 2003**. pp 11-21
- C2 “Evaluating Regularity Extraction in Logic Synthesis”: *Ashutosh Chakraborty*, Davide Pandini, A. Macii, E. Macii, M. Poncino, **ISSCS 2005**. pp 641-644
- C3 “Exploiting Cross-Channel Correlation for Energy Efficient LCD Bus Encoding”: *Ashutosh Chakraborty*, Enrico Macii, Massimo Poncino, **PATMOS 2005**. pp 297-307
- C4 “Energy-Efficient Encoding for HDCP Protected Digital LCD Interfaces”: *Ashutosh Chakraborty*, Enrico Macii, Massimo Poncino, **ISSCS 2005**. pp 19-22

- C5 “Dynamic Management of Thermally-Induced Clock Skew”: *Ashutosh Chakraborty*, K. Duraisami, A. Sathanur, P. Sithambaram, A. Macii, E. Macii, M. Poncino, **PATMOS 2006**. pp 214-224
- C6 “Implications of Ultra Low Voltage Devices on Techniques and Tools for High-Performance VLSI Circuits”: *Ashutosh Chakraborty*, K. Duraisami, A. Macii, E. Macii, M. Poncino, A. Sathanur, P. Sithambaram, **ISCAS 2006 (invited)**, pp 4-7
- C7 “Dynamic Thermal Clock Skew Compensation Using Tunable Delay Buffers”: *Ashutosh Chakraborty*, K. Duraisami, A. Sathanur, P. Sithambaram, et al. **ISLPED 2006**, pp 162-167
- C8 “Thermal Resilient Bounded-Skew Clock Tree Optimization Methodology”: *Ashutosh Chakraborty*, P. Sithambaram, K. Duraisami, A. Macii, E. Macii, M. Poncino, **DATE 2006**. pp 832-837
- C9 “Layout Level Timing Optimization by Leveraging Active Area Dependent Mobility of Strained-Silicon”: *Ashutosh Chakraborty*, Sean X. Shi, David Pan: **DATE 2008**, pp 849-855
- C10 “An Integrated Nonlinear Placement Framework with Congestion and Porosity Aware Buffer Planning”: Tung-Chieh Chen, *Ashutosh Chakraborty*, David Z. Pan: **DAC 2008**, pp 702-707
- C11 “Analysis and Optimization of NBTI Induced Clock Skew in Gated Clock Trees”: *Ashutosh Chakraborty*, Gokul Ganesan and David Z. Pan: **DATE 2009 (to appear)**
- C12 “On Stress Aware Active Area Sizing, Gate Sizing, and Repeater Insertion”: *Ashutosh Chakraborty* and David Z. Pan: **ISPD 2009 (to appear)**
- C13 “RegPlace: A High Quality Opensource Placement Framework for Structured ASICs”: *Ashutosh Chakraborty*, Anurag Kumar and David Z. Pan: (*submitted*)
- T1 “A MOS Approach to CMOS Double-Edge-Triggered Flip-Flop Design”: *Ashutosh Chakraborty*: **Undergraduate Thesis**, Department of Electrical Engineering, IIT Delhi, 2002
- T2 “Analysis and Control of Clock Gating Aggravated NBTI Induced Clock Skew”: *Ashutosh Chakraborty*, **Masters Report**, University of Texas at Austin, 2000

Selected Review Activities

IEEE Transactions on Computer-Aided Design (TCAD)
 IEEE Transactions on Very Large Scale Integration (TVLSI)
 IEEE Transactions on Circuits and Systems I (TCAS-I)
 IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)
 IEEE/ACM Design, Automation Conference (DAC)

Skills & Activities

Languages/Scripting: C/C++/Java, TCL, Perl, SPICE/HDLs, Unix shells
Applications: MatLab & Mathematica, Cadence ICFB/Encounter, Synopsys Primetime/DC etc
Miscellaneous: Strong verbal/written communication skills, self-motivated and good team-worker
Fabrication: Acetone/Ethanol clean, HF Etch, Photoresist/Lithography, Diffusion, Masks alignment
Membership: Student member of IEEE since 2002.