Ashutosh Chakraborty

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Objective

Internship for summer 2008 loosely in the area of performance estimation/optimization or process simulation of strain engineered silicon devices (eSiGe, STI, liners etc types).

Education

- **University of Texas at Austin** — Austin, TX
  PhD. Student, Electrical & Computer Engineering — *2006-present*
  - Advisor: Prof. David Z. Pan
  - Relevant courses: VLSI Fabrication, Semiconductor Microlithography, VLSI 1, Physical Design Automation, Optimization Algorithms, Nanometer IC Design, VLSI Testing
  - Area of research: CAD for Strained Silicon devices and NBTI Aware Design methodology

- **Indian Institute of Technology (IIT)** — New Delhi, India
  B. Tech., Electrical Engineering — *Sep. 1998 - May. 2002*
  - Relevant courses: Data Structures in C++, Discrete Mathematics, Microprocessor Design, Circuit Theory, Information Theory, Satellite Communication, Analog Integrated Circuits
  - Best undergraduate thesis award (given to one thesis in the whole department each year)

Research Experience

- **UT Design Automation Group, UT Austin** — Austin, TX
  Member and Research Assistant — *Aug. 2006 - present*
  - Worked on performance driven layout optimization based on active area dependent mobility of SiGe S/D type Strained Si Devices.
  - Developed VLSI Global Router with progressive capacity control and congestion massaging techniques to mitigate congestion.
  - Developed algorithm for congestion aware buffer insertion during placement for timing closure
  - Developed NBTI aware gated-clock skew analysis technique and optimization methodology

- **Politecnico di Torino** — Torino, Italy
  Research Assistant and Graduate Student — *Aug 2004 - Aug. 2006*
  - Designed algorithms for preserving design regularity from logic synthesis to physical design
  - Designed algorithm for Cross-channel data redundancy based low power LCD bus encoding
  - Proposed clock-tree synthesis approach to dynamically control thermally induced clock skew
  - Funded by Govt. of Italy's federal scholarship for graduate studies won through competitive selection procedure

- **IBM Solution Research Center** — New Delhi, India
  Graduate Summer Intern — *June 02 - Aug. 02 and Aug 2001 - March 2002*
  - Designed static and dynamic low-power meta-stability aperture enhanced flip-flop
  - Designed a new flip-flop design by fusing NMOS/CMOS design styles for faster performance

Previous Co-op/Internships

- **Advanced Micro Devices (AMD)** — Austin, TX
  Summer Co-op — *June 2006 - Aug 2006*
  - Developed tcl based automatic scripts for transistor level threshold voltage assignment for timing optimization under a given power budget.

- **Mentor Graphics Corporation** Noida, India
  Summer Intern *May 2001 - Aug 2001*
  - Optimized Verilog Cross Compiler (VCC) for runtime and to support 64-bit operating system

Industry Experience

- **Mentor Graphics Corporation** Noida, India
  Senior Member - Technical Staff (SMTS) *Aug 2002 - Aug. 2004*
  - Designed and developed QT based front-end interface for propritery hardware emulation product connecting distributed machines with hardware emulator (Group of four engineers)
  - Implemeted Concurrent Messaging System to be used as the common communication protocol among all interacting tools from synthesis down to waveform extraction from emulator
  - Enhanced VHDL co-simulator product to support accelaration of user defined primitives
  - Imparted training on unix-internal (pipes, sockets, RPC) to new hires
- **Ester Industries** New Delhi, India
  Consulatant Engineer *Jan. 2001 - March. 2001*
  - Implemented PDA based e-mail application using graffitti hand-writing recognition library

Major Graduate School Course Projects

- **Fabrication:** Developing performance models for Hybrid Crystal Orientation fabrication technique
- **VLSI 1:** Design of hardware Co-Dec for encoding LCD Bus data for reduced power consumption
- **Nano IC Design:** Near-optimal secondary V_{th} value selection for dual V_{th} design styles.
- **Physical Design:** Congestion driven global router based on global capacity reduction.
- **VLSI Testing:** Implemented a very fast concurrent fault simulator

Publications

1. "Design and Deployment of Tunable Delay Buffers to Mitigate Thermal Profile Induced Dynamic Clock Skew Violations": *Ashutosh Chakraborty*, K. Duraisami, A. Sathanur, P. Sithambaram, A. Macii, E. Macii, M. Poncino: **TVLSI** *(to appear)*
2. "An Integrated Nonlinear Placement Framework with Congestion and Porosity Aware Buffer Planning": Tung-Chieh Chen, *Ashutosh Chakraborty*, David Pan: **DAC 2008***(to appear)*
3. "Layout Level Timing Optimization by Leveraging Active Area Dependent Mobility of Strained-Silicon Devices": *Ashutosh Chakraborty*, Sean X. Shi, David Pan: **DATE 2008***(to appear)*
4. "A MOS Approach to CMOS DET Flop-Flop Design": P. Varma, B.S. Panwar, *Ashutosh Chakraborty*, Dheeraj Kapoor **TCAS** 2002, Vol 49, No.7. pp 1-4
5. "Thermal resilient bounded-skew clock tree optimization methodology": *Ashutosh Chakraborty*, P. Sithambaram, K. Duraisami, A. Macii, E. Macii, M. Poncino, **DATE 2006**. pp 832-837
6. "Dynamic thermal clock skew compensation using tunable delay buffers": *Ashutosh Chakraborty*, K. Duraisami, A. Sathanur, P. Sithambaram, L. Benini, A. Macii, E. Macii, M. Poncino, **ISLPED 2006**. pp 162-167
7. "Implications of Ultra Low Voltage Devices on Design Techniques and Tools for High-Performance VLSI Circuits": *Ashutosh Chakraborty*, K. Duraisami, A. Macii, E. Macii, M. Poncino, A. Sathanur, P. Sithambaram, **ISCAS 2006**
8. "Dynamic Management of Thermally-Induced Clock Skew": *Ashutosh Chakraborty*, K. Duraisami, A. Sathanur, P. Sithambaram, A. Macii, E. Macii, M. Poncino, **PATMOS 2006**. pp 214-224
9. "Energy-Efficient Encoding for HDCP Protected Digital LCD Interfaces": *Ashutosh Chakraborty*, Enrico Macii, Massimo Poncino, **ISSCS 2005**. pp 19-22

10. "Exploiting Cross-Channel Correlation for Energy Efficient LCD Bus Encoding": *Ashutosh Chakraborty*, Enrico Macii, Massimo Poncino, **PATMOS 2005**. pp 297-307
11. "Evaluating Regularity Extraction in Logic Synthesis": *Ashutosh Chakraborty*, Davide Pandini, A. Macii, E. Macii, M. Poncino, **ISSCS 2005**. pp 641-644
12. "Low-Voltage, Double-Edge-Triggered Flip Flop": Pradeep Varma, **Ashutosh Chakraborty**, **PATMOS 2003**. pp 11-21

Skills

Fabrication: Acetone/Ethanol clean, HF Etch, Photoresist/Lithography, Diffusion, Masks alignment

Languages/Scripting: C/C++/Java, TCL/Perl, SPICE/HDLs, Unix shells

Applications: MatLab & Mathematica, Cadence ICFB/Encounter, Synopsys Primetime/DC etc

Miscellaneous: Strong verbal/written communication skills, self-motivated and good team-worker

Interests

Academic: Graph Theory, Modern Physics, Philosopy

Sports: Playing soccer and swimming

Membership: Student member of IEEE since 2002. Reviewer for DAC 2007

Miscellaneous

Date of Birth: 28th Sepember 1981

VISA Status: F-1 (Student) Visa

Citizen: Republic of India