

Zhiheng Cao

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Education:

Ph.D., Electrical and Computer Engineering, August 2004 - December 2007

The University of Texas at Austin, Austin, TX

Overall GPA: 4.0/4.0

Advisor: Dr. Shouli Yan

Dissertation title: "Low Power A/D Conversion for Deep Submicron CMOS Integration"

Master of Science, Electrical Engineering, April 2004 - July 2004 (withdrawn)

The University of Tokyo, Tokyo, Japan

Bachelor of Engineering, Information Communication Engineering, March 2004

The University of Tokyo, Tokyo, Japan

High-school Diploma, April 1997 – March 2000

Kaisei Gakuen High-school, Tokyo, Japan

Courses Taken in the University of Texas at Austin:

Mixed-Signal System Design and Modeling

VLSI-I

Digital Communications

Digital Signal Processing

Analog/RF Wireless IC Design

Analog Integrated Circuit Design

VLSI-II

Power Electronics

Radio Frequency Integrated Circuit Design

VLSI Fabrication Techniques

Industry Experience:

Senior Engineer, January 2008– Present

RFIC design, Qualcomm, San Diego, CA

Designed and successfully characterized band-gap reference, TCXO buffer, temperature sensor, R-calibration, gm-calibration circuits in 65nm CMOS (for a Bluetooth + FM project)

Investigated digital polar modulation for Bluetooth EDR and WLAN

Design Co-op, July 2007– December 2007

High Performance Analog, Texas Instruments, Dallas, TX

Supervisor: Robert Payne, Marco Corsi

Design of output serial interface (1~3Gbps) for high performance pipelined ADCs using TI's BiCom3 SiGe BiCMOS technology (0.6 μ m CMOS + 30GHz f_T complementary bipolar). Specifically, designed 8b10b encoders, serializers and a 1-4GHz tunable bipolar ring-oscillator based self-biased PLL. A new ring-oscillator tuning / PLL bandwidth auto-adjustment scheme has been used to achieve wide tuning range, constant K_{VCO} , and improved matching of charge pump current sources at low output frequency.

Engineering Intern, July 2006– December 2006

High Speed Converter Group, Analog Devices, Wilmington, MA

Supervisor: Yunchu Li

Designed an LC-VCO system in 0.18 μ m CMOS for high speed DAC internal clock multiplier application. Tunable from 2.3GHz to 4.6GHz over PVT corners with 512 digitally controlled frequency bands. This design includes automatic frequency calibration logic, a digital AAC loop and a novel VCO biasing scheme based on a low noise LDO

regulator and a low bandwidth digital feedback loop to achieve low flicker noise without using large filtering capacitors.

Publications:

Conference Papers

1. **Zhiheng Cao**, Shouli Yan and Yunchu Li, "A 32mW 1.25GS/s 6b 2b/Step SAR ADC in 0.13 μ m CMOS," Paper 30.2, *International Solid State Circuit Conference (ISSCC)*, February, 2008
2. **Zhiheng Cao**, Yunchu Li and Shouli Yan, "A 0.4ps-RMS-Jitter 1-3GHz Ring-Oscillator PLL Using Phase-Noise Preamplification," Paper 12.2, *Symposium on VLSI Circuits*, June 2008
3. **Zhiheng Cao** and Shouli Yan, "A 52mW 10b 210MS/s Two-Step ADC for Digital-IF Receivers in 0.13 μ m CMOS," Paper 12.5 *IEEE Custom Integrated Circuits Conference (CICC)*, September 2008.
4. **Zhiheng Cao**, Tongyu Song and Shouli Yan, "A 14mW 2.5MS/s 14bit Sigma-Delta Modulator Using Pseudo-Differential Split-Path Cascode Amplifiers," Paper 4.2, *IEEE Custom Integrated Circuits Conference (CICC)*, September 2006.
5. Tongyu Song, **Zhiheng Cao** and Shouli Yan, "A 2.7mW 2MHz Continuous-Time Sigma-Delta Modulator with a Hybrid Active-Passive Loop Filter," Paper 4.4, *IEEE Custom Integrated Circuits Conference (CICC)*, September 2006.
6. **Zhiheng Cao** and Shouli Yan, "A Robust Analog Background Calibration Technique for Multi-bit Switched-Capacitor DACs," *IEEE International Midwest Symposium on Circuits and Systems*, vol. 1, pp. 12-16, August 2006.
7. **Zhiheng Cao** and Shouli Yan, "A Study of Voltage Reference Buffers for Low-Power Low-Voltage Switched-Capacitor Circuits," *IEEE International Midwest Symposium on Circuits and Systems*, vol. 2, pp. 502-506, August 2006.
8. **Zhiheng Cao** and Shouli Yan, "A Digital Background Calibration Method for MASH Delta-sigma Modulators by Using Coefficient Estimation," *IEEE International Symposium on Circuits and Systems*, vol. 4, pp. 3091-3094 May 2005.

Journal Papers

9. **Zhiheng Cao**, Shouli Yan and Yunchu Li, "A 32mW 1.25GS/s 6b 2b/Step SAR ADC in 0.13 μ m CMOS," accepted for publication in *IEEE Journal of Solid State Circuits*.
10. **Zhiheng Cao**, Yunchu Li and Shouli Yan, "A 0.4ps-RMS-Jitter 1-3GHz Ring-Oscillator PLL Using Phase-Noise Preamplification," *IEEE Journal of Solid State Circuits*, September 2008, pp. 2079-2089.
11. **Zhiheng Cao**, Tongyu Song and Shouli Yan, "A 14mW 2.5MS/s 14bit Sigma-Delta Modulator Using Pseudo-Differential Split-Path Amplifiers," *IEEE Journal of Solid State Circuits*, Oct. 2007, pp. 2169-2179.
12. Tongyu Song, **Zhiheng Cao** and Shouli Yan, "A 2.7mW 2MHz Continuous-Time Sigma-Delta Modulator with a Hybrid Active-Passive Loop Filter," *IEEE Journal of Solid State Circuits*, Feb. 2008, pp. 330-341.
13. **Zhiheng Cao** and Shouli Yan, "A Robust Analog Background Calibration Technique for Multi-bit Switched-Capacitor DACs," *Electronics Letters*, Vol. 42, Issue 11, May 2006, pp. 618-620.

Books:

14. **Zhiheng Cao** and Shouli Yan, "*Low-Power High-Speed ADCs for Nanometer CMOS Integration*," ISBN 978-1-4020-8449-2, Springer 2008

Patent Applications:

15. **Zhiheng Cao** and Bob Payne, "*Wide tuning bipolar ring-oscillator PLL*," approved for filing by Texas Instruments
16. **Zhiheng Cao** and Shouli Yan, "*Switched Capacitor Circuits*," filed by University of Texas Office of Technology Commercialization, USPTO serial number 11/853509
17. Xiaohong Li, Shouli Yan and **Zhiheng Cao**, "*Digital-to-Analog Converter for Audio Application*," filed by University of Texas Office of Technology Commercialization, USPTO serial number 60/938382

Academic Research Experience:

Research Assistant, Jan. 2005-Aug. 2007

Department of Electrical and Computer Engineering, University of Texas at Austin, Austin, TX

Research Projects:

1. A 1.2V 210MS/s 10-bit two-step ADC in 0.13 μ m CMOS. Taped out in July 2007. It achieved 74dB SFDR/55dB SNDR for 10MHz input and 71dB SFDR for 100MHz input while consuming 52mW.
2. A 32mW (including ADC input driver and reference buffers) 1.25GS/s 6-bit “two-bit-per-step” SAR ADC with 2.5GHz internal clock frequency in 0.13 μ m CMOS. Taped out in March 2007. It achieved 36.5dB SNDR for 20MHz input and >32dB SNDR up to 450MHz input without any digital post processing or offline error correction.
3. A 1-3GHz multiply-by-8 ring-oscillator PLL in 0.13 μ m CMOS featuring digitally configurable power consumption and phase noise performance for a given output frequency and a phase error pre-amplification technique to lower PLL in-band noise without increasing loop filter capacitor size. Taped out in March 2007. Provides clock to the above ADC. Measured 0.4ps RMS jitter for >2.5GHz output and -120dBc/Hz PLL in-band phase noise (100kHz-10MHz).
4. An 84dB (excluding driver opamp, 86dB) SNR, 1.25MHz signal bandwidth, 14mW $\Delta\Sigma$ modulator with 125MHz sampling frequency in 0.25 μ m CMOS. This chip achieved the highest SNR to power consumption ratio among all previously published 1.25MHz signal bandwidth $\Delta\Sigma$ modulators. (Taped out in 2005)

Graduate Research, April 2004-Aug. 2004

Department of Electrical Engineering, University of Tokyo

Investigated analog circuits for VLSI power supply noise measurement and reduction.

Undergraduate Research, April 2003-March 2004

Department of Electrical Engineering, University of Tokyo

Designed and fabricated InP-based photonic integrated circuits.

Relevant Course Projects:

- Design of an UWB analog front-end (broadband LNA, mixers, VGA and anti-aliasing filters)
- Design of a total cost optimized anti-aliasing filter and digital filter for audio application
- Non-idealities modeling of a 20-bit audio delta-sigma modulator in Matlab
- Design and modeling of equalizers (ZFE, MMSE-LE and MMSE-DFE) in Matlab
- Extension of the ARM processor in HDL level

Software Skills

Cadence custom flow (schematic, layout)

SpectreRF

Cadence SKILL and ocean scripting languages

VerilogHDL for synthesis using Synopsys Design Compiler

Agilent ADS

Familiar with productivity enhancement tools under UNIX such as Perl, B-shell scripts and Emacs

Matlab/Simulink

C/C++ (Windows programming using MFC and ATL libraries), Java, C#, Visual Basic

References

Available upon request

Employment Status

H-1B from Oct. 2008

Chinese citizen

Permanent resident of Japan