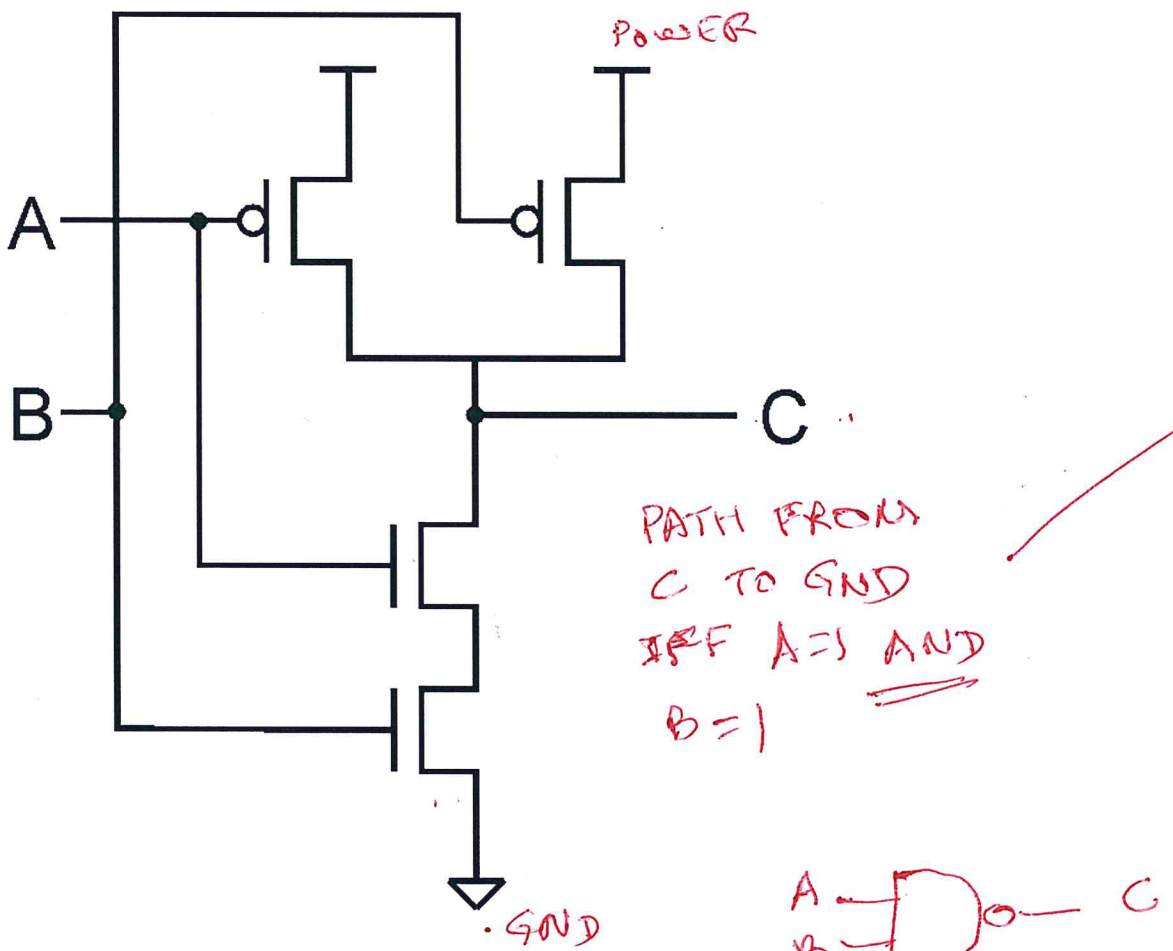
5. Logic Circuits, Storage Elements Sept. 17, 2018 (Chapter 3, 3.3-3.4)

- Logic gates (cont'd)
  - Transistor structures
  - Gate-level circuits
  - De Morgan's law
- Combinational Logic Circuits
  - Decoder
  - Multiplexer
  - Full Adder
  - Programmable Logic Array
- Storage Elements
  - R-S Latch
  - Gated D Latch
  - Register
  - Memory

NAND Gate (AND-NOT)

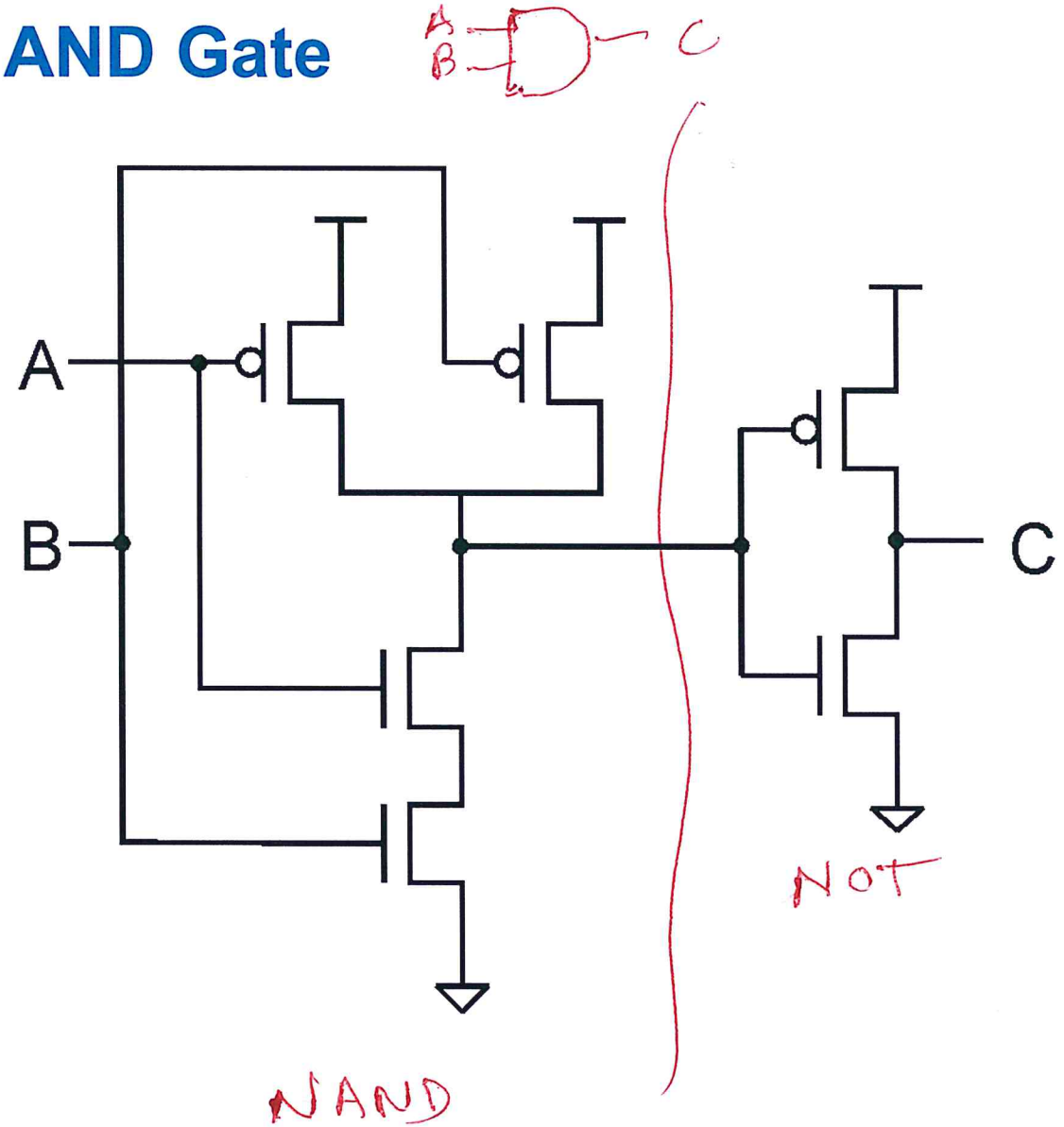


A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

PATH FROM C TO GND IF A=1 AND B=1

Note: Parallel structure on top, serial on bottom.

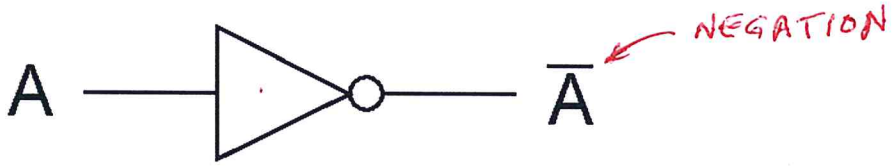
AND Gate



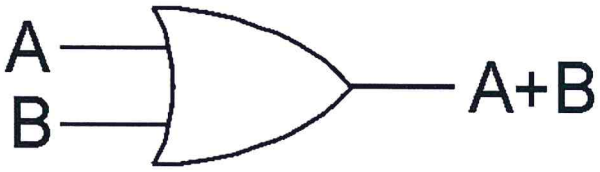
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Add inverter to NAND.

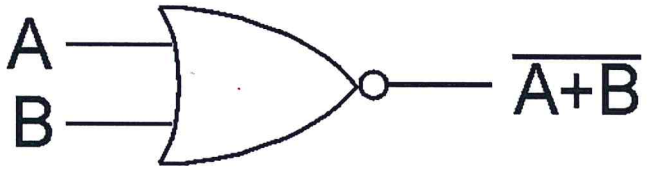
Basic Logic Gates



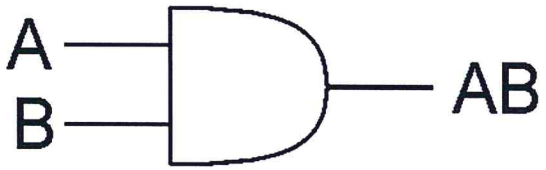
NOT



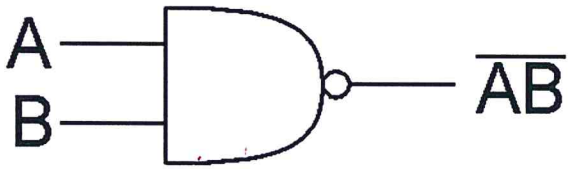
OR



NOR

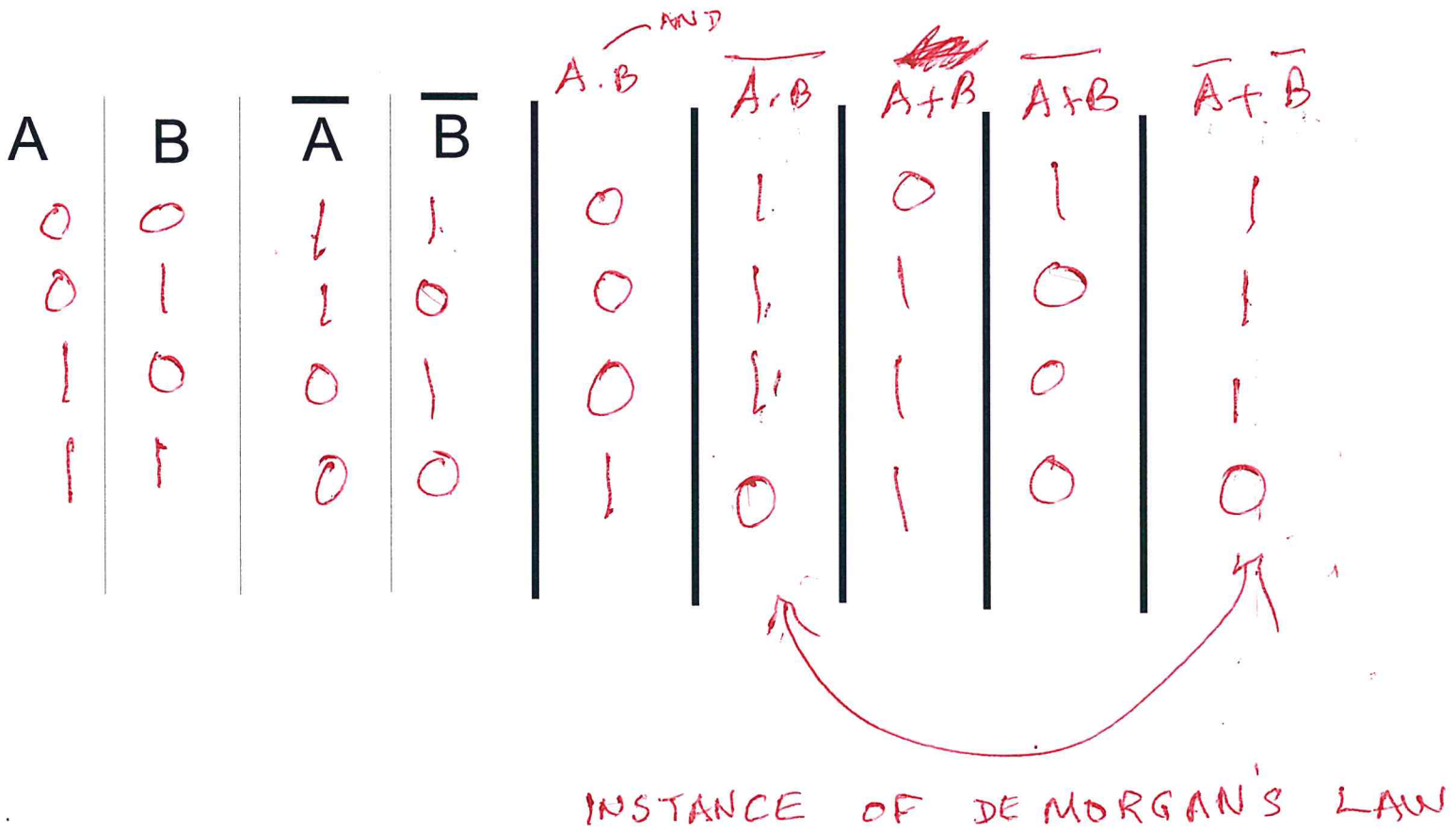


AND

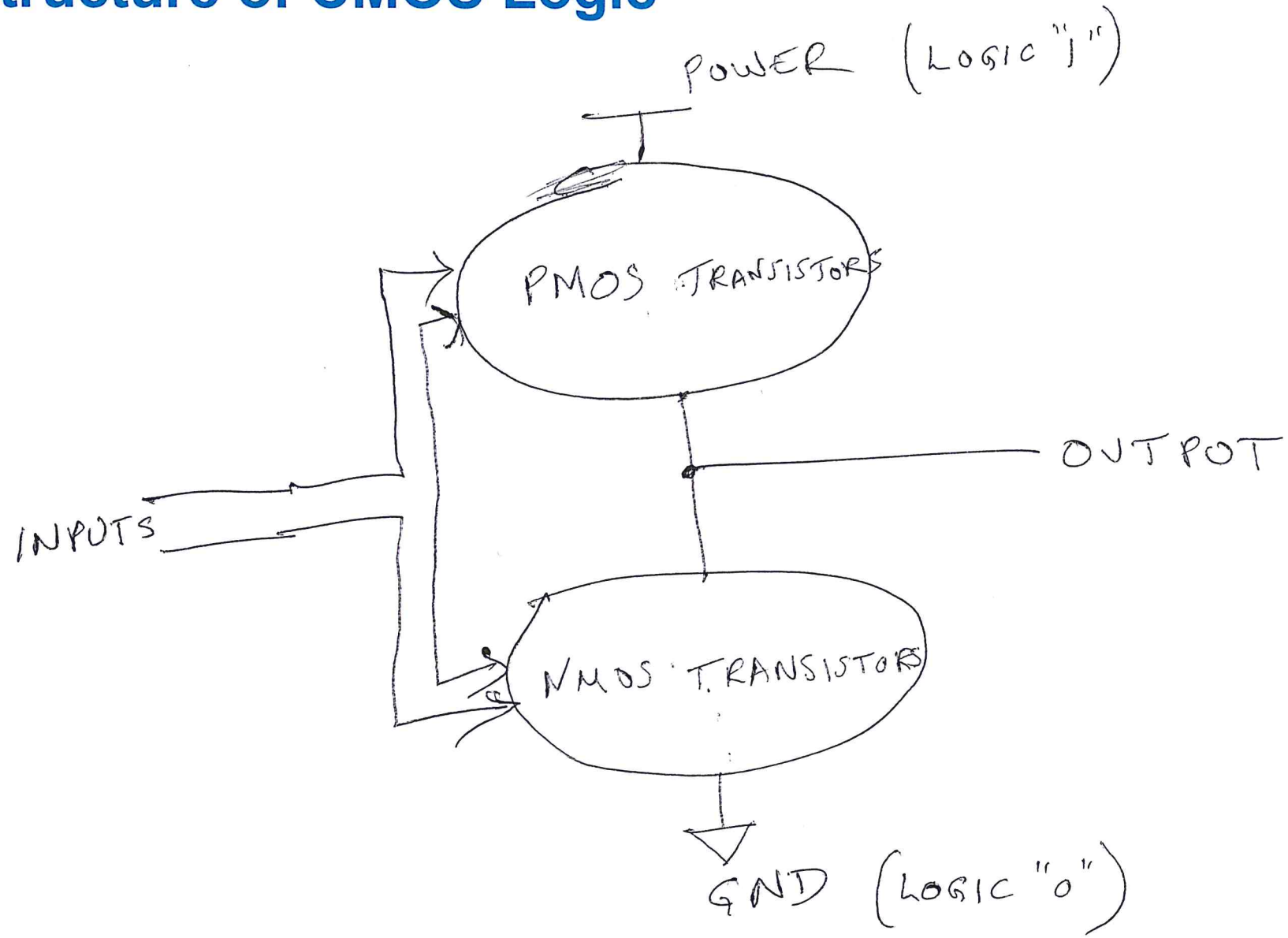


NAND

Truth Tables of Basic Gates



Structure of CMOS Logic

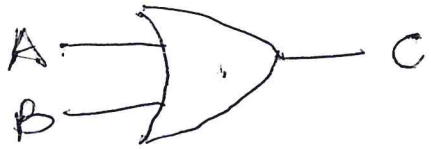


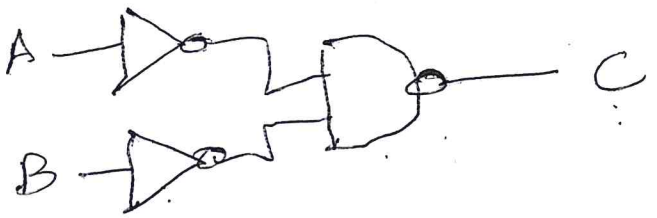
DeMorgan's Law

WHY? CONVERT CIRCUIT BLOCKS - AND → OR
AND → NAND

Converting between gate types (AND to OR, etc.) (with help from NOT)

A	B	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot \overline{B}$	$\overline{\overline{A} \cdot \overline{B}}$	A+B
0	0	1	1	1	0	0
0	1	1	0	0	1	1
1	0	0	1	0	1	1
1	1	0	0	0	1	1

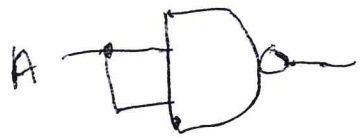




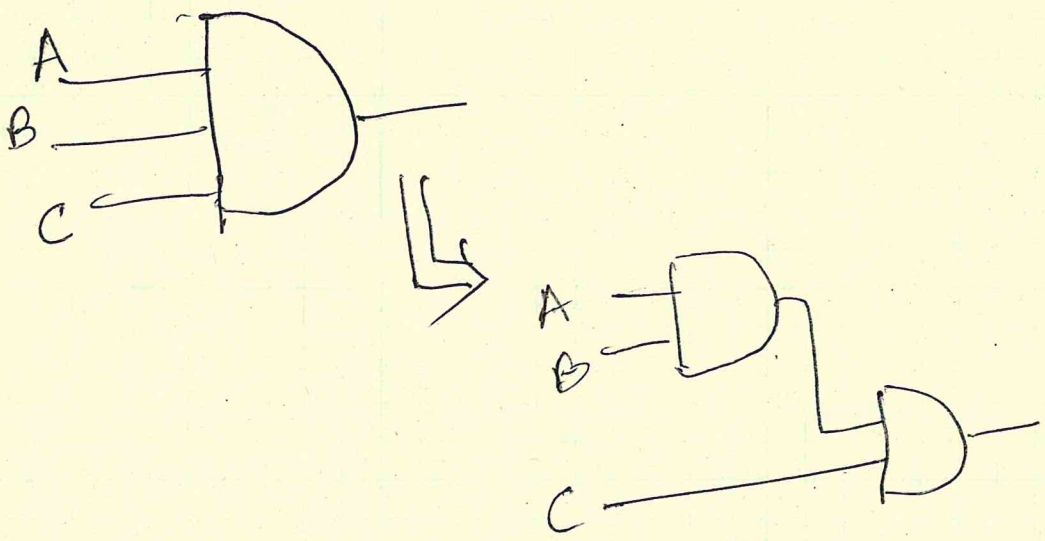
$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

NOT A

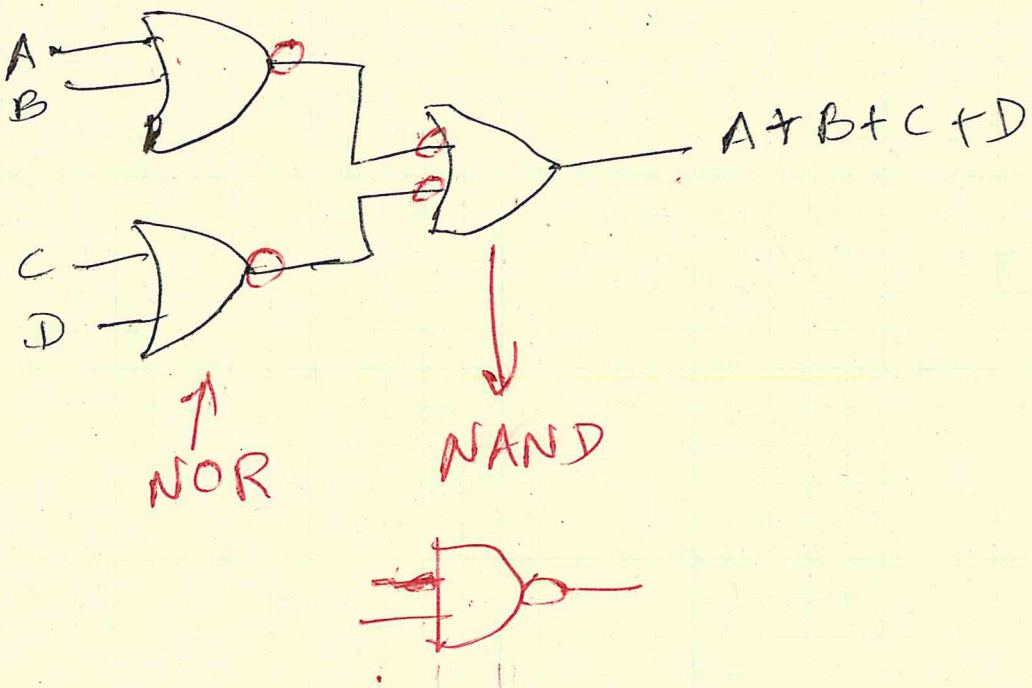


MORE THAN 2 INPUTS



$$A \cdot B \cdot C = (A \cdot B) \cdot C$$

$$A + B + C + D = (A + B) + (C + D)$$

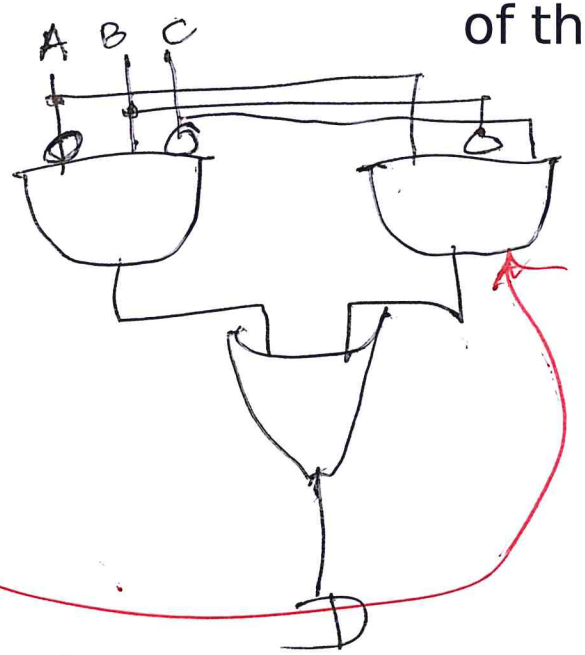


Logical Completeness

Can implement ANY truth table with AND, OR, NOT.

A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

$D = \bar{A} \cdot B \cdot \bar{C} + A \cdot \bar{B} \cdot C$



1. AND combinations that yield a "1" in the truth table.

2. OR the results of the AND gates.

LOGIC FUNCTIONS

1. COMBINATIONAL
   OUTPUT IS A FUNCTION OF INPUTS

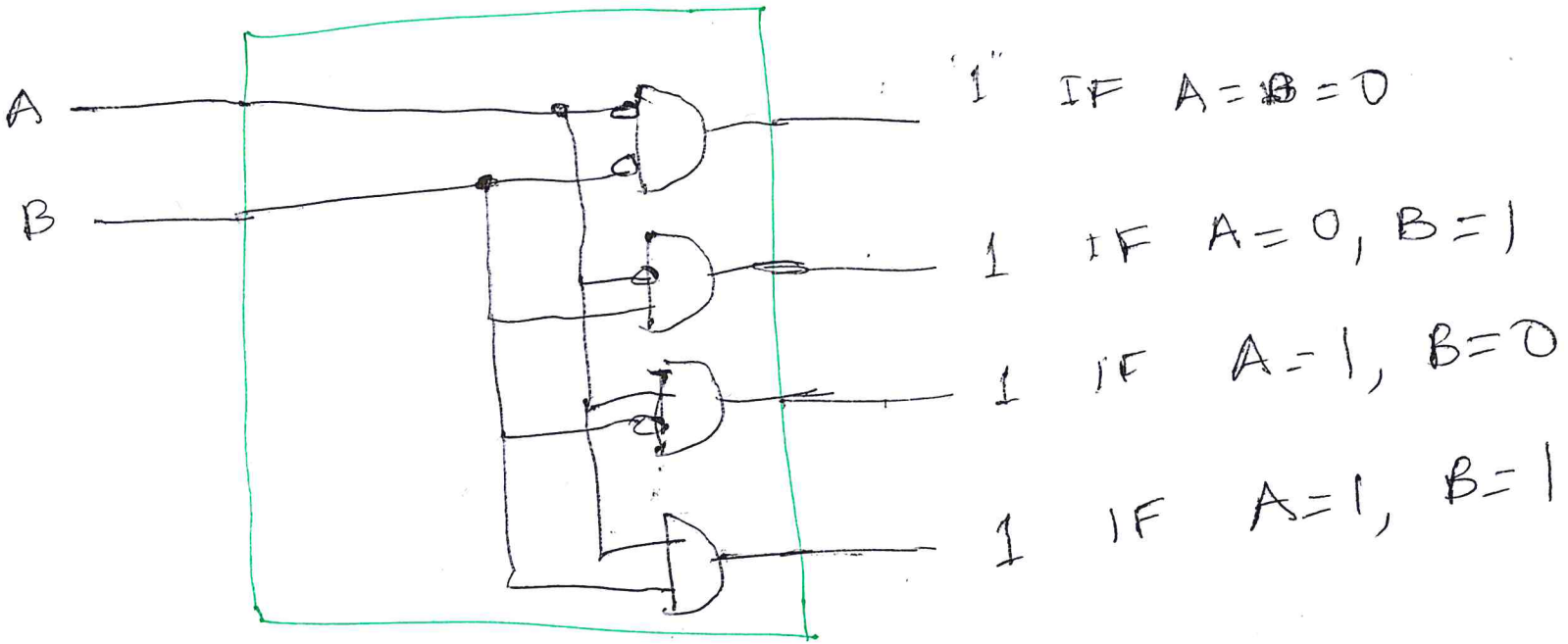
2. SEQUENTIAL
   OUTPUT DEPENDS ON INPUT SEQUENCE

[STORE "STATES" FROM PAST INPUTS]

Decoder

n inputs, 2^n outputs

- **exactly one output is 1 for each possible input pattern**



MULTIPLEXER (MUX)

n-BIT SELECTOR

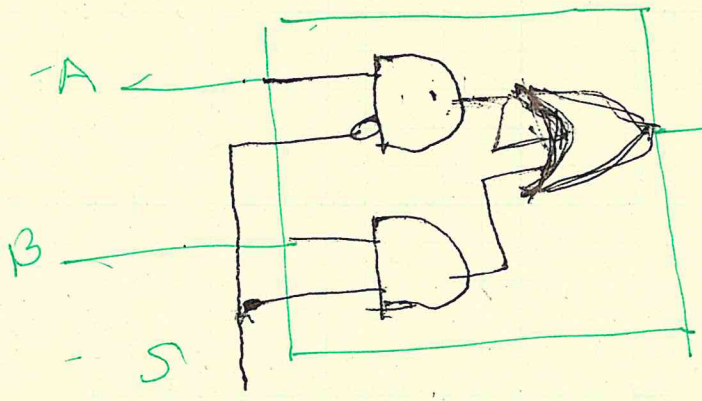
2^n - INPUTS

1 - OUTPUT

FOR 2 BITS,

INPUT A, B

SELECT S



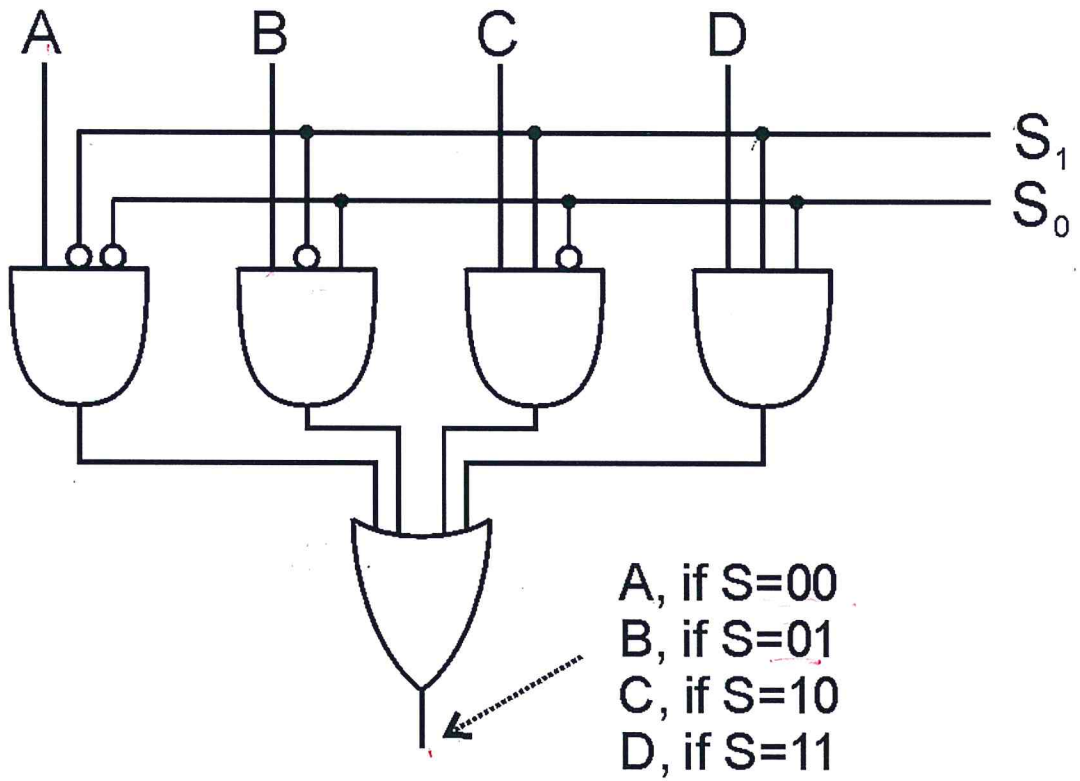
$= \bar{S} \cdot A + S \cdot B$

Multiplexer (MUX)

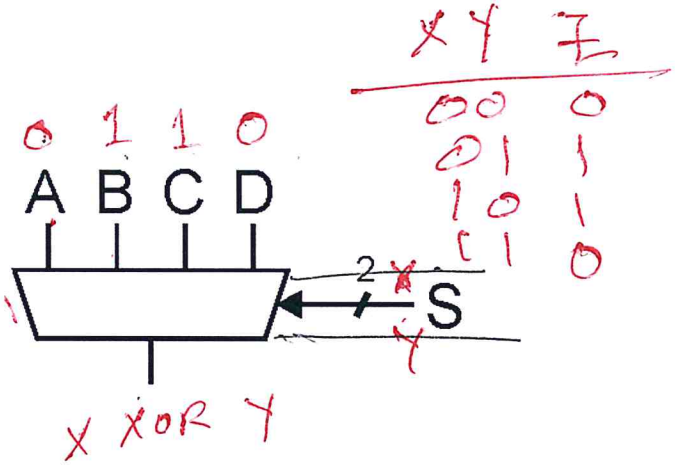
n-bit selector and 2^n inputs, one output

- output equals one of the inputs, depending on selector

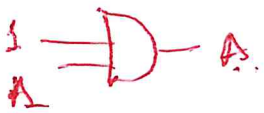
4-INPUT MUX



XOR WITH THIS MUX

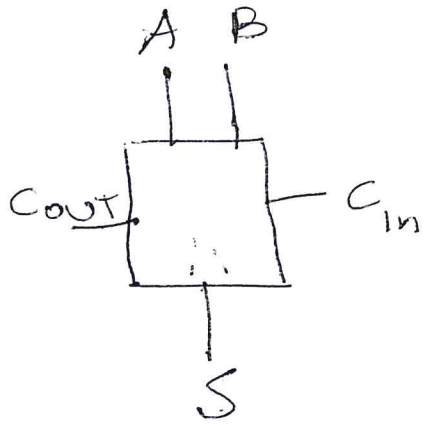


4-to-1 MUX



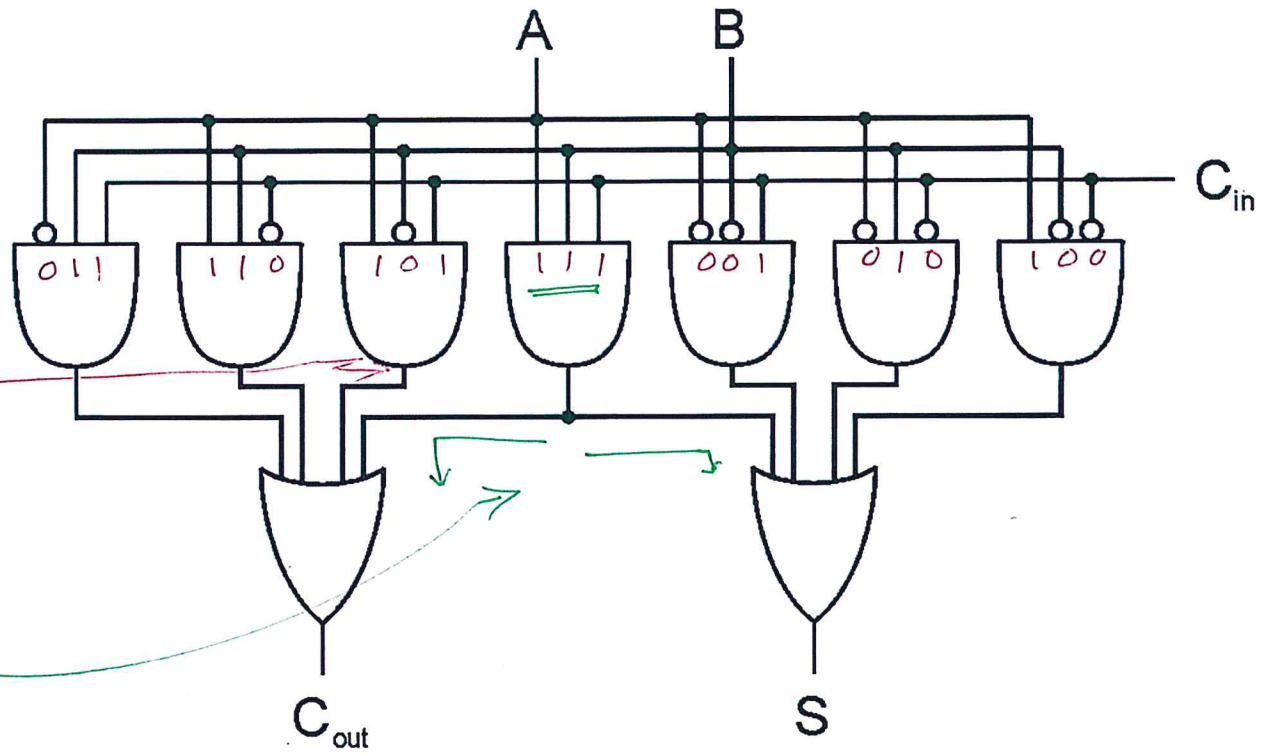
Full Adder

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



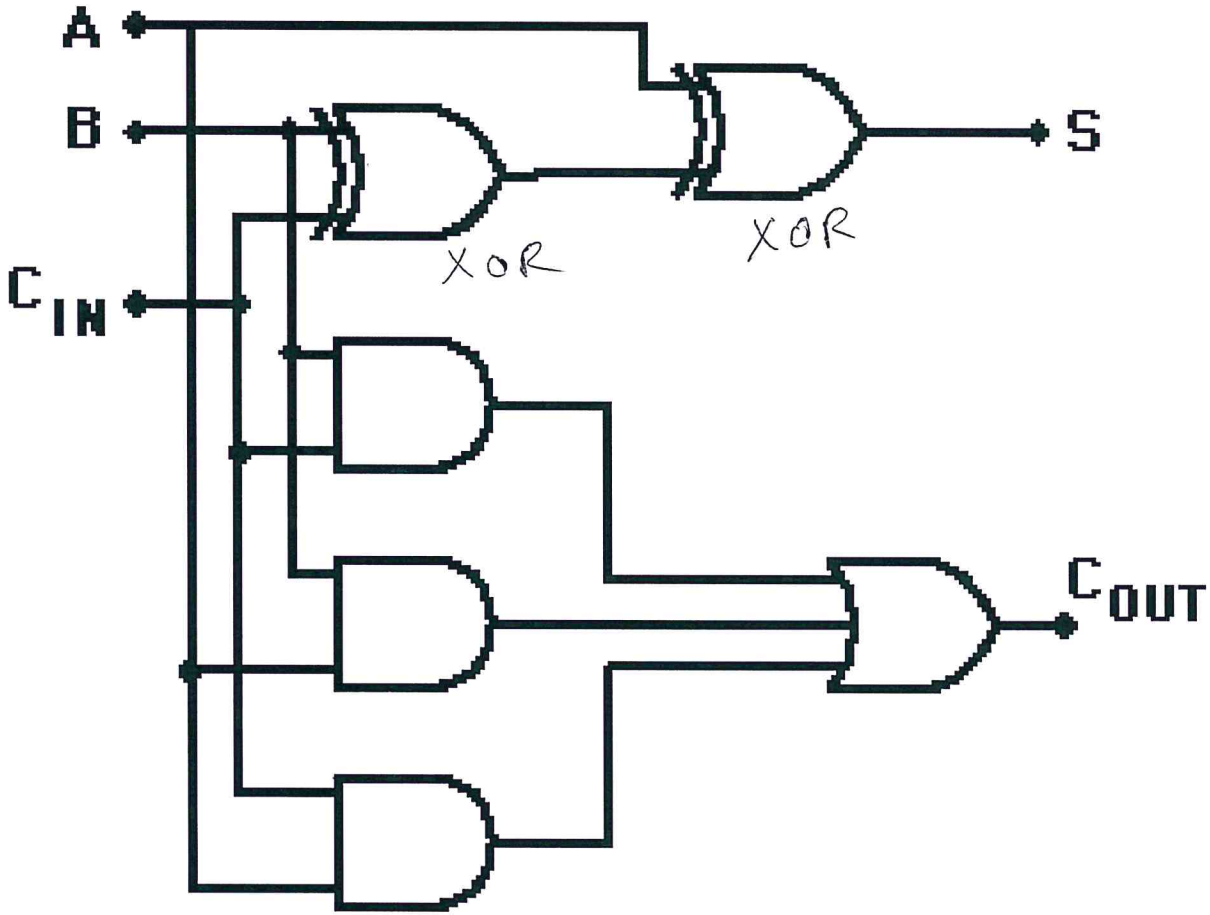
Full Adder

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



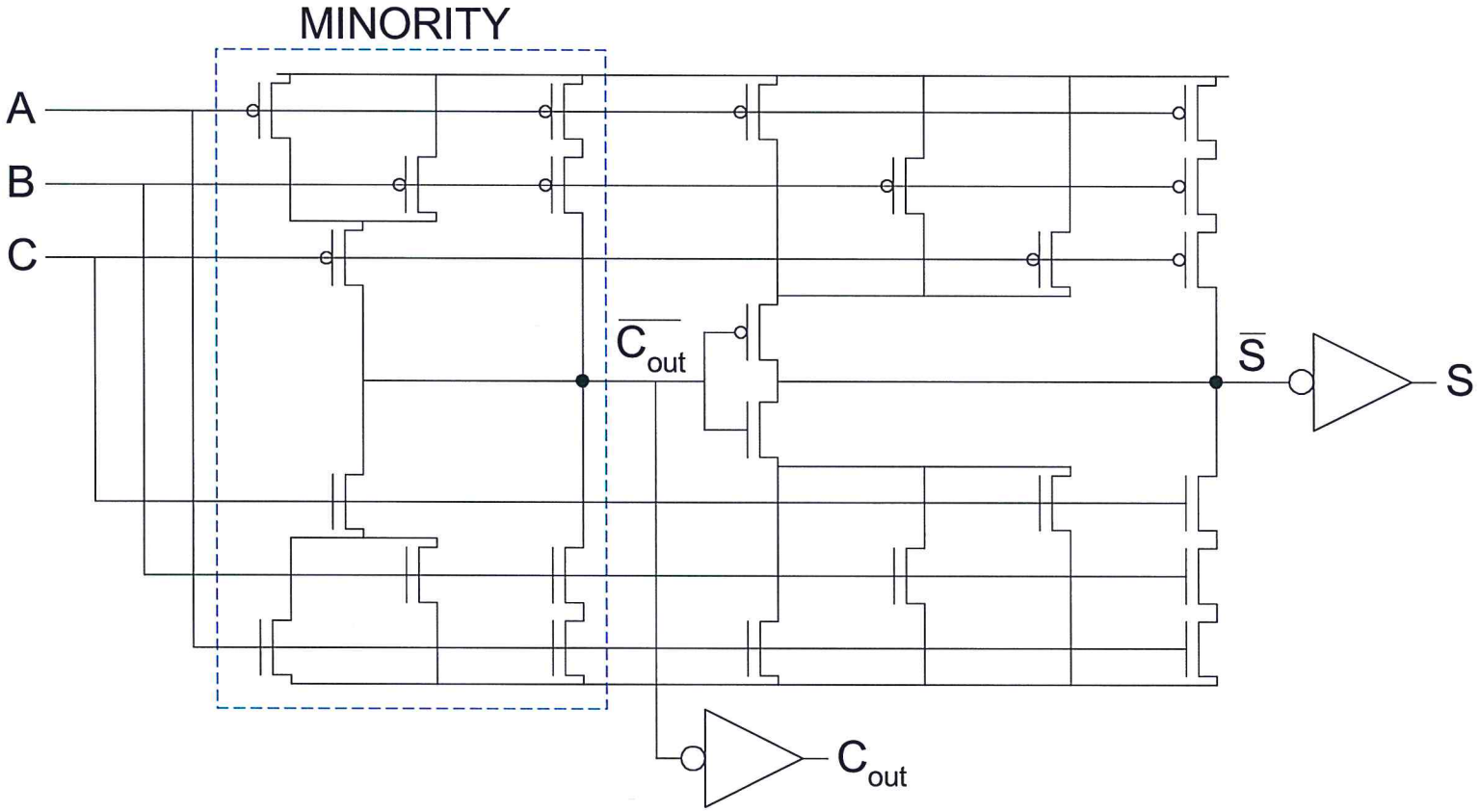
Logic Circuit for Adder

FYI

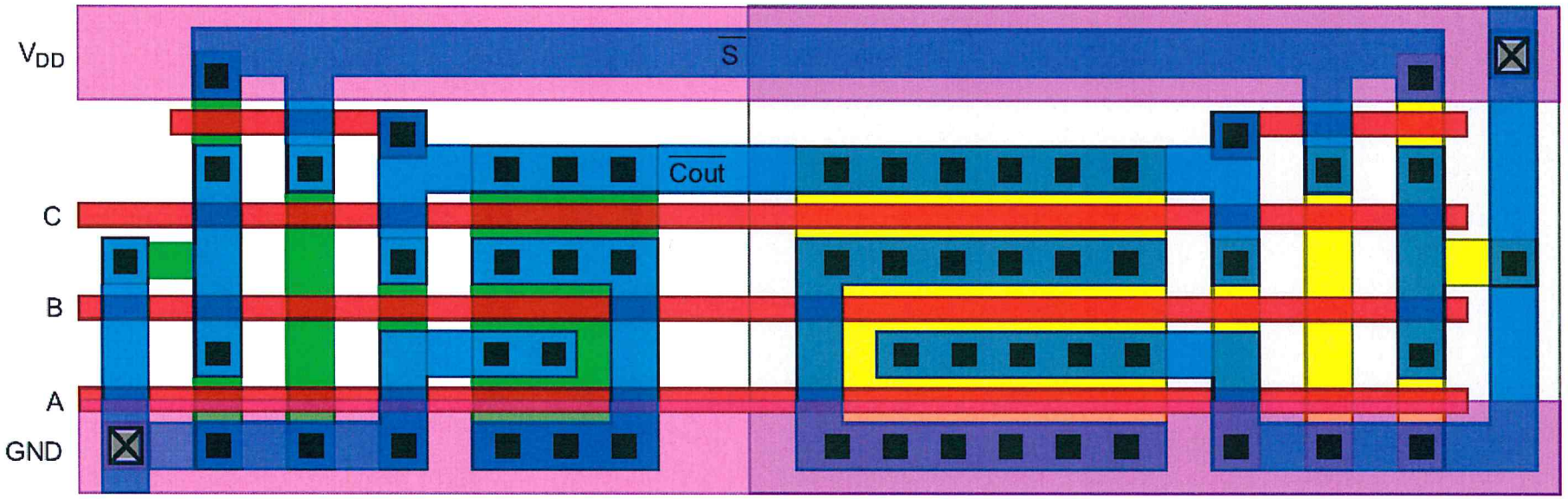


FYI

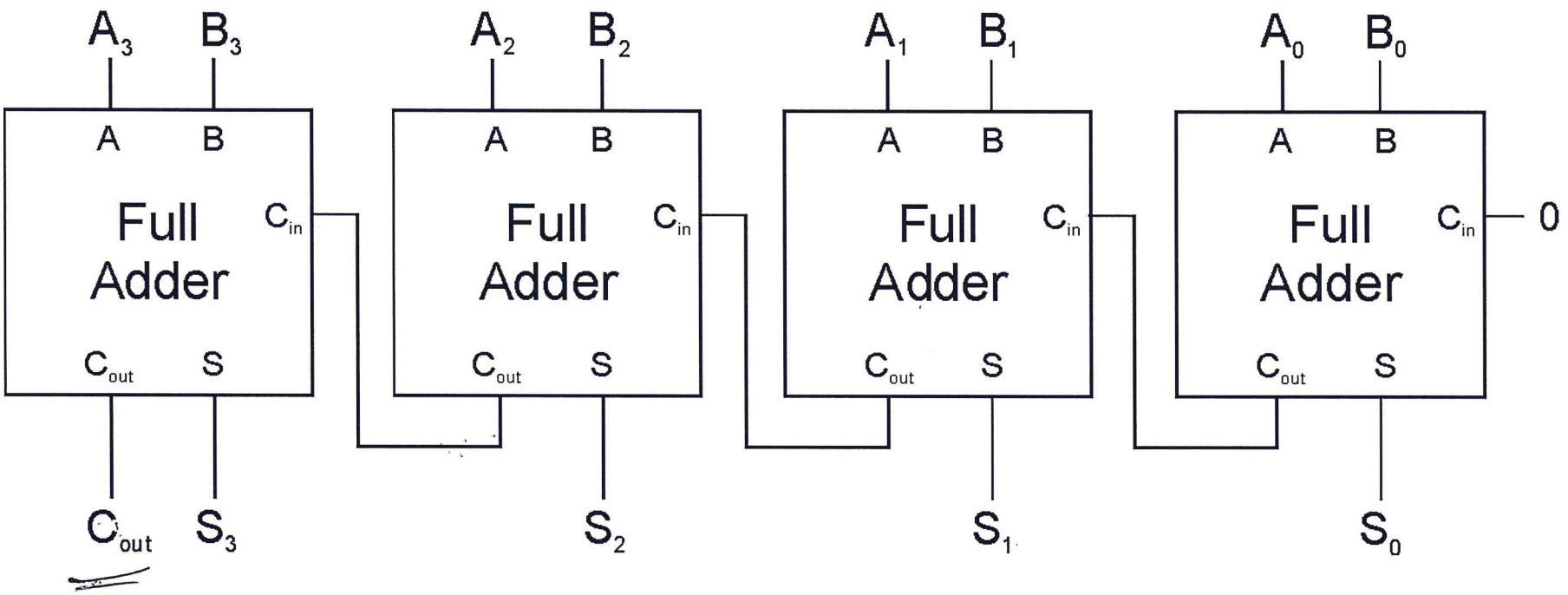
More Detailed View of Adder Circuit: Transistors



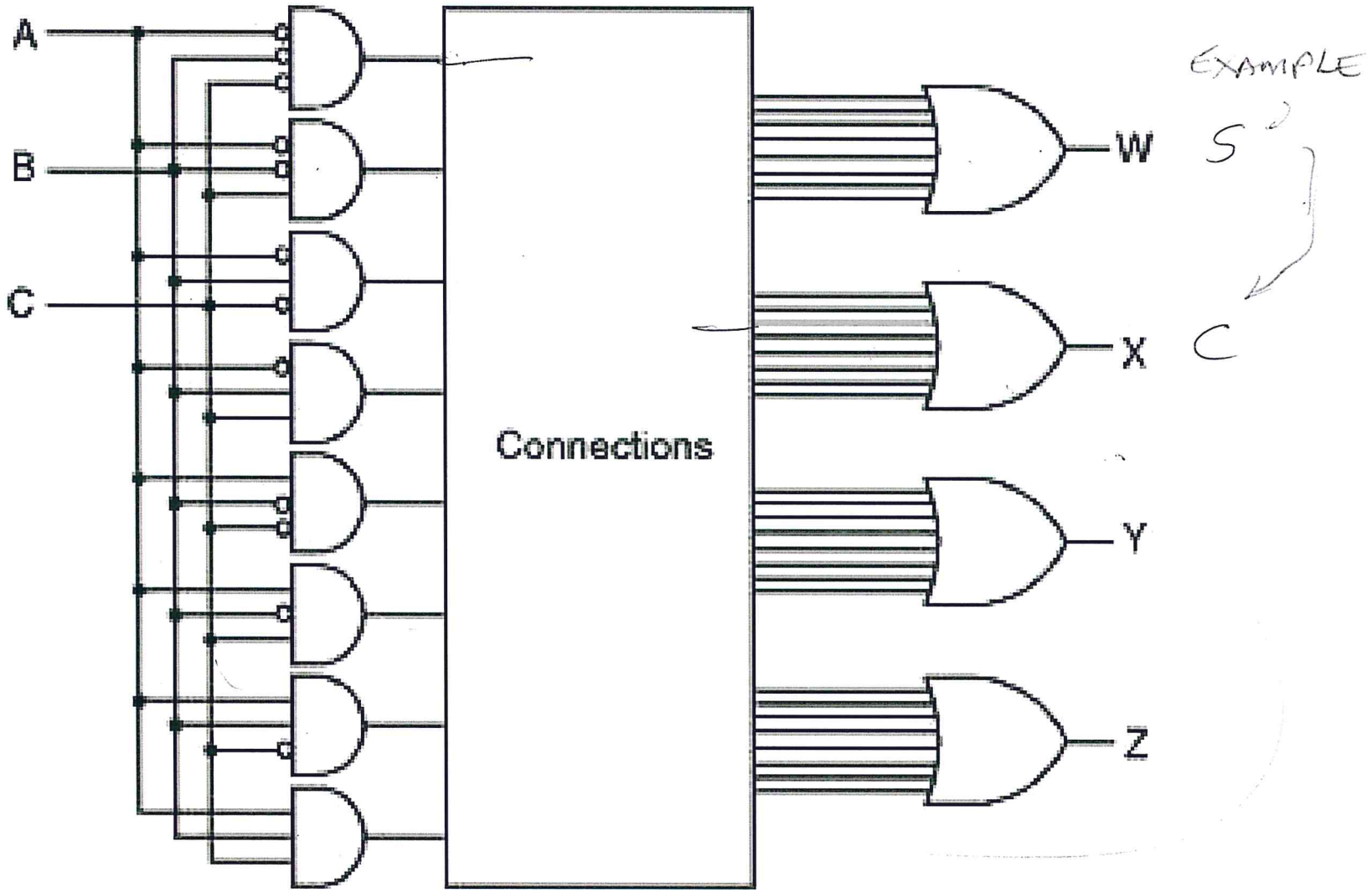
Layout of Adder Cell



Four-bit Adder

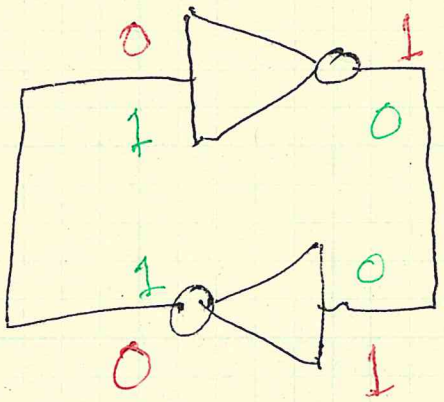


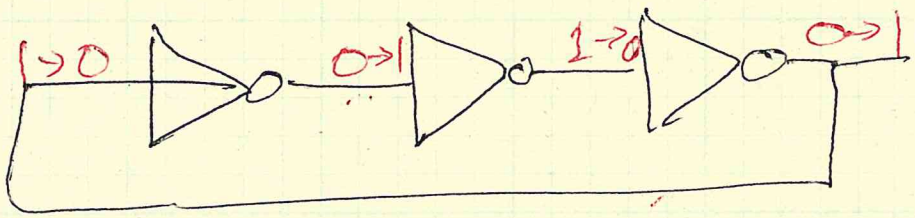
Programmable Logic Array



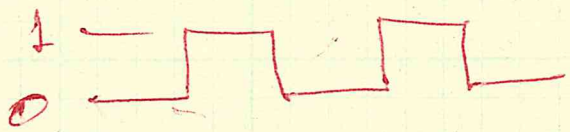
SEQUENTIAL CIRCUIT

[FOR MEMORY, STORAGE]

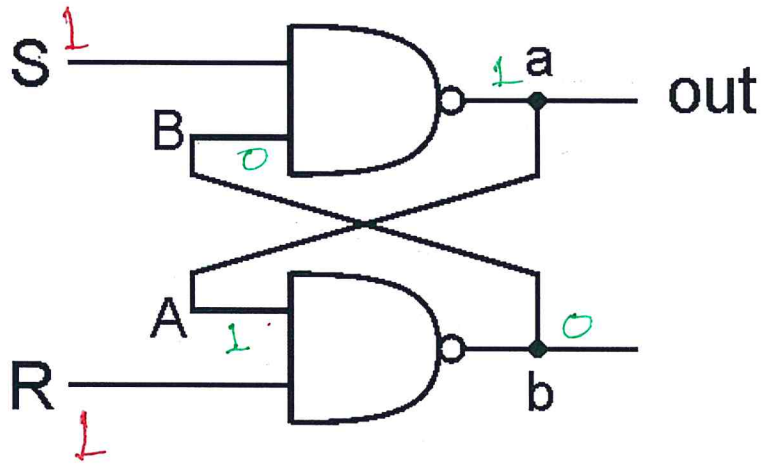




OSCILLATOR



R-S Latch: Simple Storage Element



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