VLSI I, Fall 2017

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Homework No. 2

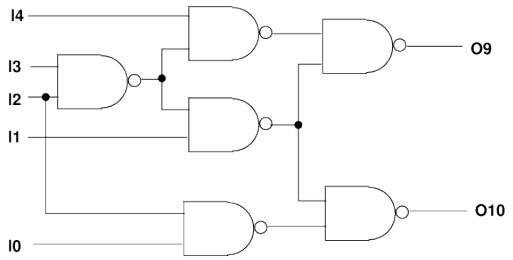
Assigned September 18, 2017, due September 25, 2017

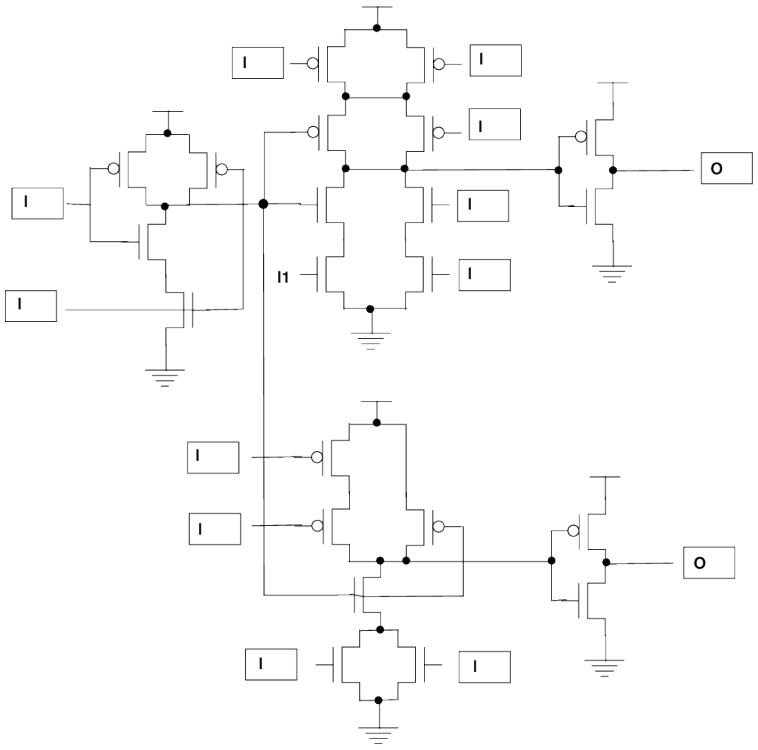
1. Sketch the transistor-level schematic for a single-stage CMOS logic gate for the function, $Y = \overline{(A \cdot B + C \cdot (A + B))}$

2. Realize the following functions using CMOS technology with the **minimum possible number of transistors**. Assume that only the true (uncomplemented) variables are available.

(a) $F = \overline{(a + b + c).d.e}$ (b) $F = \overline{(a + b).c + d}$
(c) $F = (x + y).(x + z)$ (d) $F = a.b + \overline{a}.c + b.c.d$

3. The gate-level circuit below has been implemented with the transistor netlist at the bottom. Label the transistor gate inputs and the circuit outputs so that the gate-level circuit is correctly implemented by the transistor circuit.





4. Problem 2.4 from the Exercises for Chapter 2.

5. Problem 2.9 from the Exercises for Chapter 2.

6. Problem 2.20 from the Exercises for Chapter 2.

7. Problem 2.21 from the Exercises for Chapter 2.

8. Find the voltages at each of the nodes, A, B, C, D, E and F below, assuming that all the nodes are initially at 2.5 V. Use the following circuit parameters.

$V_{dd} = 5V$, $V_{tn} = 0.5V$, $|V_{tp}| = 1.5V$.