Resumé

Jacob A. Abraham
Professor, Department of Electrical and Computer Engineering
Professor, Department of Computer Sciences
Director, Computer Engineering Research Center
Cockrell Family Regents Chair in Engineering
The University of Texas at Austin

CITIZENSHIP: U. S. A.

EDUCATION:

- University of Kerala, India, Electrical Engineering, B.Sc., 1970
- Stanford University, Electrical Engineering, M.S., 1971
- Stanford University, Electrical Engineering and Computer Science, Ph.D., 1974

PREVIOUS ACADEMIC POSITIONS:

- Professor, Department of Electrical and Computer Engineering, Professor, Department of Computer Science, Research Professor, Coordinated Science Laboratory, University of Illinois, 1983 – 1988
- Associate Professor, Department of Electrical Engineering, Research Associate Professor, Coordinated Science Laboratory, University of Illinois, 1980 – 1983
- Assistant Professor, Department of Electrical Engineering, Research Assistant Professor, Coordinated Science Laboratory, University of Illinois, 1975 – 1980
- Acting Assistant Professor, Department of Electrical Engineering and Digital Systems Laboratory, Stanford University, 1974 – 1975

RESEARCH CONTRIBUTIONS:

- **Fault-Tolerant Computing:**
  - *Reliability evaluation*
  - *Algorithm-based fault tolerance*
  - *Software-based fault injection*
- **Automatic Test Generation and Design for Test:**
  - *Memory and Microprocessor testing*
  - *Fault modeling*
  - *Hierarchical fault simulation*
  - *Design of testable circuits*
  - *Use of genetic algorithms for test generation*
  - *Hierarchical test generation*
  - *Testing of analog and RF modules*
  - *Self-testing systems on a chip*
- **Formal Verification:**
  - *Probabilistic verification*
  - *Sequential equivalence checking*

  - *Property checking using abstractions*

- **VLSI Design:**
  - *Design of on-chip sensors*
  - *Design of low-power systems*
  - *High-performance, low power baseband for high data rate wireless communications*

AWARDS AND HONORS:

- Ranked First in the University of Kerala in Engineering, 1970.
- Elected Fellow, Institute of Electrical and Electronics Engineers, Jan. 1, 1985, *for contributions to the testing of large, complex integrated circuits.*
- Beckman Associate, Center for Advanced Study, University of Illinois, 1985-86.
- Listing in *Who's Who in America*, 1986 –.
- Inventor Recognition Award, Semiconductor Research Corporation, 1987.
- IEEE Computer Society Technical Activities Board, TAB Pioneer Award, 1988.
- **Best Paper Award**, 23rd IEEE/ACM Design Automation Conference, June 1993.
- Elected Fellow, Association for Computing Machinery (ACM), 2002.
- **Best Paper Award**, 21st IEEE VLSI Test Symposium, 2002.
- Listed as a **Highly Cited Author** by http://isihighlycited.com (*Science Citation Index*).
- **IEEE Emanuel R. Piore Award**, 2005.
- **Best Paper Award**, 25th IEEE VLSI Test Symposium, 2006.
- **Best Paper Award**, 9th International Symposium on Quality Electronic Design, 2008.

Ph.D. DISSERTATIONS SUPERVISED: 73

Completed Ph.D.s, place of first employment, and Dissertation Titles:

- Warren C. Pratt, April 1977 (EE), University of Illinois at Urbana-Champaign
  Hewlett Packard Company, Fort Collins, Colorado
  "Transformation of Boolean Equations for the Design of Multiple-Output Networks"
- Satish M. Thatte, April 1979 (EE), University of Illinois at Urbana-Champaign
  Texas Instruments Central Research Laboratories, Dallas, Texas
  "Test Generation for Microprocessors"
- Timothy C. K. Chou, May 1981 (EE), University of Illinois at Urbana-Champaign
  Tandem Corporation, Cupertino, California
  "High Performance, High Availability Distributed Processor Systems"
- Gong-Po Mak, April 1982 (CS), University of Illinois at Urbana-Champaign
  Zilog Corporation, Campbell, California
  "The Design of Programmable Logic Arrays with Concurrent Error Detection"

- Kuang-Hua Huang, January 1983 (CS), University of Illinois at Urbana-Champaign
  AT&T Western Electric Engineering Research Center, Princeton, New Jersey
  "Fault-Tolerant Algorithms for Multiple Processor Systems"

- Robert K. Montoye, October 1983 (CS), University of Illinois at Urbana-Champaign
  IBM Thomas J. Watson Research Center, Yorktown Heights, New York
  "Optimization and Testing of nMOS Arithmetic Structures"

- Richard L. Norton, October 1984 (EE), University of Illinois at Urbana-Champaign
  Digital Equipment Corporation, Colorado Springs, Colorado
  "Formal Representation of Computer Architectures"

- Prithviraj Banerjee, January 1985 (EE), University of Illinois at Urbana-Champaign
  University of Illinois, Urbana, Illinois
  "A Theory for Algorithm-Based Fault Tolerance in Array Processor Systems"

- W. Kent Fuchs, April 1985 (EE), University of Illinois at Urbana-Champaign
  University of Illinois, Urbana, Illinois
  "Concurrent Error Detection in VLSI Systems through Structure Encoding"

- Jing-Yang Jou, August 1985 (CS), University of Illinois at Urbana-Champaign
  GTE Laboratories, Waltham, Massachusetts
  "Fault Tolerant Matrix Arithmetic and Signal Processing on Highly Concurrent VLSI Systems"

- Niraj K. Jha, August 1985 (EE), University of Illinois at Urbana-Champaign
  University of Michigan, Ann Arbor, Michigan
  "Totally Self-Checking Circuits and Testable CMOS Circuits"

- Hsi-Ching Shih, October 1986 (CS), University of Illinois at Urbana-Champaign
  Digital Equipment Corp., Hudson, MA
  "Fault Simulation and Transistor-Level Test Generation for Physical Failures in MOS Circuits"

- Gary M. Koob, January, 1987 (EE), University of Illinois at Urbana-Champaign
  Carnegie-Mellon University, Pittsburgh, PA
  "An Abstract Complexity Theory for Boolean Functions"

- William A. Rogers, January 1987 (EE), University of Illinois at Urbana-Champaign
  University of Texas, Austin, TX
  "The Use of Hierarchy in Test Generation, Fault Simulation and Testability Analysis Algorithms"

- Chien-Yi Roger Chen, May 1987 (EE), University of Illinois at Urbana-Champaign
  Texas Instruments, Inc., Dallas, TX
  "Design and Analysis of Fault-Tolerant Processor Arrays for Numerical Applications"

- Robert Fujii, May 1987 (EE), University of Illinois at Urbana-Champaign
  Purdue University, West Lafayette, IN
  "Issues in Design for Testability and Self-Test"

- Kien A. Hua, May 1987 (EE), University of Illinois at Urbana-Champaign
  IBM Corp., Kingston, NY
  "Design of Systems with Concurrent Error Detection Using Software Redundancy"

- Hongtao Chang, August 1987 (EE), University of Illinois at Urbana-Champaign
  IBM Corp., Endicott, NY
  "Use of High-Level Descriptions in Fault Simulation and Test Generation"

- Joseph T. Rahmeh, January 1988 (EE), University of Illinois at Urbana-Champaign
  University of Texas, Austin, TX,
  "Performance Modeling of Iterative Numerical Algorithms on Loosely Coupled Systems"

- Dhananjay S. Brahme, December 1988 (EE), University of Illinois at Urbana-Champaign
  Texas Instruments, Inc., Dallas, TX
  "Knowledge Based Testing of VLSI Circuits"

- Abhijit Chatterjee, December 1988 (EE), University of Illinois at Urbana-Champaign
  General Electric, Schenectady, NY
  "The Testability of Regular Logic Structures"

- Ram Kunda, May 1990 (EE), University of Illinois at Urbana-Champaign
  SUN Microsystems, Sunnyvale, CA
  "Use of Architectural-Level Primitives in System-Level Diagnosis and Speed Up of Test Vector Generation"

- Robert Mueller-Thuns, July 1990 (EE), University of Illinois at Urbana-Champaign
  Cadence, Inc., Waltham, MA
  "Parallel Processing for VLSI Simulation"

- V. S. Sukumaran Nair, July 1990 (EE), University of Illinois at Urbana-Champaign
  Southern Methodist University
  "Analysis and Design of Algorithm-Based Fault-Tolerant Systems"

- Marc E. Levitt, August 1990 (EE), University of Illinois at Urbana-Champaign
  SUN Microsystems, Sunnyvale, CA
  "Time-Based Strategies for Semiconductor Manufacture and Test"

- Kurt Thearling, August 1990 (EE), University of Illinois at Urbana-Champaign
  Thinking Machines, Cambridge, MA
  "Techniques for Automatic Test Knowledge Extraction from Compiled Circuits"

- Carol Gura, September 1990 (EE), University of Illinois at Urbana-Champaign
  IBM Corporation, Austin, TX
  "A Unified Approach for Assessing Circuit and Packaging Technologies in a System Environment"

- Kaushik Roy, September 1990 (EE), University of Illinois at Urbana-Champaign
  Texas Instruments, Dallas TX
  "Timing Verification and Synthesis of Circuits for Delay Fault Testability"

- David Blaauw, December 1991 (CS), University of Illinois at Urbana-Champaign
  IBM Corporation, Endicott, NY
  "Functional Abstraction in Switch-level Simulation"

- Rabindra K. Roy, February 1992 (EE) (with Dan Saab), University of Illinois at Urbana-Champaign
  NEC Research Laboratories, Princeton, NJ
  "Automatic Test Generation for Bit-Serial VLSI Digital Signal Processors"

- Prakash Narain, September 1992 (EE) (with Dan Saab), University of Illinois at Urbana-Champaign
  IBM Corporation, Kingston, NY
  "A High Level Approach to Test Generation for VLSI Circuits"

- Jawahar Jain, May 1993 (ECE) (with Don Fussell), University of Texas at Austin
  Fujitsu Laboratories of America, San Jose, CA
  "On Analysis of Boolean Functions"

- Hoon Chang, August 1993 (ECE), University of Texas at Austin
  Motorola, Inc., Austin, TX
  "Strategies for Design and Test of High Performance Systems"

- Chun-Hung Chen, August 1993 (ECE), University of Texas at Austin
  Consultant, San Jose, CA
  "A Multi-Level Hierarchical Sequential Circuit Test Generation Algorithm"

- Praveen Vishakantaiah, August 1993 (ECE), University of Texas at Austin
  Intel Corporation, Folsom, CA
  "ATKET: Automatic Extraction of Test Knowledge from VHDL Specifications"

- Ghani Kanawati, November 1993 (ECE), University of Texas at Austin
  Research Scientist, University of Texas, Austin, TX
  "Evaluation of System Dependability Properties Using Fault and Error Injection"

- Nasser Kanawati, November 1993 (ECE), University of Texas at Austin
  CompuShare, Detroit, MI
  "Fault-Tolerance in Object-Based Systems"

- John Moondanos, December 1993 (ECE), University of Texas at Austin
  Intel Corporation, Folsom, CA
  "Formal Verification Techniques Based on State Machine Comparison"

- Naveena Nagi, December 1994 (ECE), University of Texas at Austin
  LogicVision, Inc., San Jose, CA
  "A Comprehensive Test Framework for Analog and Mixed-Signal Circuits"

- Sankaran Karthik, May 1995 (ECE), University of Texas at Austin
  Intel Corporation, Folsom, CA
  "Distributed Mixed-Level Logic and Fault Simulation"

- Gopi Ganapathy, August 1995 (ECE), University of Texas at Austin
  Advanced Micro Devices, Austin, TX
  "Test Generation and Fault Simulation Technqiues for Full Custom ULSI"

- Yatin Hoskote, December 1995 (ECE), University of Texas at Austin
  Intel Corporation, Aloha, OR
  "Automated Techniques for Multilevel Verification of Sequential Circuits"

- Prakash Arunachalam, August 1996 (ECE), University of Texas at Austin
  Intel Corporation, Aloha, OR
  "A Distributed Mechanism for Large Memory Problems"

- Ashok Balivada, December 1996 (ECE), University of Texas at Austin
  Crystal Semiconductor, Austin, TX
  "Structured Test Generation Techniques for Analog and Mixed Signal Circuits"

- Rajarshi Mukherjee, May 1997 (ECE) (with Don Fussell), University of Texas at Austin
  Fujitsu Laboratories of America, San Jose, CA
  "Efficient Techniques for Verifying Combinational Circuits"

- Jin Chen, August 1998 (ECE), University of Texas at Austin
  Motorola, Inc., Austin, TX
  "Fault Modeling and Test Techniques for Analog and Mixed-signal Circuits"

- Konstantinos Moundanos, August 1998 (ECE), University of Texas at Austin
  Consultant, San Jose, CA
  "A Unified Validation Framework for VLSI CircuitsUsing Formal and Abstraction Techniques"

- Raghuram Tupuri, May 1999 (ECE), University of Texas at Austin
  Advanced Micro Devices, Austin, TX
  "Hierarchical Sequential Test Generation for Large Circuits"

- Jian Shen, May 1999 (ECE), University of Texas at Austin
  Cadence Design Systems, Austin, TX
  "Effective Techniques for Processor Validation and Test"

- Rathish Jayabharathi, August 1999 (ECE), University of Texas at Austin
  Intel Corporation, Folsom, CA
  "Hierarchical Timing Verification and Delay Fault Testing"

- Kyung Tek Lee, August 1999 (ECE), University of Texas at Austin
  IBM Corporation, Austin, TX
  "Crosstalk Fault Test Generation and Hierarchical Timing Verification in VLSI Digital Circuits"

- Chia-Pin Robin Liu, August 1999 (ECE), University of Texas at Austin
  Motorola, Inc., Austin, TX
  "Transistor Level Synthesis and Hierarchical Timing Analysis for CMOS Combinational Circuits"

- Richard Raimi, August 1999 (ECE), University of Texas at Austin
  Motorola, Inc., Austin, TX
  "Environment modeling and efficient state reachability checking"

- Nina Saxena, August 1999 (ECE), University of Texas at Austin
  IBM Corporation, Austin, TX
  "Scalable Solutions to Verification and Specification of Large Designs"

- Jayanta Bhadra, June 2001 (ECE), University of Texas at Austin
  Motorola, Inc., Austin, TX
  "Abstraction Techniques for Verification of Digital Designs"

- Jeongjin Roh, June 2001 (ECE), University of Texas at Austin
  Intel Corporation, Austin, TX
  "Mixed-Signal Signature Analysis for System-On-a-Chip"

- Jason Baumgartner, December 2002 (ECE), University of Texas at Austin
  IBM Corporation, Austin, TX
  "Automatic Structural Abstraction Techniques for Enhanced Verification"

- Sungbae Hwang, December 2002 (ECE), University of Texas at Austin
  National Semiconductor Corporation, Santa Clara, CA
  "System-on-a-Chip Testing Using an Embedded Microprocessor"

- Vivek Vedula, March 2003 (ECE), University of Texas at Austin
  Intel Corporation, Austin, TX
  "Program Slicing for Accelerating Sequential ATPG: Applications to Test Generation and Verification"

- Kyoil Kim, August 2003 (ECE), University of Texas at Austin
  Dongyang Technical College, South Korea
  "Verification Methods for Secure Protocols"

- Arun Krishnamachary, December 2003 (ECE) University of Texas at Austin
  Intel Corporation, Chandler, AZ
  "Test Generation for Realistic Defects"

- Narayanan Krishnamurthy, December 2003, University of Texas at Austin
  Motorola Corporation, Austin, TX
  "A design validation methodology for high performance microprocessors"

- Jianhua Gan, December 2003 (ECE), University of Texas at Austin
  Cirrus Logic Corporation, Austin, TX
  "Non-Binary Capacitor Array Calibration for a High Performance Successive Approximation A/D Converter"

- Hak-Soo Yu, August 2004 (ECE), University of Texas at Austin
  Samsung Corporation, Seoul, Korea
  "BIST-based performance characterization of mixed-signal circuits"

- Jing Zheng, May 2005 (ECE), University of Texas at Austin
  Freescale Corporation, Austin, TX
  "Improving Timing Verification and Delay Testing Methodologies for IC Designs"

- Robert Sumners, August 2005 (ECE), University of Texas at Austin
  AMD, Austin, TX
  "Deductive mechanical verification of concurrent systems"

- Hongjoong Shin, December 2006 (ECE), University of Texas at Austin
  Texas Instruments, Austin, TX
  "Built-in Performance Characterization of Embedded Mixed-Signal Circuits"

- Ramayanshu Datta, December 2006 (ECE), University of Texas at Austin
  Texas Instruments, Dallas, TX
  "Parametric Testing, Characterization and Reliability of Integrated Circuits"

- Byoung-Ho Kim, December 2007 (ECE), University of Texas at Austin
  National Semiconductor, Santa Clara, CA
  "Predicting Mixed-Signal Dynamic Performance Using Optimized Signature-Based Alternate Test"

- Shobha Vasudevan, December 2007 (ECE), University of Texas at Austin
  University of Illinois at Urbana-Champaign, Urbana, IL
  "High Level Static Analysis of System Descriptions for Taming Verification Complexity"

- Sankar Gurumurthy, May 2008 (ECE), University of Texas at Austin
  AMD, Austin, TX
  "Automatic Generation of Instruction Sequences for Software-Based Self-Test of Processors and Systems-on-a-Chip"

- Baker Mohammad, August 2008 (ECE), University of Texas at Austin
  Qualcomm Corporation, Austin, TX
  "Cache Design for Low Power and Yield Enhancement"

- Qingqi Dou, August 2008 (ECE), University of Texas at Austin
  Broadcom Corporation, Irvine, CA
  "I/O Test Methods in High-speed Wireline Communication Systems"

MAJOR RESEARCH CONTRACTS:

- "Reliable, High Performance VHSIC Systems," DoD VHSIC Program, 1980–1984.

- "Reliable VLSI Architectures," Semiconductor Research Corporation, 1983–1988.

- "Recovery Techniques for Real-Time Electronics Systems," ONR, 1989–1991.

- "Test Generation for Very Large Scale Integrated Circuits Using Genetic Learning", Texas Advanced Research Program, 1989–1991.

- "The Design of Testable Systems," Semiconductor Research Corporation, 1989–1994.

- "Investigation of Fault Injection Techniques," U. S. Air Force (through Computer Sciences Corporation), 1992–1993.

- "Novel Techniques for Design Verification and Verification-Based Test," Semiconductor Research Corporation, 1992–1994.

- "Fault Modeling and Test Generation for Mixed-Signal Integrated Circuits," National Science Foundation, 1992–1995.

- "Multilevel Verification and Testing of VHDL Designs", Semiconductor Research Corporation, 1993–1994.
- "A Flexible Software-Based Fault Injection System," Naval Air Warfare Center, 1993–1997.
- "Software Tools for Automated Formal Verification and Verification-Based Test," Texas Advanced Technology Program Development, 1994–1996.
- "Integrated Approaches to Test and Verification," Semiconductor Research Corporation, 1994–1998.
- "Self-Test Techniques for Complex Processors," Texas Advanced Technology Program, 1996–1997.
- "Redundant Low Cost Solid-State Inertial Reference System with GPS Aiding for General Aviation," NASA STTR (through Vision Micro Devices, Inc.), 1996–1999.
- "Test Automation Tools and Research," U. S. Air Force, Rome Air Development Center (through LogicVision Software, Inc.), 1996–1997.
- "Application of Learning Techniques to Combinational Verification," Fujitsu Laboratories of America, 1997–1998.
- "Native-Mode Self Test for Processors," Intel Corporation, 1997–1998.
- "Software Tool for On-Chip Native Mode Built-In Tests and Test Structures," Texas Advanced Technology Program Development, 1998–1999.
- "Hierarchical Testability Analysis and Design Verification for Analog and Mixed-Signal Systems," National Science Foundation, 1998–2001.
- "Low Cost Self-Test Techniques for Systems on a Chip," Semiconductor Research Corporation, 1999-2002.
- "High Level Generation and Testability Techniques for Realistic Defects," Semiconductor Research Corporation, 1999-2003.
- "Analog and Mixed-Signal Test Techniques," Gigascale Silicon Research Center (MARCO), 2001-2006.
- "Built-In Test of High-Speed/RF Mixed-Signal Electronics," National Science Foundation (Medium ITR Grant), 2003-2006.
- "Built-Off Self Test," Samsung Corporation, 2007-2009.
- "Test Generation for Post-Silicon Validation," Intel Corporation, 2007-2009.

PROFESSIONAL SOCIETIES

- Member of IEEE, 1971 - present
- Member of ACM, 1974 - present
- International Federation for Information Processing, Member of Working Group 10.4 - Reliable Computing and Fault Tolerance, 1980 - present

PROFESSIONAL SOCIETY AND MAJOR GOVERNMENT COMMITTEES:

- Technical Program Committee, International Symposium on Fault-Tolerant Computing, 1979, 1985, 1986, 1987, 1990, 1993, 1996–1999.
- Organizer and chair of session on "Fault Tolerant and Maintainable Systems," National Computer Conference, New York, New York, June l979.

- Program Chairman, Eleventh International Symposium on Fault-Tolerant Computing, Portland, Maine, 1981.
- Keynote Speaker, 1982 Bell System Conference on Electronic Testing, Princeton, New Jersey, October 5-7, 1982.
- Technical Program Committee, IEEE International Conference on Computer-Aided Design, Santa Clara, California, 1983, 1985, 1986, 1987.
- Tutorial Session Chair, IEEE International Conference on Computer-Aided Design, Santa Clara, California, November 1988.
- Technical Program Committee, IEEE Workshop on Design for Testability, Vail, Colorado, 1984-1992. April 1988.
- Associate Editor, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1984-1986.
- Lecturer, Societe pour la Diffusion de l'Innovation (DINOV) Seminar Series, Toulouse, France, June 1986.
- Panel Organizer and Chair, 1986 IEEE International Conference on Computer Design, Rye Brook, New York, October 1986.
- Member, National Science Foundation Advisory Committee for Microelectronic Information Processing Systems, 1987-1989.
- Technical Program Committee, 3rd International Conference on Data Engineering, Los Angeles, California, February 1987.
- Technical Program Committee, International Conference on VLSI Design, 1994–.
- Technical Program Committee, IEEE VLSI Test Symposium, 1995–.
- Technical Program Committee, Int'l Mixed-Signals Testing Workshop, 1995–.
- Lecturer, NATO Advanced Study Institute on Testing and Diagnosis of VLSI and ULSI, Como, Italy, June 1987.
- Member, Executive Committee, 1988 IEEE International Conference on Computer-Aided Design, Santa Clara, California, November 1988.
- General Co-Chair, International Symposium on Fault-Tolerant Computing, 1989.
- Program Committee, IFIP Working Conference on Dependable Computing for Critical Applications, 1991, 1992.
- Chair, IEEE Computer Society Technical Committee on Fault-Tolerant Computing, 1992–1993.
- Advisory Committee, IEEE Computer Society Technical Committee on Fault-Tolerant Computing, 1991–.
- Vice Chair, IFIP Working Group 10.4 on Dependable Computing and Fault Tolerance, 1996–1997.
- Associate Editor, IEEE Transactions on VLSI Systems, 1992.
- Associate Editor, Journal of Electronic Testing: Theory and Applications, 1994–present.
- Program Chair, IEEE International Conference on Computer Design, 1996.
- General Chair, IEEE International Conference on Computer Design, 1997.
- Program Chair, IEEE International On-Line Testing Symposium, 1998.

- Associate Editor, IEEE Transactions on Secure and Dependable Computing, 2004–present.

MAJOR CONSULTING: Aerospace Corp., DEC, Defense Nuclear Agency, ESL, GE, GM, GRC, GTE, H-P, IBM, Intel, Level One, National, Sperry, Tektronix

Consulting tasks for industry and government (held *Secret* clearance) included the following.

- Developed functional test techniques for microprocessors
- Developed designs for processors and memories to tolerate single-event upsets due to radiation
- Developed system-level fault tolerance techniques for application-specific processors
- Served on select advisory team to define fault tolerance requirements and validation procedures for fault-tolerant systems being built for U.S. Air Force and U.S. Navy
- Evaluated fault tolerance capabilities of proposed contractor designs for U.S. Air Force and U.S. Navy
- Developed design-for-test and built-in self test techniques for integrated circuits
- Evaluated test features of processors for military applications
- Developed verification techniques for complex designs
- Developed techniques and tools for converting legacy circuits to new technologies

SHORT COURSES TAUGHT AT: AMD, DEC, IBM, Motorola, Intel

- Taught short courses in testing, fault tolerance and verification

SUMMARY OF RESEARCH CONTRIBUTIONS:

- **Fault-Tolerant Computing**
  - *Reliability Evaluation:* Techniques for evaluating the reliability of TMR systems (part of Ph.D. dissertation), general networks (heavily cited) and hierarchical systems using a numerical technique to solve hierarchical Markov chains.
  - *Algorithm-Based Fault Tolerance:* Formulated this novel technique for low-cost fault tolerance which uses information about the computation being performed to detect and correct errors due to faults. Developed techniques for a variety of computations and structures, as well as the underlying theory for the types of redundancy techniques to be used. The idea has been picked up by many researchers, the results are heavily cited, and there have been sessions devoted to this topic in the recent international symposia on Fault-Tolerant Computing.
  - *Software-based fault injection:* Developed a general software-based fault injection system, FERRARI, useful for evaluating the fault tolerance properties of a system. Hardware faults within a processor can be emulated accurately in software, and faults can be injected into object code. The ideas have been adopted by other research groups in this country and Europe. An extension to real-time systems, FIESTA, has been used to evaluate a prototype fault-tolerant control system for the U.S. Navy, running on an embedded processor under a commercial operating system.
- **Automatic Test Generation and Design for Test**
  - *Memory Testing:* First to develop systematic functional fault models for memories, and to show that "coupling" faults between arbitrary memory cells could be detected by an $O(n)$ algorithm (industry practice at the time was to use an $O(n^2)$ algorithm). This paper has been widely used as the basis of further research work as well as test implementation in industry. Results appear in textbooks on the subject.
  - *Microprocessor Testing:* First to formulate higher level, functional fault models for processors, and to develop general algorithms for generating tests for microprocessors. Papers have been heavily cited, the techniques appear in textbooks in digital testing, and the ideas have been used by researchers and in industry.
  - *Fault Modeling:* Systematic development of fault models at various levels; showed the mapping of faults at the transistor level to logic and higher-level faults.
  - *Hierarchical Fault Simulation:* Showed that exploiting the hierarchy in the circuit design can reduce the complexity of fault simulation to $O(n.\log n)$ from $O(n^2)$. These ideas led to the implementation of a switch level fault simulator which is able to fault grade commercial microprocessors at the gate and switch levels on an engineering workstation, which has been extended by industry to fault simulate memory chips. Ideas from this research and work on distributed simulation were incorporated in a tool by Intel Corporation, and used to fault grade tests for the Pentium Pro processor on a network of workstations.
  - *Design of Testable Circuits:* Novel techniques at the logic and layout levels for making circuits easier to test, and a general theory of generating very compact tests for regular structures such as array multipliers. The technique of "Selective Pseudo-Scan" won a best paper award at the IEEE/ACM Design Automation Conference, and it has been used in very large custom processors with excellent results. Developed new on-chip sensors for determining parameters of high-speed RF circuits using low-cost test equipment, and fabricated chips to evaluate their benefits.
  - *Use of Genetic Algorithms for Test Generation:* Showed that use of genetic algorithms with clever heuristics can be used to generate high quality tests for very large sequential circuits. The ideas have been picked up by several other research groups over the world, and are being applied to custom processors.
  - *Hierarchical Test Generation:* Developed a novel hierarchical test generation method which has demonstrated spectacular results for large designs. The method targets one embedded module and automatically extracts functional constraints on the module under test. The embedded module

along with its constraints is given to a commercial sequential ATPG tool and the module level vectors are translated to chip level functional vectors. Results show that sequential ATPG time is reduced by two orders of magnitude and, simultaneously, the number of undetected faults is by an order of magnitude over conventional test generation.

- *"Native-Mode" Self Test of Processor Chips:* Developed the technique of native-mode test for processors, in which test programs are executed at internal chip speeds from the processor cache to detect manufacturing defects. This technique has been incorporated into the *FRITS* system at Intel Corporation, and shown to detect subtle failures in Pentium and Itanium chips.
- *Testing of Analog and Mixed-Signal Systems:* Was one of the first to develop structural test techniques for analog circuits. Developed techniques for using embedded processors in a System-on-a-Chip to test the A/D and D/A cores in a system. Showed that low-cost oscillation-based tests can be used to extract performance parameters of analog circuits. Developed new methods of testing analog blocks on a chip using an embedded digital core. Used novel on-chip sensor to allow low-cost test of RF performance parameters, and evaluated the technique through a GSM transceiver front-end implemented in Silicon.

- **Formal Verification**
  - *Probabilistic Verification:* Developed the novel idea of "probabilistic verification" which verifies Boolean functions by encoding them into an integer hash code.
  - *Sequential Equivalence Checking:* Developed a general package for checking the equivalence of sequential circuits between RTL and gate level. Developed techniques for verifying sequential equivalence between SystemC and Verilog.
  - *Property Checking Using Abstractions:* Proposed the idea of writing properties to be verified in a hardware description language, making it easy for designers to specify them. Developed powerful abstractions to contain the state space explosion when verifying large designs. Have applied the techniques to verify circuits larger than possible by any other packages from university or industry.

- **Design of Low Power and High Speed Circuits**
  - *Design of Low Power Circuits:* Developed techinique for annotating microprocessor descriptions at the Register Transfer Level (RTL) in order to achieve lower power dissipation. Developed very low-power sub-threshold circuits and evaluated them in Silicon.
  - *Design of High-Performance Signal Processing Circuits:* Designed very high speed functions (such as multipliers and FFT modules) for high data rate wireless systems.

PUBLICATIONS:

A. Refereed Archival Journal Publications

[A.1] J. A. Abraham and D. P. Siewiorek, "An Algorithm for the Accurate Reliability Evaluation of Triple-Modular Redundancy Networks," *IEEE Transactions on Computers*, vol. C-23, no. 7, July 1974, pp. 682–692.

[A.2] J. A. Abraham, "A Combinatorial Solution to the Reliability of Interwoven Redundant Logic Networks," *IEEE Transactions on Computers*, vol. C-24, no. 5, May 1975, pp. 578–584.

[A.3] R. Nair, S. M. Thatte and J. A. Abraham, "Efficient Algorithms for Testing Semiconductor Random Access Memories," *IEEE Transactions on Computers*, vol. C-27, no. 6, June 1978, pp. 572–576.

[A.4] J. A. Abraham, "An Improved Algorithm for Network Reliability," *IEEE Transactions on Reliability*, vol. R-28, April 1979, pp. 58–61.

[A.5] T. C.-K. Chou and J. A. Abraham, "Performance/Availability Modeling of Shared-Resource Multiprocessors," *IEEE Transactions on Reliability*, vol. R-29, April 1980, pp. 70–74.

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