VLSI Design, Fall 2020

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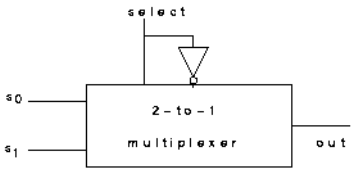
Homework No. 1

Assigned September 3, 2020, due September 10, 2020

1. This problem relates to the design of circuits using multiplexer modules. A 2-to-1 multiplexer module is shown below (the transistor circuit for this was discussed in class). Three of these modules can be combined to produce a 4-to-1 multiplexer. Any 2-input logic function can be implemented using this 4-to-1 multiplexer with the two inputs fed to the select line and the truth table entries appropriately fed to the input lines. However, a 4-to-1 multiplexer can also implement a 3-input logic function if the complement of one of the inputs is also available. Can you figure this out?



select	out
0	s_0
1	s_1

a	b	c	z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Figure 1: Function to be implemented

(a) Implement the logic function in Figure 1 using three of the 2-to-1 multiplexer modules.

(b) Design a gate-level implementation of the above function using multiplexer modules made of NAND/NOR gates. You don't have to draw all the gates explicitly; show the implementation of a module, and use it as a "black box" for the implementation.

(c) How many transistors are needed for the gate level implementation?

(d) If the same function is implemented using multiplexers with transmission gates, what would be the number of transistors needed for this implementation?

2. Draw the transistor schematic representing the circuit below. Can you describe the function of the circuit?

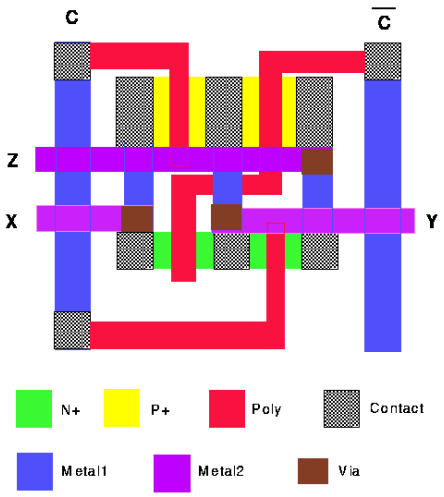


Figure 2: Layout of circuit

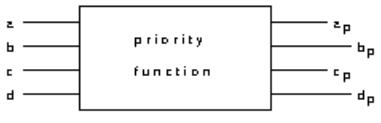
Is this cell easy to "tile" in the vertical direction? The horizontal direction? Explain.

3. This problem relates to the design of priority functions in CMOS. The 4-input priority function is described below:

(a) Design a gate-level implementation of the 4-input priority function. You don't need to explicitly draw all the gates; provide enough of the design so that someone could see how the complete design can be done.

(b) Design the transistor level implementation of the above function. Again, you don't have to draw all the transistors explicitly.

The above implementation cannot be readily expanded in a natural way to implement a function with more inputs.
Another solution to the realization of the priority function for N inputs would be to repeat a single variable cell N times. Appropriate information is transmitted between cells as shown in the figure below:



a	b	c	d	a_p	b_p	c_p	d_p
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	x	0	0	1	0
0	1	x	x	0	1	0	0
1	x	x	x	1	0	0	0

Figure 3: Priority function

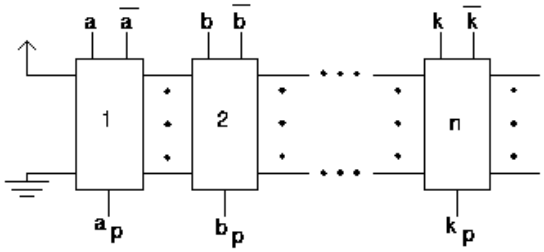


Figure 4: Iterative logic array implementation of priority function

(c) Design a cell in CMOS technology at the transistor level which, when repeated as above, implements the priority function.

4. What is the function, F implemented by the circuit in Figure 5?

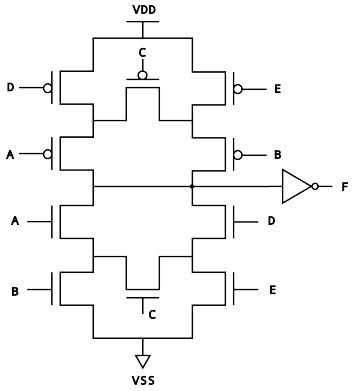


Figure 5: CMOS circuit

5. Problem 1.1 from the exercises for Chapter 1 in the book (page 57). Comment on the prediction.