VLSI Design, Fall 2020

J. A. Abraham

Homework No. 3

Assigned September 17, 2020, due September 24, 2020

1. Size the gates in Figure 1 so that it has the same drive strength as an inverter that has a pMOS transistor of width 3 and an nMOS transistor of width 2.

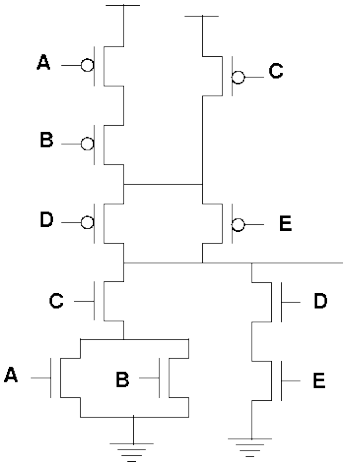

Figure 1: Transistor sizing

2. Problem 2.15 from the Exercises for Chapter 2 (page 97).

3. Use the Elmore delay approximation to find the *worst-case* rise and fall delays at the output for Figure 2. The gate sizes of the transistors are given in the figure. Use the assumption that the diffusion capacitance is equal to the gate capacitance, and that a minimum sized transistor has gate and diffusion capacitance equal to C. The resistance of an nMOS transistor with unit width is R and the resistance of a pMOS transistor with width 2 is also R. Also assume NO sharing of diffusion regions. (Hint: off-path capacitances can contribute to delay.)

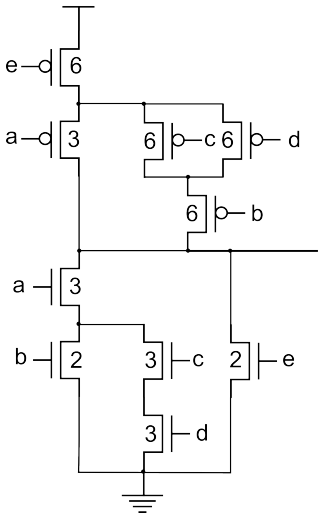

Figure 2: Complex gate

4. Problem 4.4 from the Exercises for Chapter 4 (page 177).

5. Find the logical efforts for the inputs, a, b, c, d and e in Figure 2.

6. (a) A ring oscillator consisting of 15 minimum-sized (2:1) inverters in a loop, placed on a 45nm chip, has a measured frequency of 6.41 GHz. What is the delay of one stage of the oscillator?

(b) If the ring oscillator performance is assumed to be representative of the performance of the transistors on the chip, what would be the FO4 delay for the inverters in this particular chip?

7. Problem 4.13 from the Exercises for Chapter 4 (page 178).
(Hint: Try a design with 4 stages; 2-bit XNOR gates to check for bitwise equality, a 16-input AND function to check equality of the input words (using 4-input gates, for example), and an AND gate to choose between Y or 0).

8. Problem 4.15 from the Exercises for Chapter 4 (page 178).

9. Problem 4.24 from the Exercises for Chapter 4 (page 179).

10.(a) Calculate the delay of the path G1-G2-G3-G4-G5 in the 2-input Exclusive-OR circuit (with input buffers) in Figure 3, using logical effort. Also give the sizes of the P and N transistors to achieve this delay. You may assume that the off-path capacitance is the same as the on-path capacitance for each branch. Input capacitance of inverter G1 = 3 units, and load capacitance driven by Gate G5 = 25 units.

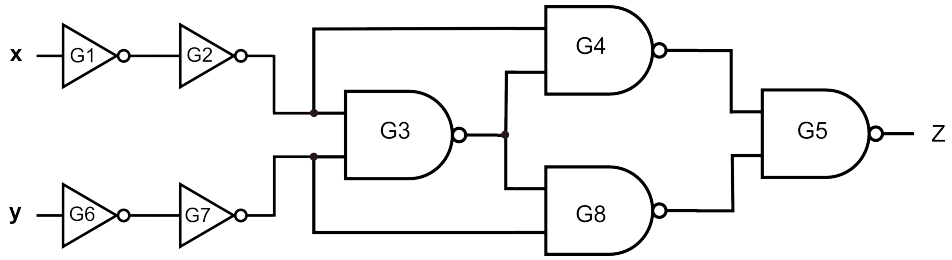

Figure 3: Sizing path

(b) The assumption that off-path capacitance is the same as the on-path capacitance for each branch is probably true for the branch at the output of G3 (assuming the symmetric path is sized similarly), but probably not correct for the branch at the output of G2 (or G7, if that path is being sized). Suggest some way of improving the result above.

11. Problem 9.10 from the Exercises for Chapter 9 (page 371).

12. Problem 9.12 from the Exercises for Chapter 9 (page 371).