VLSI Design, Fall 2020

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Homework No. 6

Assigned October 27, 2020, due November 5, 2020

1. Problem 12.1 from the Exercises for Chapter 12 (page 546).

2. Problem 12.2 from the Exercises for Chapter 12 (page 546).

3. This problem is to design a fast **addition circuit (+)** to add a 32-bit number with a 4-bit number (to produce a 33-bit number). The circuit should be designed with two macros (shown below): an adder macro (adds numbers of a specified bit-width) which produces an adder with a delay of 100 pS/bit, and a multiplexer (which selects from inputs of specified bit width) which has a delay of 100 pS (independent of the size). The arrival times of the input signals to the circuit are also shown below.

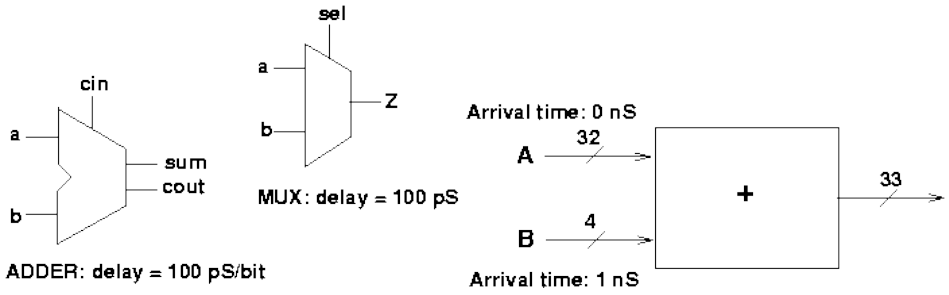

Figure 1: DSP Adder

Design the circuits for the following specifications, and show the interconnection of the modules below to meet the specs. Make sure that you show the appropriate bits for the inputs to the modules. (You may not need to use all the modules for a solution, or you may need to add additional modules. Do NOT add any other logic other than the two modules.)

(a) Design a circuit to complete the addition in ≤ 3 nS

(b) Design a circuit to complete the addition in ≤ 2 nS.

4. Suppose you are given an input pattern that contains SEVEN numbers ranging from 0 to 3, and each number from 0 to 3 occupies exactly two positions in the input pattern, except one number which only occupies one position. Design the logic to detect this number (i.e., the output should match the single number on the input). The basic cells are 2-input NAND, 2-input NOR, and Inverter. You can design any cell based on the basic cells and use it in your design (in the same way as in lab 2). Assume that the inputs and output are expressed as 2-bit unsigned numbers, the top bit is the most significant bit, and the bottom bit is the least significant bit.