2. Transistors, Fabrication, Layout

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VLSI Design
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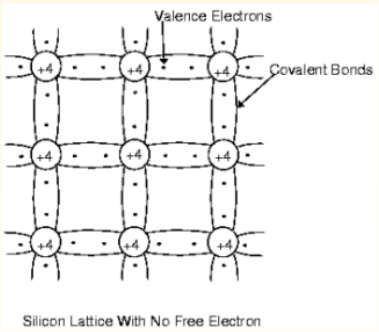
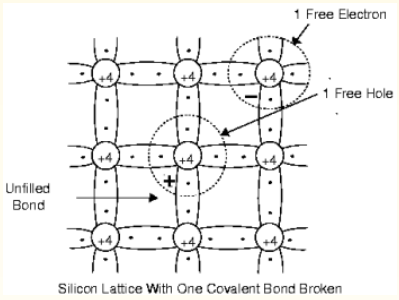
Conductivity in Silicon Lattice

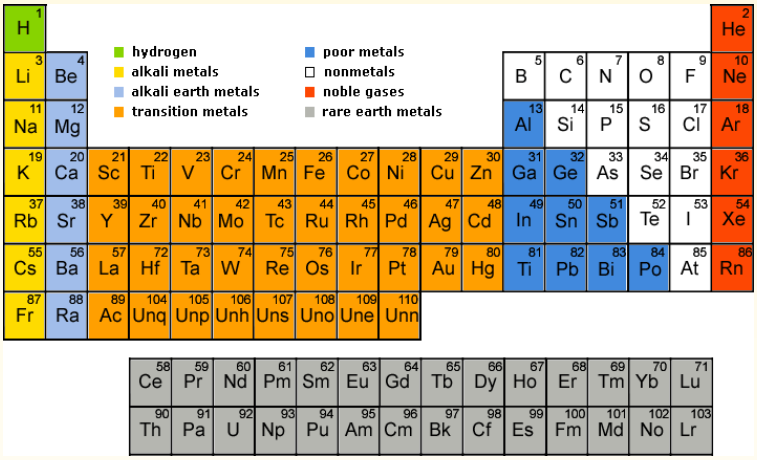
Look at the behavior of crystalline silicon

- At temperatures close to 0 K, electrons in outermost shell tightly bound (insulator)
- At higher temps., (300 K), some electrons have thermal energy to break covalent bonds





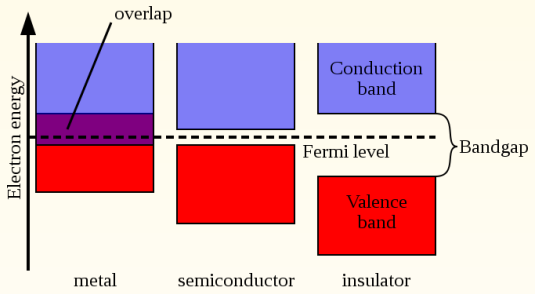
The Elements (Periodic Table)



Build Systems with Information on Electrical Characteristics of Building Blocks (Transistors)

This course will not cover semiconductor physics

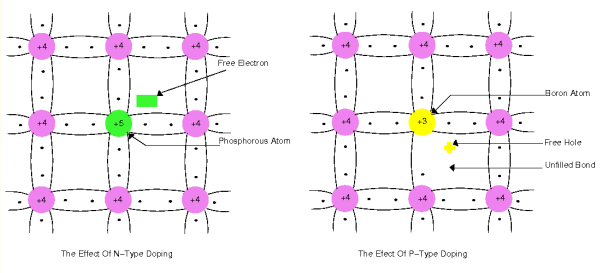
- Learn this from other courses in the department
- We will design VLSI circuits knowing the electrical behavior of the transistors



Dopants

Used to selectively change the conductivity of silicon

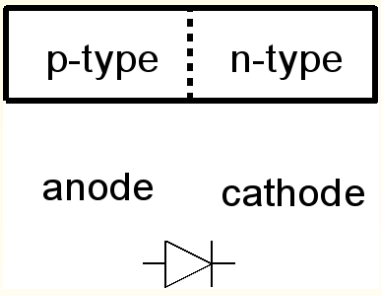
- Silicon is a semiconductor
- Pure silicon has no free carriers and conducts poorly
- Adding dopants **impurities** to pure silicon increases the conductivity
- Group V: extra electron (n-type)
- Group III: missing electron, called hole (p-type)



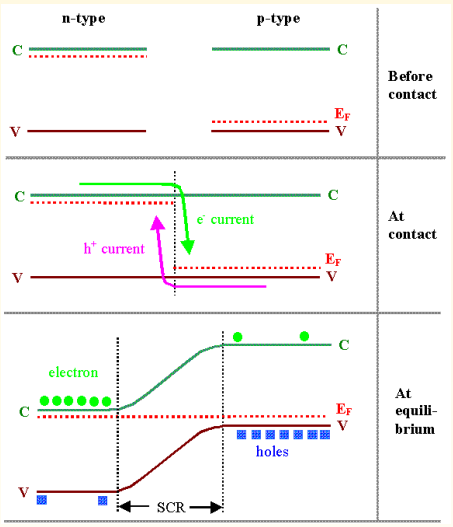
p-n Junctions

Diodes

- A junction between p-type and n-type semiconductor forms a diode
- Current flows only in one direction



p-n Junction, Cont'd

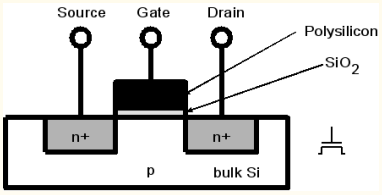


Source: Prof. Dr. Helmut Föll, University of Kiel

nMOS Transistor

Four-Terminal device: gate, source, drain, body

- Gate oxide body stack looks like a capacitor
- Gate and body are conductors
- SiO_2 (oxide) is a very good insulator
- Called metal oxide semiconductor (MOS) capacitor, even though gate material changed to polysilicon
- Recent gate material in nanoscale processes is back to metal



nMOS Transistor Operation

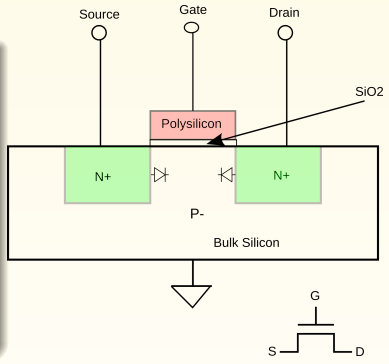
Body (bulk) is commonly tied to Ground (0 V)

When the gate is at a low voltage

- P-type body is at low voltage
- Source-body and drain-body diodes are OFF
- No current flows, transistor is OFF

When the gate is at a high voltage

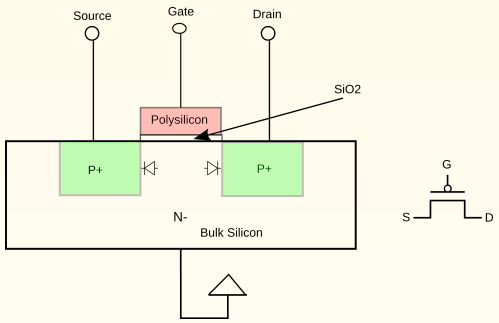
- Positive charge on gate of MOS capacitor
- Negative charge attracted to body
- Inverts a channel under gate to n-type
- Now electrons can flow through n-type silicon from source through channel to drain, transistor is ON



pMOS Transistor

Similar to nMOS transistor, but doping and voltages reversed

- Body tied to high voltage (VDD)
- Gate low: transistor ON
- Gate high: transistor OFF
- Bubble indicates inverted behavior



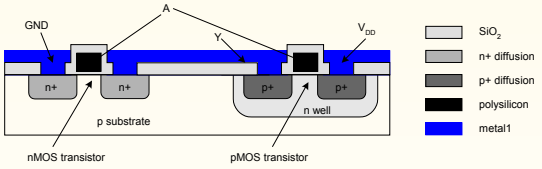
CMOS Fabrication

Silicon technology

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

Example inverter cross-section

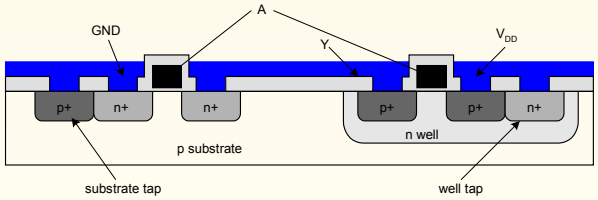
- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



Well and Substrate Taps

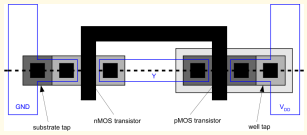
Substrate contacts are critical to correct operation of CMOS

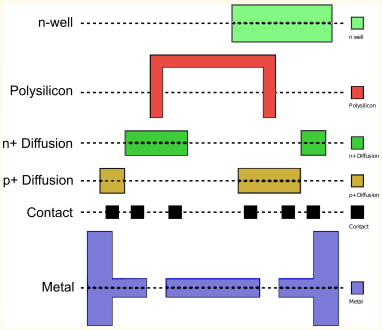
- Substrate must be tied to GND, n-well to VDD (reverse-biased diodes isolate regions)
- Metal to lightly-doped semiconductor forms poor connection called Schottky Diode – use heavily doped well and substrate contacts/taps



Inverter Masks

- Transistors and wires are defined by **masks**
- Cross-sections shown above taken along dashed line





Examples of Fabrication Steps

A VERY simplified description illustrating the major step – modern processes follow these basic steps, but are much more complex

- Start with blank wafer
- Build inverter from the bottom up

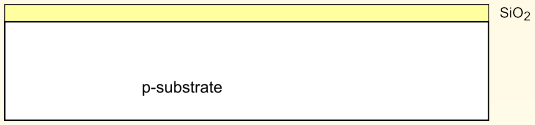
First step is to form the n-well

- Cover wafer with protective layer of SiO_2 (oxide)
- Remove layer where n-well should be built
- Implant or diffuse n dopants into exposed wafer
- Strip off SiO_2

Oxidation and Photoresist

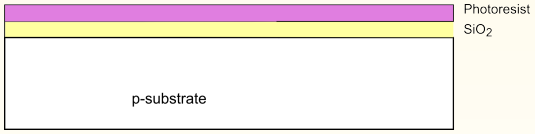
Grow SiO_2 on top of Si wafer

- 900 $--$ 1200°C with H_2O or O_2 in oxidation furnace



Spin-on photoresist

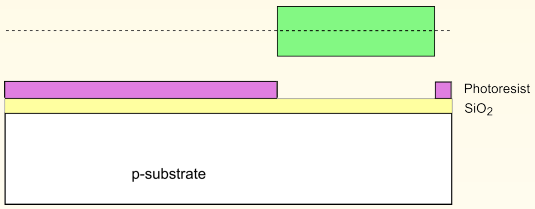
- Photoresist is a light-sensitive organic polymer which softens where exposed to light (positive resist)



Lithography

Use light to transfer a pattern to the wafer

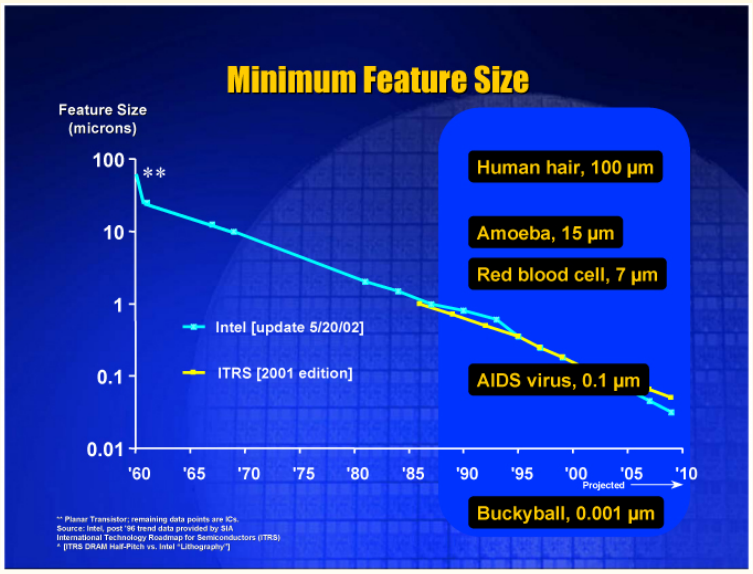
- Expose photoresist through n-well mask (using UV light – example 193 nm wavelength)
  - "Immersion lithography" used in some nanoscale processes
- Strip off exposed photoresist



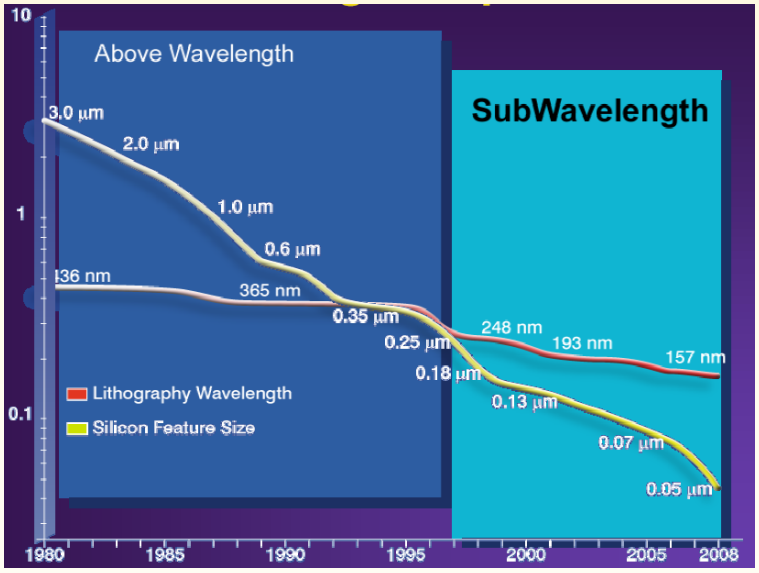
Interesting physics problem

- How can we "print" a 45 nm feature using light with a wavelength of 193 nm?
- Significant distortion of the image!

Trend in Integrated Circuit Feature Sizes

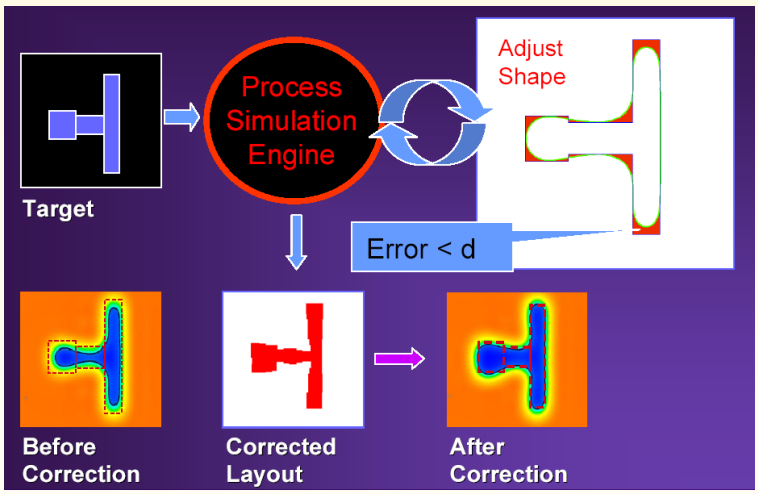


Features Smaller than Wavelength of Light Used



Optical Proximity Correction (OPC)

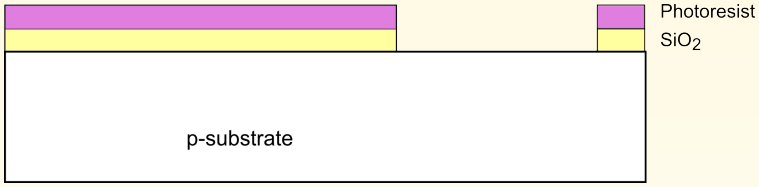
What you see is NOT what you get



Etch and Strip Photoresist

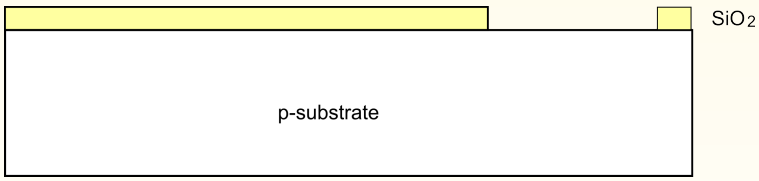
Etch oxide with Hydrofluoric acid (HF)

- Only attacks oxide where resist has been exposed



Strip remaining photoresist using mixture of acids ("piranha" etch)

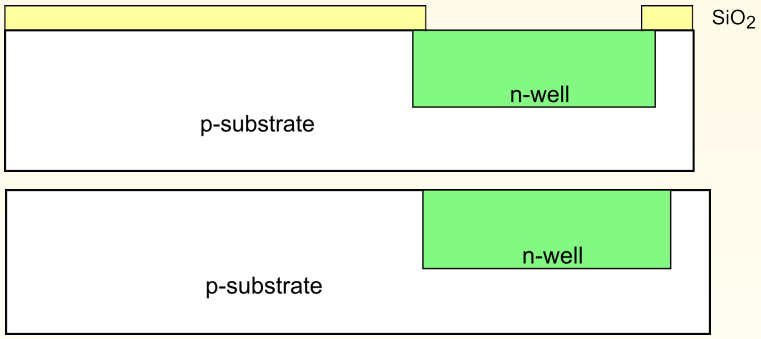
- Necessary so resist does not melt in the next step



n-Well

Formed using ion implant (used to be diffusion)

- Bombard wafer with As ions, which only enter exposed Si
- (With diffusion, wafer is placed in a furnace with As gas)
- Remaining oxide is then stripped off using HF, and it is back to the bare wafer, but with an n-well



Subsequent steps repeat the above process

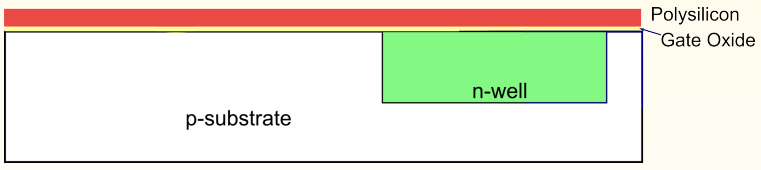
Polysilicon (Modern Processes use Metal Gates)

Very thin layer of gate oxide is grown on wafer

- Gate oxide thickness is < 20Å (few atomic layers)
- One of the most critical steps in fabrication process

Polysilicon deposited on top of gate oxide

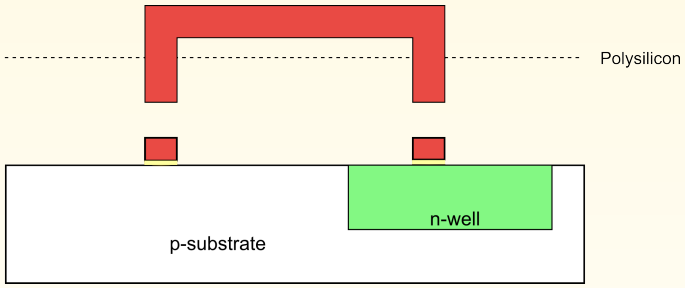
- Grown using Chemical vapor deposition (CVD)
- Wafer placed in furnace with Silane (SiH) gas
- Small crystals (polysilicon) formed on wafer
- Heavily doped to be a good conductor



Polysilicon Patterning

Use same lithography processing to pattern polysilicon

- Reactive Ion Etch (RIE) process
- Charge buildup on un-etched polysilicon can lead to "antenna effects" and damage gate oxide



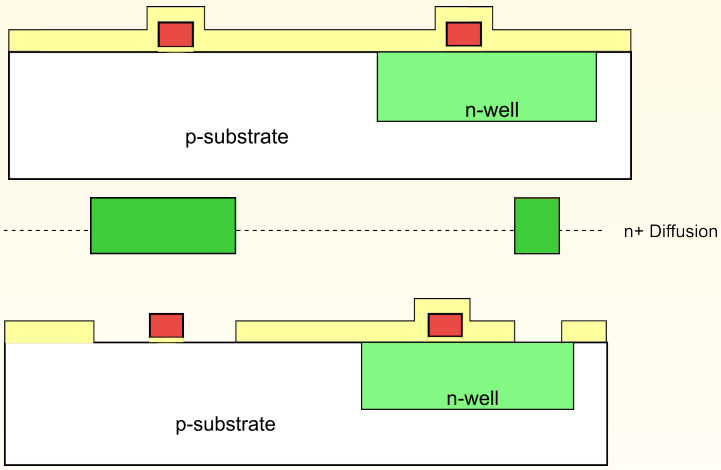
Self-aligned process

- Polysilicon "blocks" dopants where the channel should be formed

N+ Diffusion

nMOS transistors are formed

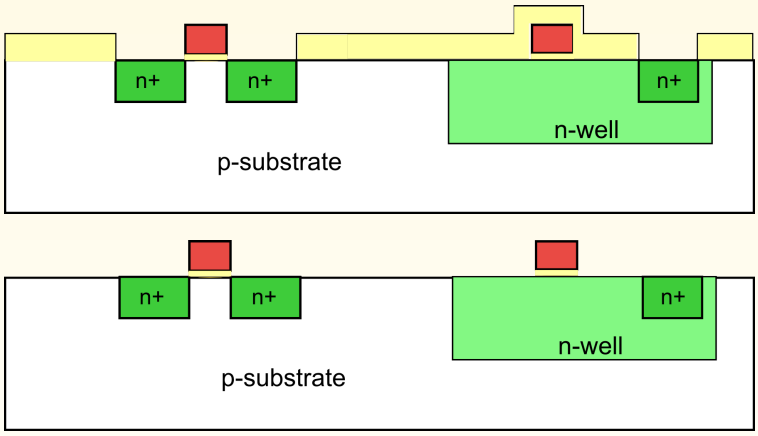
- Oxide is patterned to form the n+ regions
- N+ diffusion forms nMOS source, drain, and n-well contact



N+ Diffusion, Cont'd

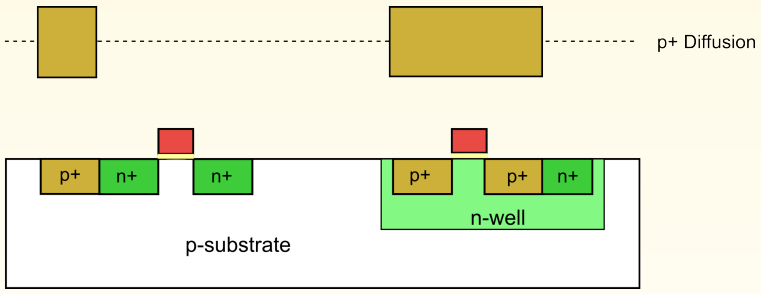
Ion implantation used to dope silicon

- n+ regions are formed
- Oxide is stripped off to complete patterning step



P+ Diffusion

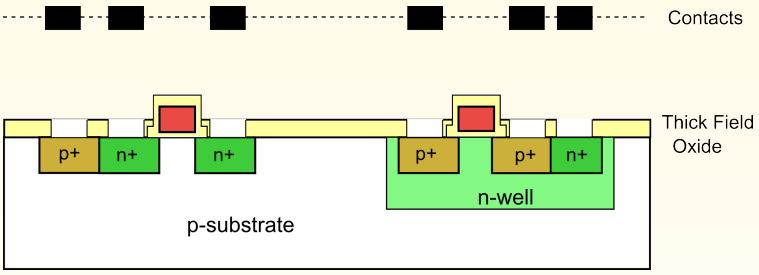
A similar set of steps is used to form the p+ diffusion regions for the pMOS transistor source and drain as well as the substrate contact



Contacts

Points where the first level of metal contacts the transistors

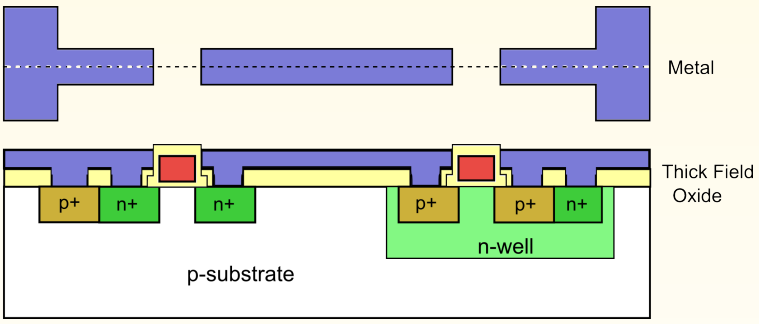
- Used to wire the devices together
- Wafer is covered with thick field oxide
- Oxide is etched where the contact cuts are needed



Metallization

Used to interconnect internal nodes

- Aluminum was the traditional metal
  - Switch to Copper for high performance processes
- Aluminum is sputtered over the entire wafer
- Patterned to remove excess metal, leaving the wires



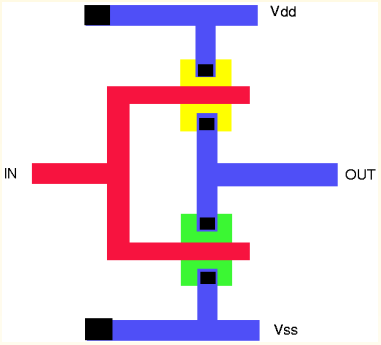
Layout

- Describes actual layers and geometry on the silicon substrate to implement a function
- Need to define transistors, interconnection
  - Transistor widths (for performance)
  - Spacing, interconnect widths, to reduce defects, satisfy power requirements
  - Contacts (between poly or active and metal), and vias (between metal layers)
  - Wells and their contacts (to power or ground)
- Layout of lower-level cells constrained by higher-level requirements: **floorplanning**
  - "design iteration"

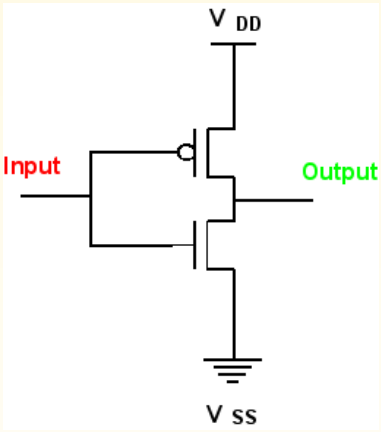
Layout, Cont'd

- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size f = distance between source and drain
  - Set by minimum width of polysilicon (= minimum "drawn" gate length)
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
  - e.g., $\lambda = 0.3\mu m$ in $0.6\mu m$ process

CMOS Inverter Layout



Note: the N- and P- well are not shown in the layout



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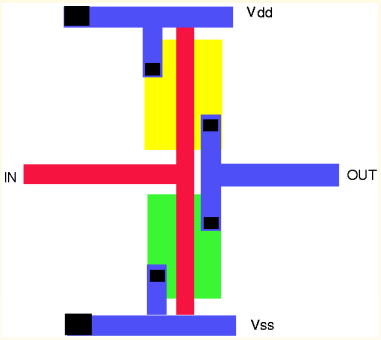
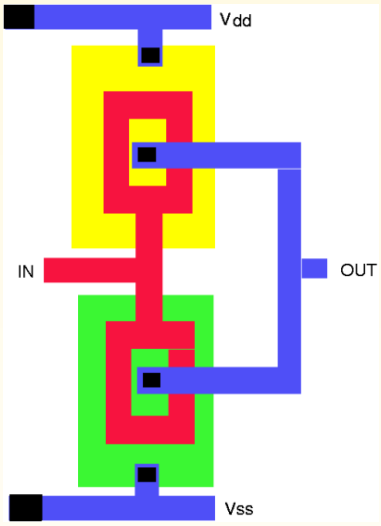
Other CMOS Layouts

Using wide transistors



Using even wider transistors



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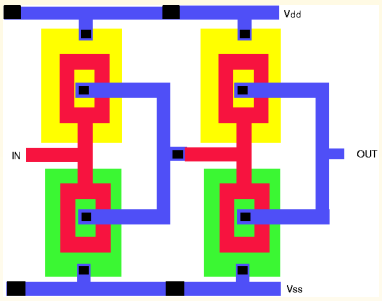
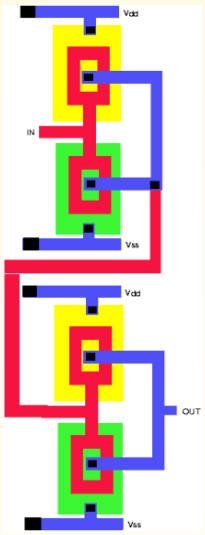
Buffer with Two Inverters

Side by side

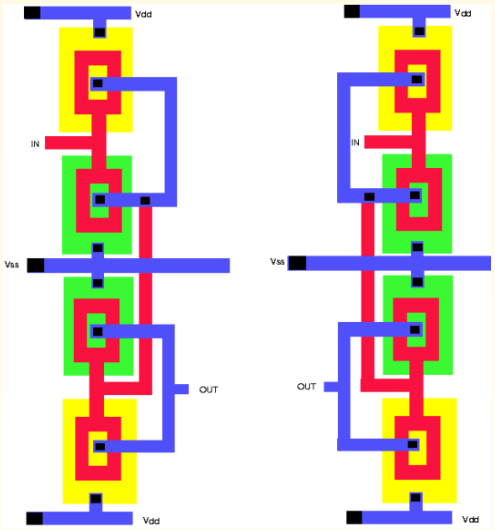


Stacked



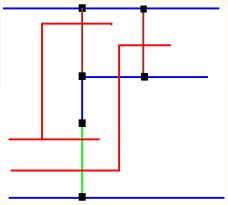
Improving Layout Efficiency

"Flip" a cell so that power (or ground) can be shared with another cell

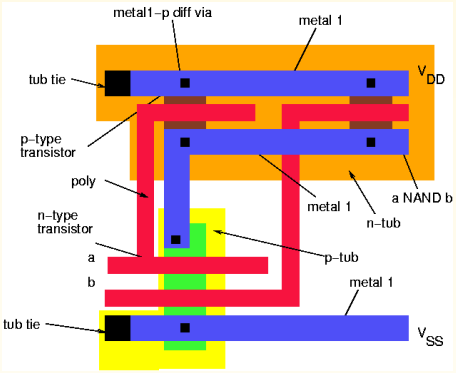


"Stick" Diagram and Simplified Layout of NAND Gate

Stick diagrams identify actual layers (which a schematic does not); both can be annotated with transistor sizes



n- and p-wells are shown

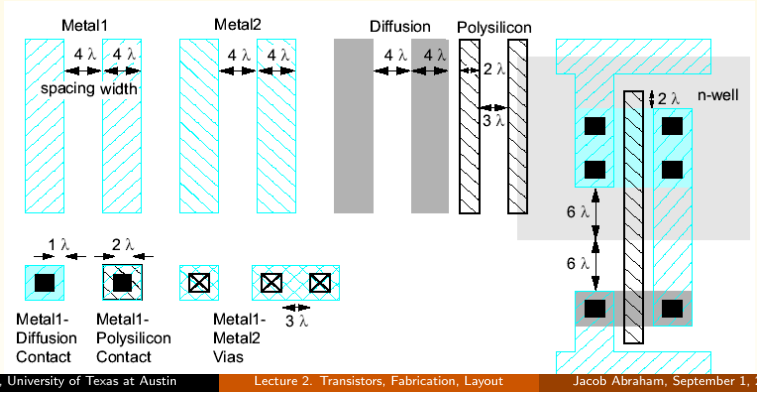


Simplified Design Rules

Based on λ (popular in academia)

Discussed in the textbook

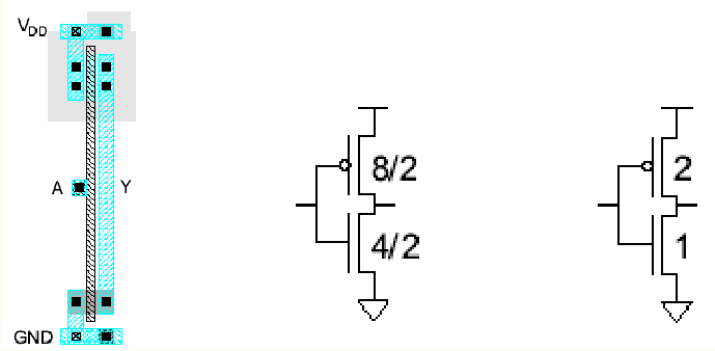
Rules based on λ can theoretically be migrated to a different technology (by changing the value of λ); in practice, all the rules do not scale in the same way, and industry typically does not use λ rules



Inverter Layout

Dimensions of pMOS and nMOS transistors

- Dimensions specified as Width/Length ($\frac{W}{L}$)
  - Minimum size, $4\lambda/2\lambda$, sometimes called unit-size transistor
  - (pMOS transistors are typically designed to be about twice the width of nMOS transistors, because of the mobilities of holes and electrons)



The MOSIS Scalable CMOS Rules

MOSIS is a prototyping and small-volume production service for VLSI circuit development

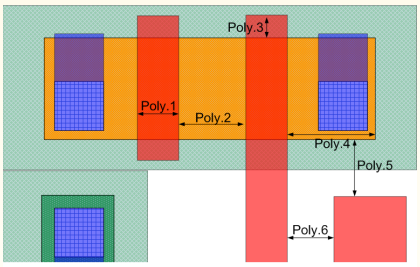
- MOSIS keeps costs down by combining many designs on a single die (multi-project chips)
  - Similar facilities exist in Europe (Europractice, CMP), Taiwan, etc.
- λ-based rules
- Designs using these rules are fabricated by a variety of companies
- Support for submicron digital CMOS, analog (buried poly layer for capacitor), micromachines, etc.
- https://www.mosis.com/files/scmos/scmos.pdf

Nangate 45nm Open Cell Library

Used in the laboratory exercises

- This is an open-source, standard-cell library
  - To aid university research programs and other organizations in developing design flows, designing circuits and exercising new algorithms
- Link to the *wiki*: http://www.eda.ncsu.edu/wiki/FreePDK45:Contents
- Example: poly rules (note: *summarized* here)

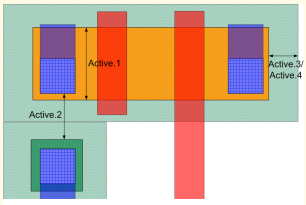
Rule	Value	Description
1	50 nm	Minimum width
2	140 nm	Minimum spacing
3	55 nm	Min. extension
4	70 nm	Min. enclosure
5	50 nm	Min. spacing
6	75 nm	Min. spacing



Example of Other Design Rules: Nangate 45nm

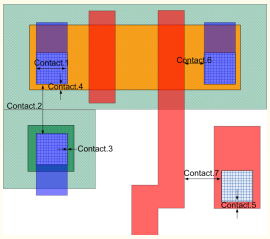
Active Rules

Rule	Value	Description
1	90 nm	Minimum width
2	80 nm	Minimum spacing
3	–	Min. well-active
4	–	active inside



Contact Rules

Rule	Value	Description
1	65 nm	Minimum width
2	75 nm	Minimum spacing
3	–	contact inside
4	5 nm	Min. active around
5	5 nm	Min. poly around
6	35 nm	Min. spacing with gate
7	90 nm	Min. spacing with poly

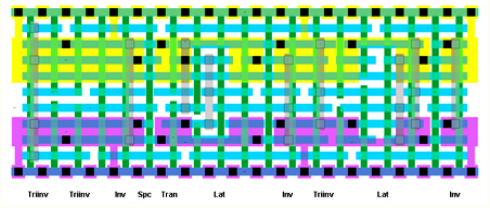


Trend Towards Reducing Number of Rules

Improve manufacturability

- Less flexibility for designers
- Intel reduced the number of poly layout rules for logic layout in 45nm by 37% compared with the 65 nm process
- Highly regular layout greatly reduces lithographic distortions
  - Limit rules, thereby limiting the number of allowed structures and shape relationships
  - Move towards 1-dimensional shapes and "Gridded Design Rules" (GDR)

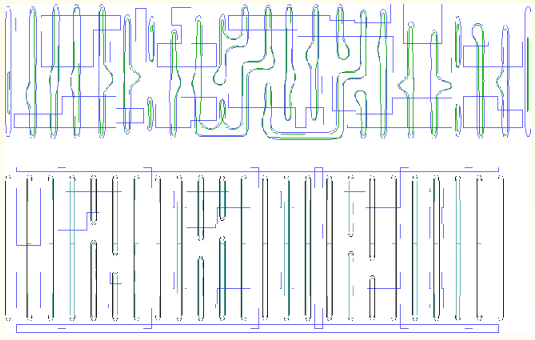
Example layout from Tela Innovations



Regular Layout

Lithography simulations

- Lithographic distortions reduced significantly with 1-D shapes and GDR
- Scan D Flip-Flop, 45nm process
- Source: Tela Innovations, Inc., ISPD 2009

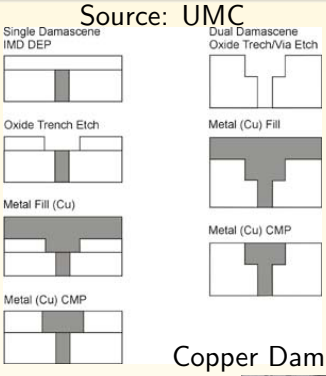


2D Conventional Layout

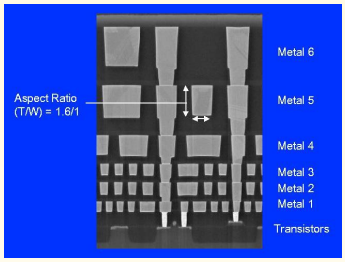
1D GDR Layout

Copper and the Damascene Process

Source: UMC



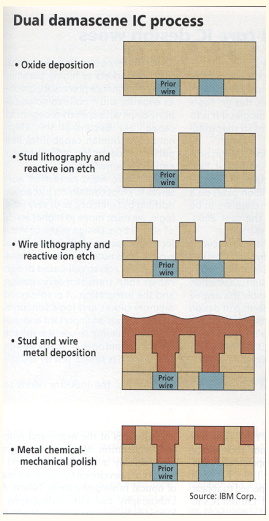
Layers of Damascene Copper (Intel)

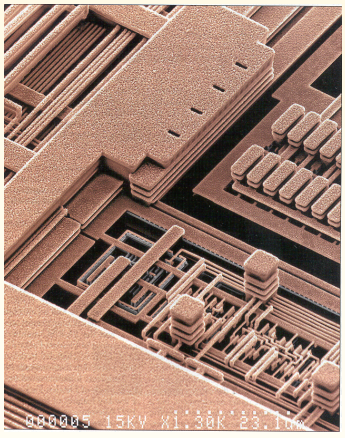


Copper Damascene Interconnect (Intel)

Advanced Metallization

IBM Technology (in Rabaey, Digital Integrated Circuits, 2nd ed.)
First commercial Copper process (0.12μ)





Example CMOS Circuit