22. SOI Technology, Packaging

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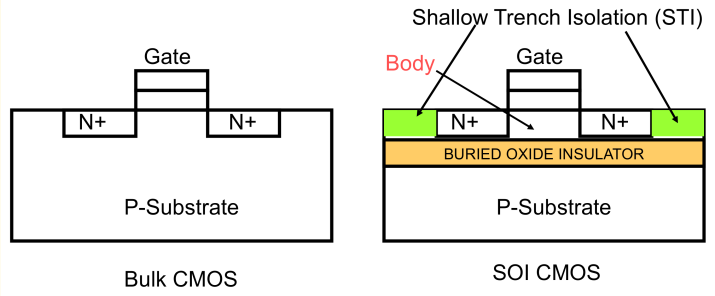
Silicon on Insulator (SOI) Technology

- Scaling of Bulk CMOS technology leads to issues such as
  - Sub-threshold leakage
  - Power
  - Parasitic device capacitances affecting the performance
- SOI technology has been around and used in other devices like IGFETs



Most of the process tooling is the same for Bulk and SOI
SOI devices have 5 terminals – Gate, Drain, Source, Substrate, Body

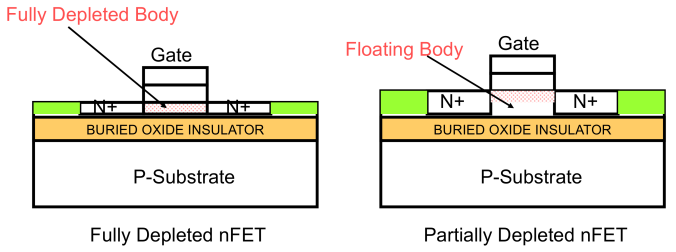
Types of SOI Devices

Fully Depleted (FD) devices

- Body is completely depleted under normal bias conditions
- The device behaves similar to a bulk device
- Requires a very thin film of Silicon so that the body can fully deplete

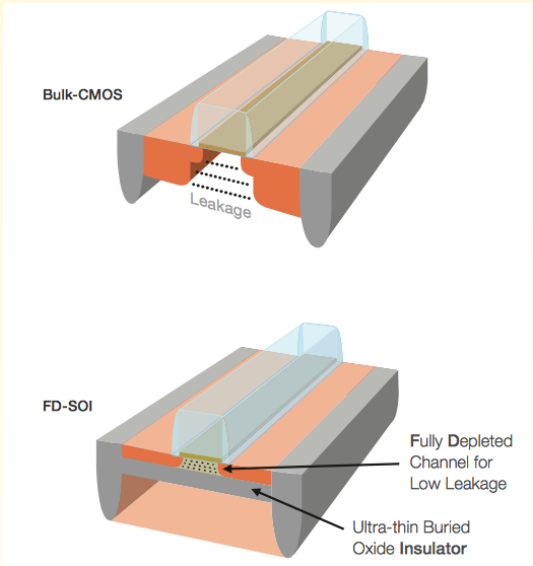
Partially Depleted (PD) devices

- Body is not completely depleted under normal bias conditions



Difficult to manufacture FD devices due to thin Si layer requirement

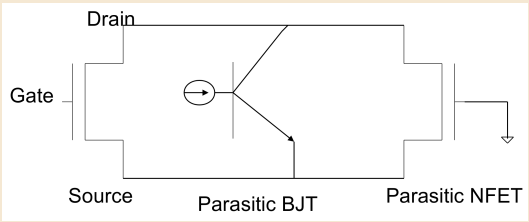
Bulk CMOS versus Fully-Depleted SOI



Source: Semiconductor Engineering, June 15, 2017; Global Foundries

PD SOI – Device Model and Floating Body Effects

PD SOI device model

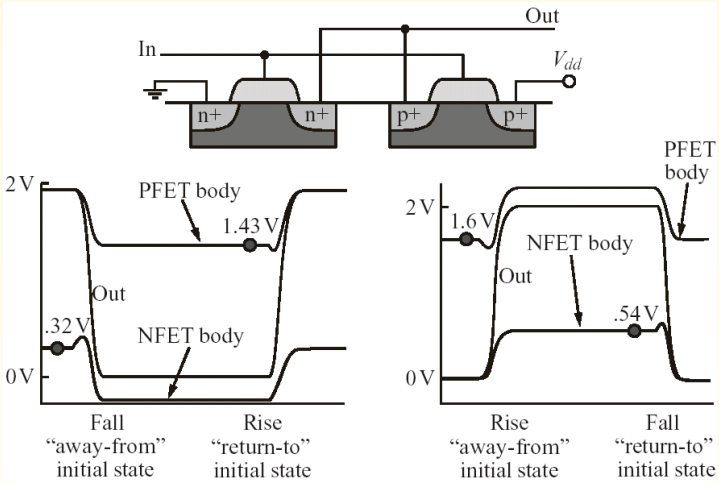


Floating body effects

- History Effect and Threshold Voltage Variability
  - Causes temporal delay variations
- Kinks
  - Lead to more current (I_{DS})
- Bipolar Device Action
  - Causes sudden Drain to Source discharge even when the FET is in the OFF state; this can lead to a functional error

History Effect

Body voltage (V_{BS}) alters device threshold voltage (V_T), which affects the propagation delay. ($V_T = V_T^0 + \gamma \cdot \sqrt{V_{SB}}$).



SOI Advantages and Disadvantages

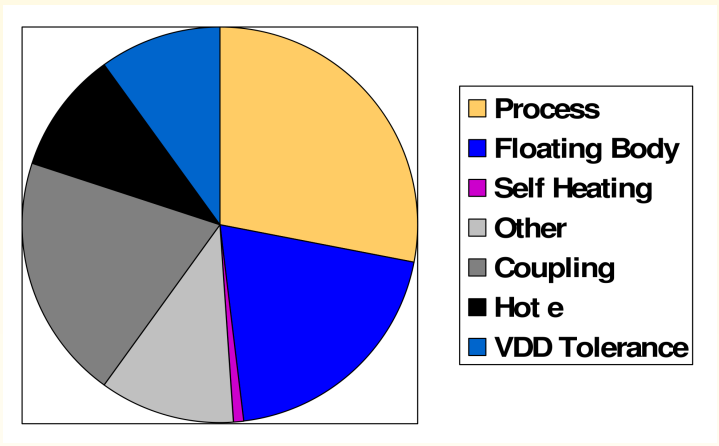
Advantages

- Diffusion capacitance reduction (since bottom touches insulator)
- Reduced short channel effect
- Lower device threshold
- Latch-up elimination (since no lateral PNP device possible)
- Reduced body effect/source follower action (smaller γ)
- Reduced soft error rate (absence of well/substrate as in bulk)
- Lower power (smaller diffusion capacitances)

Disadvantages

- History Effect
- Higher Drain Induced Barrier Lowering
- Self Heating

On-Chip Delay Variations for SOI



SOI in Industry

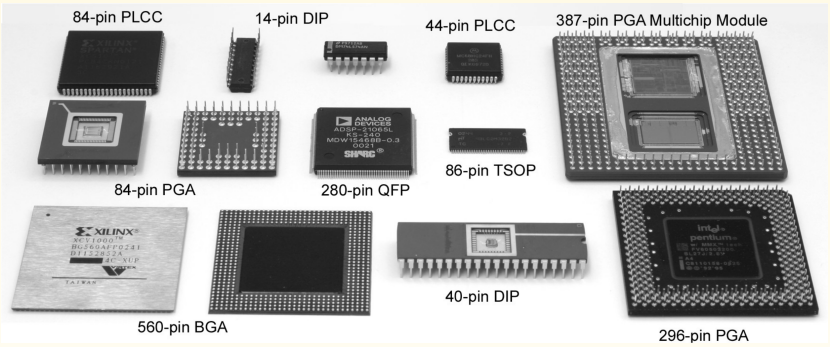
- IBM was the pioneer in developing SOI process technology
  - 45nm SOI process available through MOSIS
- Freescale (now NXP), Samsung have used SOI technology
- AMD processors have been designed in SOI technology
- Global Foundries is now providing the technology
  - Was focusing on FD-SOI process
  - However, a year ago, Global Foundries announced that it was pulling back from leading edge 7 nm process development to focus on specialized processes
- Intel and TSMC are still using bulk CMOS

Packages

- Package functions
  - Electrical connection of signals and power from chip to board
  - Little delay or distortion
  - Mechanical connection of chip to board
  - Removes heat produced on chip
  - Protects chip from mechanical damage
  - Compatible with thermal expansion
  - Inexpensive to manufacture and test

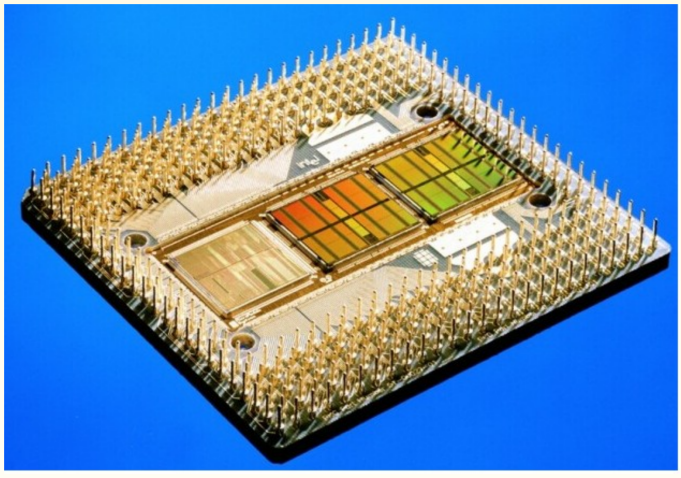
Package Types

Through-hole versus surface mount



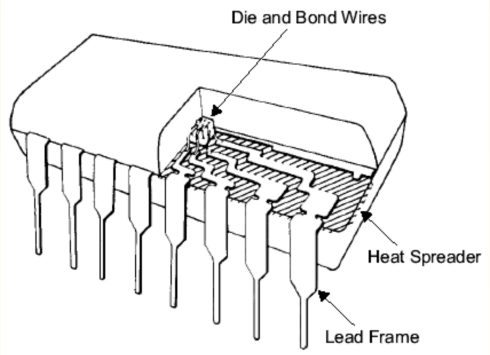
Multichip Modules (MCMs)

- Pentium Pro MCM
  - Fast connection of CPU to cache
  - Expensive, requires known good dice



Chip-to-Package Bonding

- Traditionally, chip surrounded by pad frame
  - Metal pads on 100 – 200 μm pitch
  - Gold bond wires attach pads to package
  - Lead frame distributes signals in package
  - Metal heat spreader helps with cooling

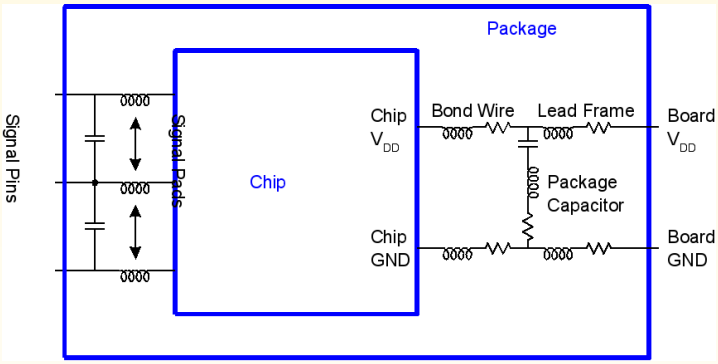


Advanced Packages

- Bond wires contribute parasitic inductance
- Fancy packages have many signal, power layers
  - Like tiny printed circuit boards
- Flip-chip places connections across surface of die rather than around periphery
  - Top level metal pads covered with solder balls
  - Chip flips upside down
  - Carefully aligned to package (done blind!)
  - Heated to melt balls
  - Also called C4 (Controlled Collapse Chip Connection)

Package Parasitics

- Use many V_{DD}, GND in parallel
  - Inductance, I_{DD}



Heat Dissipation

- 60 W light bulb has surface area of 120 cm^2
- Itanium 2 die dissipates 130 W over 4 cm^2
  - Chips have enormous power densities
  - Cooling is a serious challenge
- Package spreads heat to larger surface area
  - Heat sinks may increase surface area further
  - Fans increase airflow rate over surface area
  - Liquid cooling used in extreme cases ($$$)

Thermal Resistance

- $\Delta T = \theta_{ja} P$
  - ΔT: temperature rise on chip
  - θ_{ja}: thermal resistance of chip junction to ambient
  - P: Power dissipation on chip
- Thermal resistances combine like resistors
  - Series and parallel
- $\theta_{ja} = \theta_{jp} + \theta_{pa}$
  - Series combination of junction-package and package-ambient thermal resistances

Example

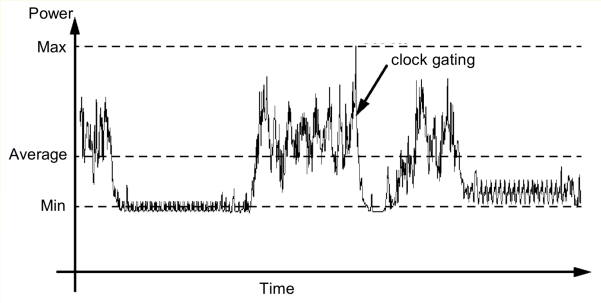
- Chip has a heat sink with a thermal resistance to the package of 4.0°C/W
- The resistance from chip to package is 1°C/W
- The system box ambient temperature may reach 55°C
- The chip temperature must not exceed 100°C
- What is the maximum chip power dissipation?
- (100-55C)/(4 + 1 C/W) = 9 W

Power Distribution

- Power Distribution Network functions
  - Carry current from pads to transistors on chip
  - Maintain stable voltage with low noise
  - Provide average and peak power demands
  - Provide current return paths for signals
  - Avoid electromigration and self-heating wearout
  - Consume little chip area and wire
  - Easy to lay out

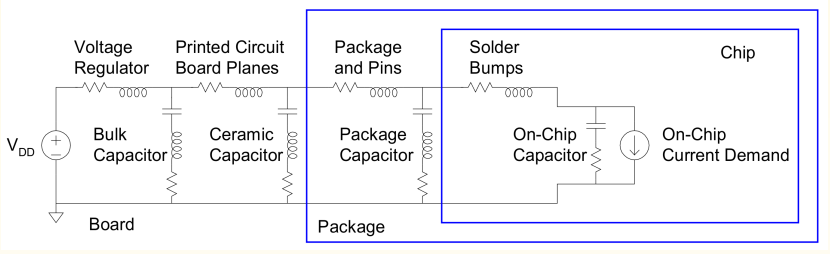
Power Requirements

- $V_{DD} = V_{DDnominal} - V_{droop}$
- Want $V_{droop} <$ +/-10% of V_{DD}
- Sources of V_{droop}
  - IR drops
  - L di/dt noise
- I_{DD} changes on many time scales



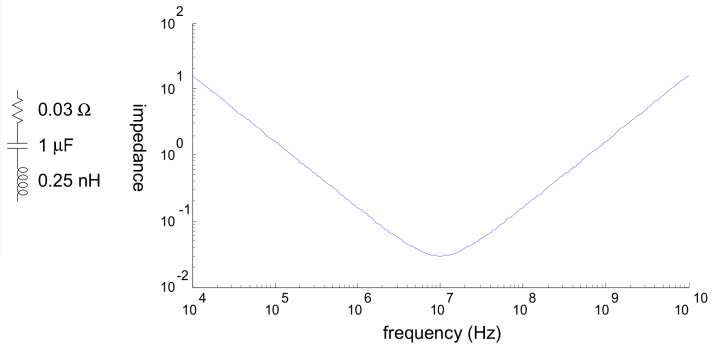
Power System Model

- Power comes from regulator on system board
  - Board and package add parasitic R and L
  - Bypass capacitors help stabilize supply voltage
  - But capacitors also have parasitic R and L
- Simulate system for time and frequency responses



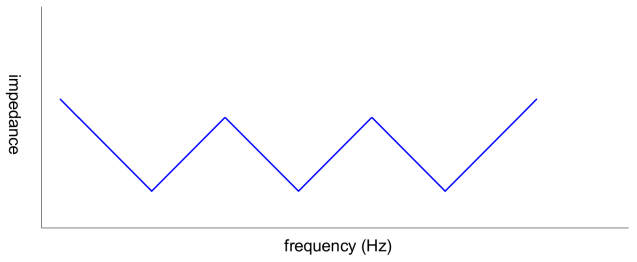
Bypass Capacitors

- Need low supply impedance at all frequencies
- Ideal capacitors have impedance decreasing with ω
- Real capacitors have parasitic R and L
  - Leads to resonant frequency of capacitor



Frequency Response

- Use multiple capacitors in parallel
  - Large capacitor near regulator has low impedance at low frequencies
  - But also has a low self-resonant frequency
  - Small capacitors near chip and on chip have low impedance at high frequencies
- Choose caps to get low impedance at all frequencies



Input/Output

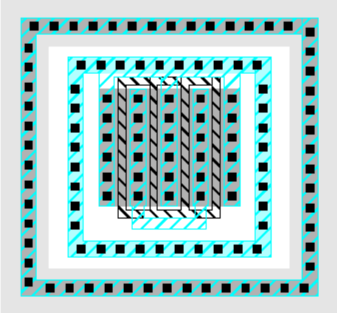
- Input/Output System functions
  - Communicate between chip and external world
  - Drive large capacitance off chip
  - Operate at compatible voltage levels
  - Provide adequate bandwidth
  - Limit slew rates to control di/dt noise
  - Protect chip against electrostatic discharge
  - Use small number of pins (low cost)

I/O Pad Types

- V_{DD}/GND
- Output
- Input
- Bidirectional
- Analog

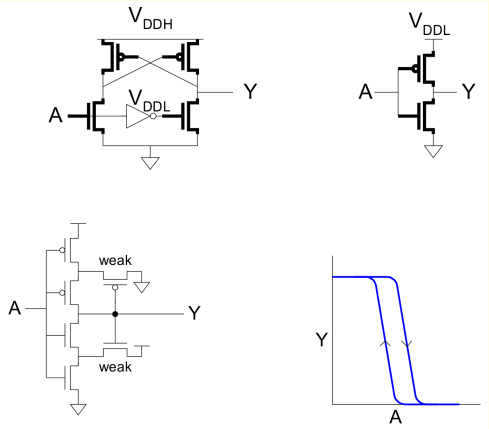
Output Pads

- Drive large off-chip loads (2 – 50 pF)
  - With suitable rise/fall times
  - Requires chain of successively larger buffers
- Guard rings to protect against latchup
  - Noise below GND injects charge into substrate
  - Large nMOS output transistor
  - p+ inner guard ring
  - n+ outer guard ring (in n-well)



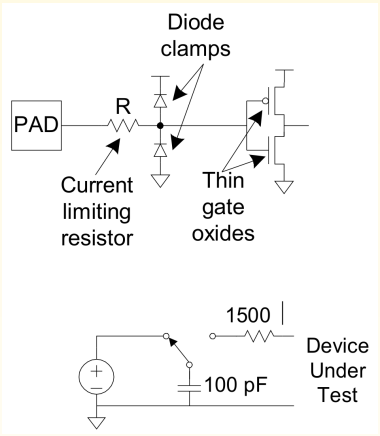
Input Pads

- Level conversion
  - Higher or lower off-chip V
  - May need thick oxide gates
- Noise filtering
  - Schmitt trigger
  - Hysteresis changes V_{IH}, V_{IL}
- Protection against electrostatic discharge



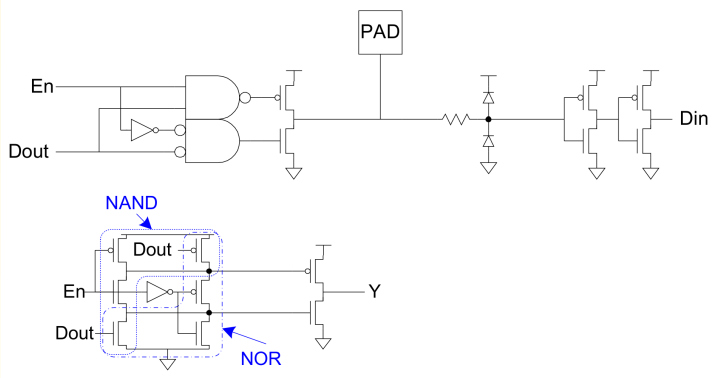
Electrostatic Discharge (ESD) Protection

- Static electricity builds up on the body
  - Shock delivered to a chip can fry thin gates
  - Must dissipate this energy in protection circuits before it reaches the gates
- ESD protection circuits
  - Current limiting resistor
  - Diode clamps
- ESD testing
  - Human body model
  - Views human as charged capacitor

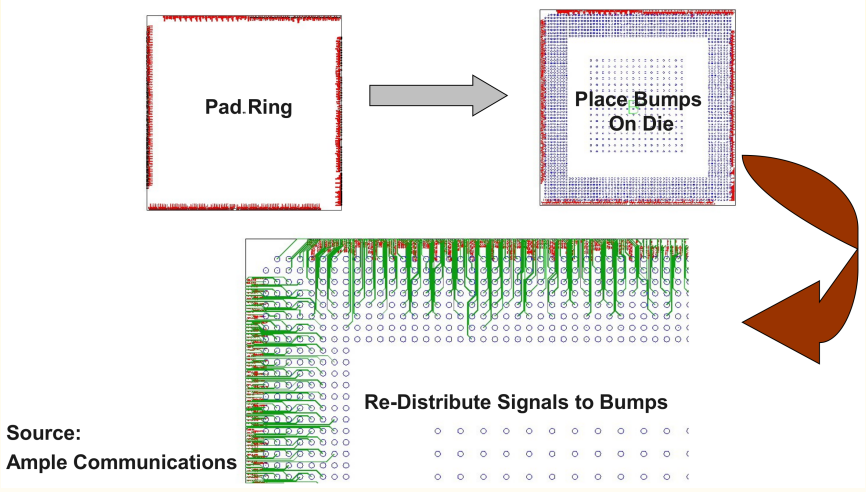


Bidirectional Pads

- Combine input and output pad
- Need tristate driver on output
  - Use enable signal to set direction
  - Optimized tristate avoids huge series transistors

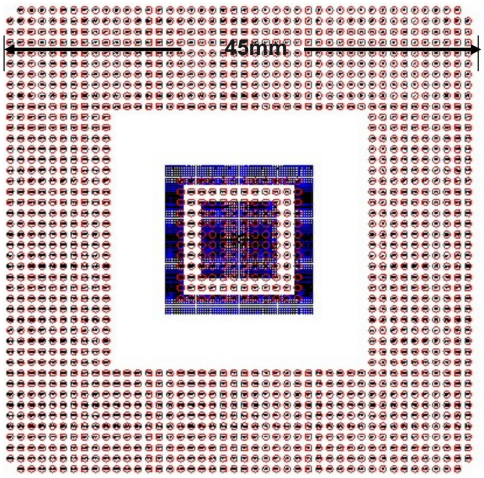


Package Design Steps



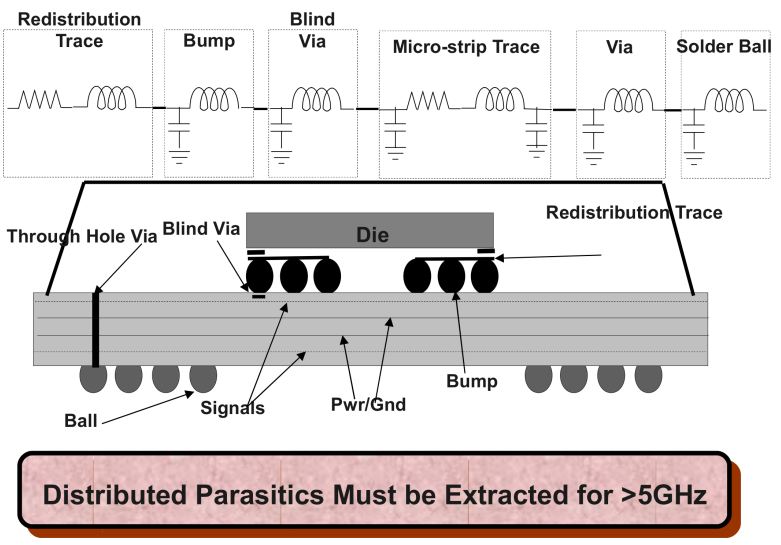
Flip the Chip and Place on Substrate

Substrate has two usable layers for signal routing
Two layers are dedicated for various split planes



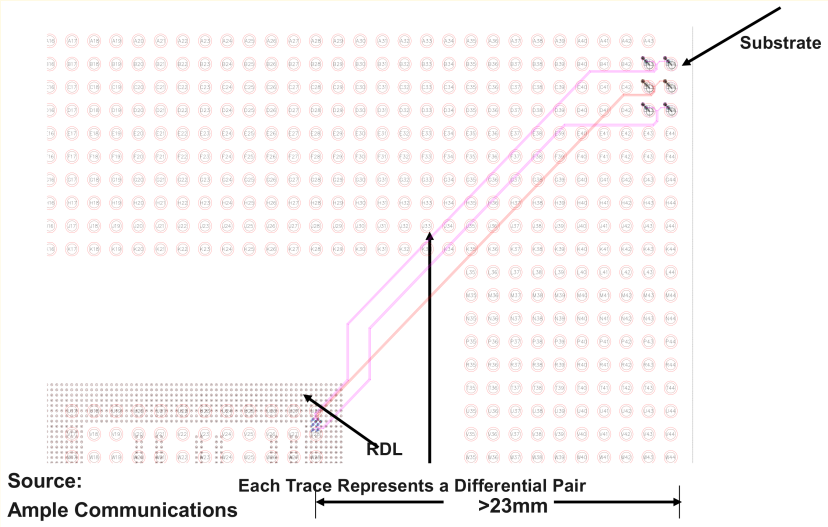
Source:
Ample Communications

Electrical Model for the Package



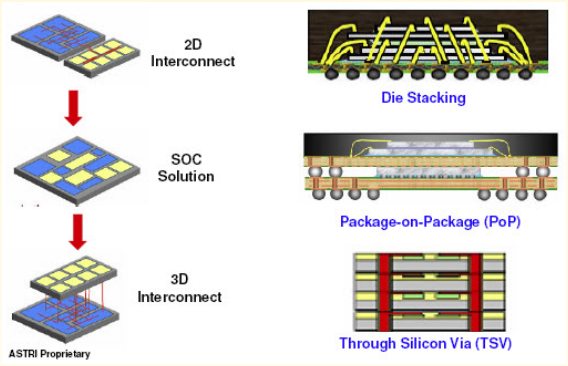
Source: Ample Communications

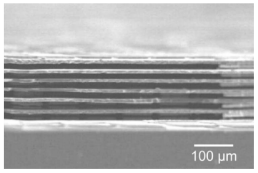
Differential Signals on Two Layers



3-D Packaging

Attempt to extend Moore's law



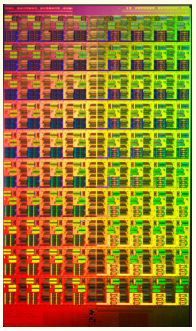


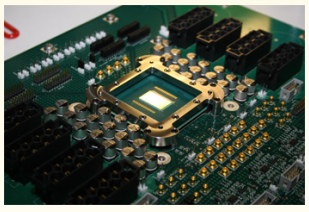
3D System: Intel Pentium 4, 2004

- Two dies using face-to-face stacking
  - Allows dense via structure
- Backside TSVs are used for IO and power supply
- Compared to the 2D Pentium 4, 3D design results in
  - 15% performance improvement (due to eliminated pipeline stages)
  - 15% power saving (due to eliminated repeaters and reduced wiring)

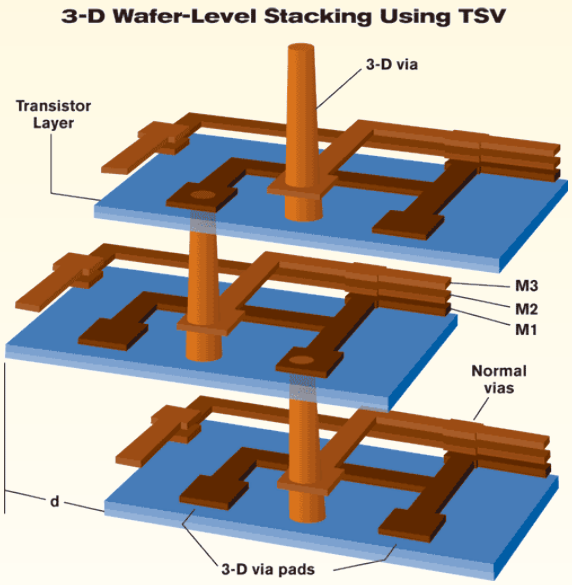
3D-System: Intel Teraflops Research Chip, 2007

- 80 cores with routers
  - Cores simpler than the ones in conventional multicore chips
- **SRAM chip stacked directly under the cores**
  - Reduce the distance, therefore signal delay and power





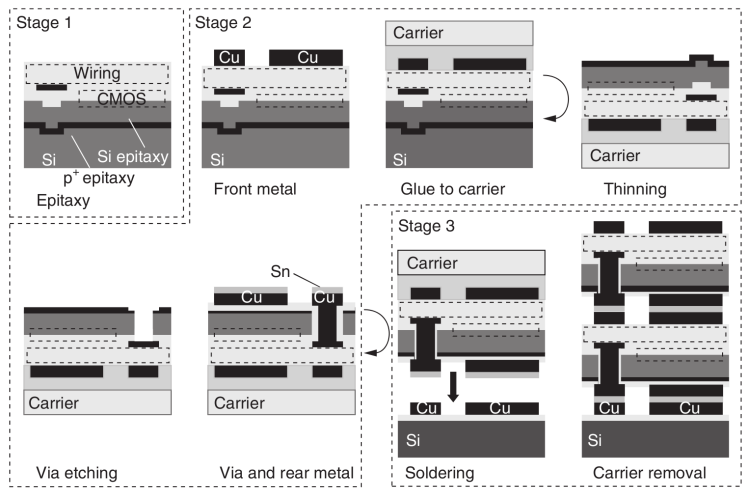
3-D Packaging with Through Silicon Vias (TSVs)



Source: Semiconductor International

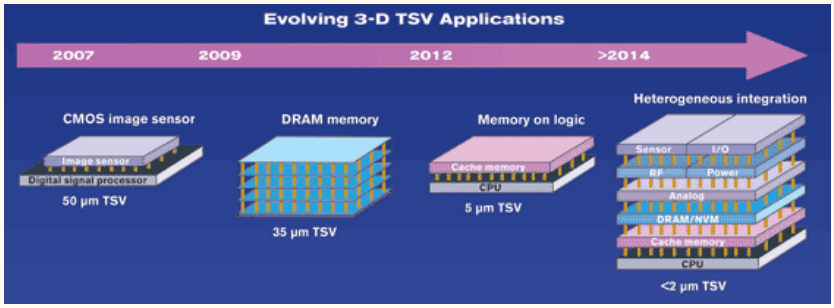
3-D Stacking of Chips

Processing steps in 3-D stacking



Source: Benker, IEEE Design & Test, Nov.-Dec., 2005

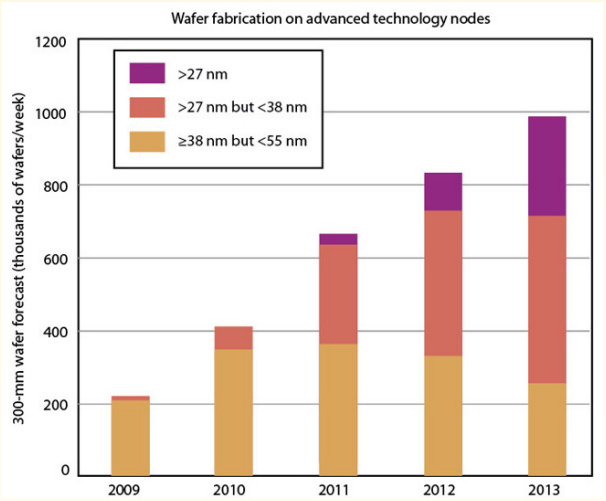
Applications of 3D-TSV Technology



Source: Semiconductor International

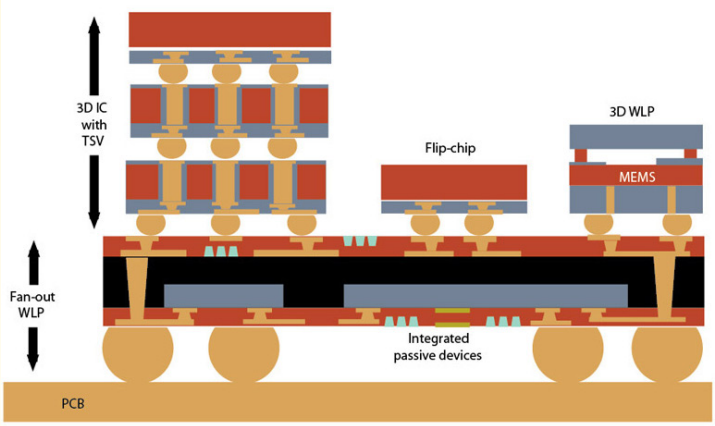
Wafer Fabrication on Advanced Technology Nodes

Adoption of 3D ICs is forecast to be a future packaging trend



Source: Electronic Design, July 2, 2010, and VLSI Research, Inc.

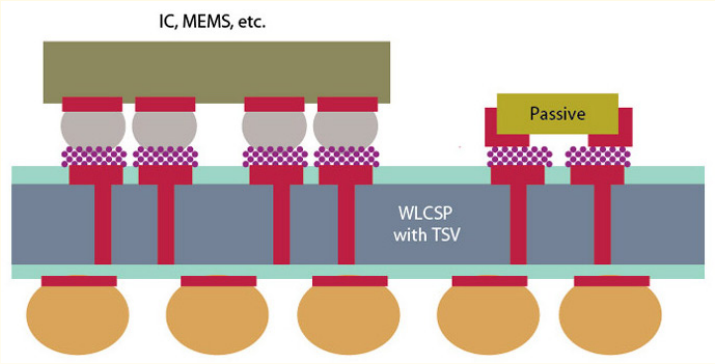
Wafer Level Packaging (WLP) Using Through-Silicon Vias (TSVs)



Source: Electronic Design, July 2, 2010, and Yolé Devéloppment

Wafer-Level Chip-Scale Packaging

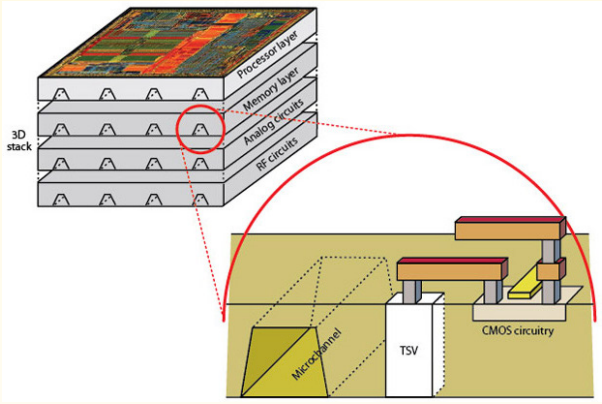
ICs will be integrated with MEMS and passive components using wafer-level chip-scale packaging and TSVs



Source: Electronic Design, July 2, 2010, and Texas Instruments

Stacking Different Dies in 3D

Processor, memory, logic and Analog/RF circuitry can be interconnected with TSVs
Liquids using MEMS microchannels can be used to cool the stack



Source: Electronic Design, July 2, 2010, and École Polytechnique Fédérale de Lausanne

TSV Overhead

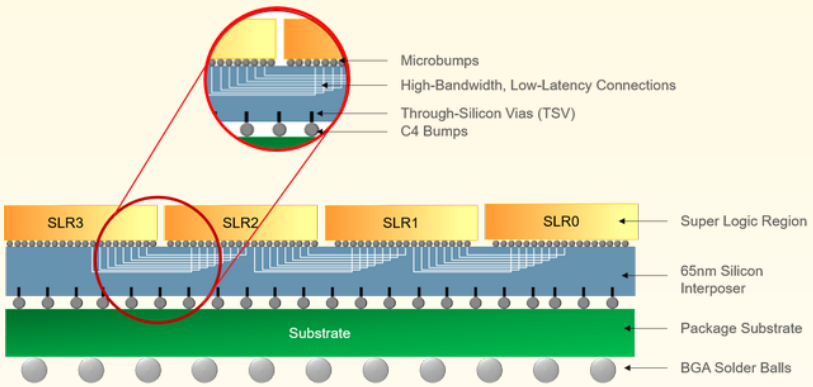
SILICON CONSUMPTION AS A FUNCTION OF TSV ASPECT RATIO

TSV aspect ratio	5:1	10:1	20:1
TSV size (diameter × depth, µm)	40 × 20	20 × 200	10 × 200
Keep-out area (2.5 × diameter, µm)	100	50	2.5
Total TSV footprint (mm^2)	7.9	2	0.5
Footprint relative to IC area	12.3%	3.10%	0.80%
Average TSV density = 16 TSVs/mm^2; die size = 8 × 8 mm			

Courtesy of Alchimer S.A.

Source: Electronic Design, July 2, 2010

Chiplets – Example Xilinx VU19P



Source: Xilinx and G. Hilson, EE Times Asia, July 10, 2020