

Jyotirmoy V. Deshmukh

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Education

Ph.D. Candidate,

Dept. of Electrical and Computer Engg., University of Texas at Austin.
August 2002 – Present. Advanced to candidacy: April 2007.
Advisor: Dr. E. Allen Emerson. Co-advisor: Dr. Adnan Aziz. GPA: 3.86
Dissertation Topic: Parameterized Data Structure Verification.

Bachelor Of Engineering in Electronics,

Veermata Jijabai Technological Institute (VJTI), Mumbai, India.
June 1996 to August 2000.
First Class with Distinction, First Rank in B.E. Electronics.

Work Experience and Internships

Research Intern, Rigorous Software Engineering,

Microsoft Research India, Bangalore, India.
May 2008 to August 2008.
Mentors: Ganesan Ramalingam, Kapil Vaswani.
Focus Area: Concurrency aspects in Programming Languages.

Research Assistant/Consultant, Systems Analysis and Verification,

NEC Labs America, Princeton, NJ.
August 2007 to December 2007.
Mentors: Sriram Sankaranarayanan.
Focus Area: Tool Development and Research on Deadlock Detection.

Research Intern, Systems Analysis and Verification,

NEC Labs America, Princeton, NJ.
May 2007 to August 2007.
Mentors: Sriram Sankaranarayanan, Vineet Kahlon, Aarti Gupta.
Focus Area: Static Analysis for Deadlock Detection in Concurrent Java programs.

Software and Circuit Design Engineer,

Texas Instruments India, Bangalore, India.
July 2000 to December 2001.
Signal Integrity Verification and Timing Analysis Group, ASIC, R&D Center Asia.

Academic Employment

Teaching Assistant, Engineering Programming Languages (C++),
Department of Electrical and Computer Engineering, Univ. of Texas at Austin.
Fall 2006, Fall 2008 (current). Supervised by: Prof. Craig Chase.

Teaching Assistant, Concurrent and Distributed Programming in Java.
Department of Electrical and Computer Engineering, Univ. of Texas at Austin.
Spring 2007, Spring 2008. Supervised by: Prof. Vijay Garg, Dr. Alper Sen.

Graduate Research Assistant,
Computer Engineering Research Center, Univ. of Texas at Austin.
Fall 2002 to Spring 2006. Advisor: Dr. E. Allen Emerson.

Publications

Symbolic Deadlock Analysis for Concurrent Libraries and their Clients
co-authored with: E. Allen Emerson, Sriram Sankaranarayanan, accepted at ASE 2009.

Verification of Recursive Method on Tree-like Data Structures.
co-authored with: E. Allen Emerson, accepted at FMCAD 2009.

Automatic Repair of Local Errors in Boolean Programs.
In proc. of FMCAD 2008, co-authored with: Roopsha Samanta, E. Allen Emerson.

Automatic Verification of Parameterized Data Structures.
In proc. of TACAS 2006, co-authored with: E. Allen Emerson, P. Gupta.

Logical Concurrency Control from Sequential Proofs.
(Submitted) co-authored with: G. Ramalingam, K. Vaswani and V. P. Ranganathan.

Academic Awards

Professional Development Award 2008, Univ. of Texas at Austin.
General Engineering Travel Grant 2006, Univ. of Texas at Austin.
Department of Computer Science Travel Grant 2006, Univ. of Texas at Austin.
Second place among 189 students, IIT Mathematics Olympiad, 1999.
National Talent Scholarship, India, 1994-2000.

Key Projects

Program analysis tool based on SOOT for concurrent software analysis (with NEC Labs).
Pravda: parameterized data structure correctness verification tool.
Tree Automata Library in Java.
Project on file system verification using formal techniques (as a mentor).
BDD based tool for checking satisfiability of Quantified Boolean Formulae (in C).
Verification of USB 2.0 based core using predicate abstraction and slicing.
Distributed load balancer in Java.

Skills

Programming languages: C, C++, C#, Java, Perl, Scheme, Lisp, Acl2, SystemC, Lex/Yacc.
Formal Verification Tools: SMV, VIS, ACL2, SLAM, SOOT.

Professional Activities

External Reviewer for: VLSI 2003; FSTTCS 2004; CAV 2004,05; VMCAI 2005, 06; ATVA 2007, SPIN 2008, TACAS 2008, ISSTA 2008, Journal of Science of Computer Programming, SPIN 2009, FSEN 2009.

Member of Association for Computing Machinery (ACM)