A 1.4mW 8b 350MS/s Loop-Unrolled SAR ADC with Background Offset Calibration in 40nm CMOS

Kareem Ragab and Nan Sun
University of Texas at Austin, Austin, TX
Email: kragab@utexas.edu, nansun@mail.utexas.edu

Abstract—A divide-and-conquer approach to address comparator offset mismatch in loop-unrolled SAR ADC is presented. Redundancy and coarse foreground calibration mitigate MSB comparators offset mismatches. A novel background calibration loop matches LSB comparators offsets to a reference comparator. The proposed scheme avoids a dedicated calibration cycle that would slow down conversion. Additionally, it ensures input common mode voltage tracking for each comparator during both calibration and normal operation, without requiring external inputs or special DAC configuration. This enabled the use of a simple bidirectional single-side switching scheme to eliminate switching logic which further boosts speed and reduces switching power. An 8b prototype ADC achieves 45dB SNDR and a Nyquist FOM of 31.3fJ/conv-step at 350MS/s in 40nm CMOS.

I. INTRODUCTION

Recent years have witnessed a significant increase in the speed of single-channel SAR ADCs reaching 750MS/s in 28nm CMOS [1] and 1.2GS/s in 32nm SOI [2] for 8b resolution. This is enabled by both technology scaling and circuit innovations including asynchronous clocking [1-3], multi-bit per step [1,4-5], comparator alternation [2], and loop unrolling [6,7]. The loop-unrolled architecture uses a dedicated comparator for each bit decision. This boosts speed by not only removing comparator reset time from the critical path, but also eliminating logic and memory delay between the comparator and the capacitive DAC (CDAC) [6]. However, its linearity significantly suffers from offset mismatches between the N-comparators used in an N-bit realization.

Offset mismatch was addressed using foreground calibration [6,7] and residue amplification [7]. However, as comparator offset and residue amplification gain drift with voltage and temperature variations, these schemes require system operation to be interrupted for offline ADC recalibration. To circumvent this limitation, we propose a background offset calibration technique that relies on a reference comparator with alternating trigger time. The offset of each LSB comparator is matched to that of the reference by firing them simultaneously during SAR conversion and checking their output difference. This method avoids the need for a dedicated background calibration cycle that slows down conversion speed. MSB comparators offsets are foreground calibrated at power-on. The proposed foreground calibration does not require external inputs [6] or direct CDAC control [7] which introduces additional delays.

This paper is organized as follows. Section II presents the proposed ADC architecture. Section III describes circuit implementation details. Measurement results of the prototype ADC are reported in Section IV, followed by the conclusion in Section V.

II. ADC ARCHITECTURE

A. Basic Operation

Fig. 1 shows ADC architecture and timing diagram. Before describing the basic operation, the three key architectural improvements that tackle the offset mismatch problem are highlighted. First, a redundant bit is added after the 4th decision to provide an error budget for MSB comparators offset mismatches and CDAC settling errors. This relaxes offset matching requirement for the first four MSB comparators, simply referred to as the MSB comparators. Second, a calibration unit performs power-on foreground coarse offset calibration for the MSB comparators. Third and more importantly, an auxiliary reference comparator enables background fine offset calibration for LSB comparators.

For basic operation, we may ignore the reference comparator. The differential input is tracked using boot-strapped track-and-hold switches [9] and is top-plate sampled on the differential CDAC on $clk$ falling edge. $clk_s$ is generated by gating the ADC 50% duty-cycle external clock $clk_{ext}$ as shown in Fig. 1. A dedicated comparator is used to resolve each bit decision and stores comparison result. No additional memory elements are needed as the comparators are only reset after conversion is completed. The 1st MSB comparator is triggered on $clk_s$ falling edge. Buffered comparator outputs $d_0[8]$ and $d_s[8]$ directly drive MSB capacitor bottom plate without the need for any logic. A 3-bit programmable delay line (PDL) ensures sufficient time for DAC settling. A dynamic OR detects the completion of the first SAR step and generates $clk_{[7]}$ to trigger the 2nd MSB comparator. This operation repeats in a domino-like fashion until all bits are resolved. Finally, digital outputs $d_p[8:0]$ are latched using $clk_l$ and then the entire ADC is reset on $Reset$ high.

B. LSB Comparators Background Calibration

Each conversion cycle, the reference comparator is triggered simultaneously with one of the LSB comparators. This is achieved by periodically aligning the reference comparator clock with each of the LSB comparators clocks $clk_{[4:0]}$, once every five cycles, using a multiplexer as shown in Fig. 1. The difference of the reference comparator output $d_{ref}$ and output of the $i$th LSB comparator being calibrated $d_p[i]$, $i \in [0 : 4]$ represents offset mismatch error. This error signal is low pass filtered, to suppress fluctuation due to comparators noise, and fedback to cancel the LSB comparator offset mismatch. Performing the calibration during normal SAR operation offers two advantages. First, it avoids budgeting a dedicated calibration time slot that would slow down conversion speed.
Second, the calibration is intrinsically performed at the right input common mode voltage. After convergence, all LSB comparators would have the same offset as the reference comparator, which sets the entire ADC offset.

C. MSB Comparators Foreground Calibration

The background offset calibration described in the previous section can be extended to calibrate MSB comparators. However, this would slow down convergence due to the low probability of MSB comparator input falling close to comparator threshold. Therefore, an alternative approach is taken to handle MSB comparators offset mismatch. First, a redundant bit is placed after the 4th decision that provides an error budget of 8LSB, divided into 4LSB for CDAC settling error and 4LSB for MSB comparators offset mismatches. This relaxes the offset matching requirement for the MSB comparators and allows for offset drift after foreground calibration.

During power-on foreground calibration, ADC inputs $V_{in,p}$ and $V_{in,n}$ are shorted to apply a zero input and the ADC operates exactly like in normal operation except for two differences. First, switch $S_0$ shorts the two CDACs as shown in Fig. 1. This ensures that: (a) a zero-input is applied to each comparator regardless of the decision of its preceding comparator, and (b) the input common mode voltage for each comparator is the same as in normal operation. Second, in order to reduce $S_0$ size, all PDLs are set to their maximum delay and ADC clock is reduced to allow sufficient time for settling during foreground calibration. With zero-input applied, the calibration unit digitally trims the offset for each of the MSB comparators and the reference comparator, based on their outputs, to $\pm 2$LSB.

III. CIRCUIT IMPLEMENTATION

A. Capacitive DAC

CDAC schematic is shown in Fig. 2. A MOM capacitor of 1.9fF is used for the unit capacitor $C_u$. CDAC switches are scaled in proportion to the switched capacitor. Redundant capacitor $8C_u$ is used to provide an error budget for MSB decisions. Conversion time saving from MSB steps CDAC incomplete settling compensates for the additional time required for the redundant SAR step. As incomplete settling error is largest for the second comparison and is negligible for the first comparison, the second MSB capacitor is sized to $28C_u$ instead of $32C_u$. This translates 4LSB of redundancy from the first comparison to the second comparison increasing its incomplete settling error budget to 8LSB.

A bidirectional single-side switching scheme is used [8]. This scheme allows the comparators to directly drive the CDAC without additional logic. After each comparison, only one side of the CDAC is switched. Additionally, this switching scheme enables control of CDAC common mode voltage during SAR operation. The common mode voltage profile is optimized to increase speed and improve LSB comparators offset mismatch. A mean common mode voltage close to $0.6V_{dd}$ increases Strong-Arm latch comparator regeneration speed without significantly increasing its input referred noise [2]. Moreover, by proper selection of the up and down transitions, the common mode variation is minimized for the LSB SAR steps. This reduces the residual systematic offset mismatch due to dependence of the reference comparator offset on the common mode voltage in the LSB steps.
Fig. 2. Schematic of the differential CDAC (a) and its common mode voltage profile (b).

Fig. 3. Schematic of MSB comparator with coarse offset correction (a) and LSB comparator with fine offset correction (b).

B. Comparators

Schematic of the MSB comparator with coarse offset correction is shown in Fig. 3a. A Strong-Arm latch is chosen for its good balance between speed, noise, and power [2]. The comparator is sized for noise and speed. It has an input referred RMS noise and offset of 0.6mV and 7mV respectively. Both MSB and LSB comparators share the same latch design and size. MSB comparator offset is corrected using auxiliary binary weighted input devices that are digitally controlled by the calibration unit. The gate terminals of the auxiliary transistors are connected to a switched capacitor (SC) reference. For each MSB comparator, capacitor ratio $C_1/C_2$ is chosen such that the gate voltage of the auxiliary transistors is nearly equal to the comparator’s input common mode voltage. $C_{ref}$ is sized to 22fF for negligible impact of comparator kickback on the reference value.

Fig. 3b shows the schematic of the LSB comparator. An auxiliary input pair is used for offset correction. Positive input $V_{cal,p}$ is connected to a fixed SC reference, which is re-used in all LSB slices given their similar common mode voltage. Negative input $V_{cal,n}$ is used to correct comparator offset and is stored on capacitor $C_{cal} = C_{ref}$ for nominal matching. This structure is similar to [2] with difference in the driving logic. Calibration unit uses the difference between the reference comparator output $d_{ref}$ and LSB comparator latched output $d[i]$ to dynamically update $V_{cal,n}$ by adding or subtracting charge from $C_{cal}$ using the UP/DN control signals. If $d_{ref} = 0$ and $d[i] = 1$, UP is set to 1 which increases $V_{cal,n}$. If $d_{ref} = 1$ and $d[i] = 0$, DN is set to 1 which decreases $V_{cal,n}$. If $d_{ref} = d[i]$, $V_{cal,n}$ remains unchanged. All $V_{cal,n}$ updates and SC reference refreshes are performed during ADC reset in order to avoid disturbing comparator offset during SAR operation.

In order to reduce $V_{cal,n}$ ripple at steady state, a large deep-trench $C_{cal}$ was used in [2]. As deep-trench capacitors were not available in the target standard CMOS process, we adopt an alternative approach to reduce the requirement on $C_{cal}$ size and save area. First, $C_{par1}$ and $C_{par2}$ are realized using only parasitic capacitance. Second, a narrow pulse is used to drive the charge transfer switches to further reduce the transferred charge as shown in Fig. 3b. Using these two methods, a small $C_{cal}$ of only 22fF equal to that used in the SC reference is sufficient to suppress the ripple power to a negligible level below ADC noise floor.

IV. Measurement Results

The prototype ADC was implemented in 40nm CMOS. Die photograph is shown in Fig. 4. The ADC operates at 350MS/s under 1.1V supply. It consumes in total 1.37mW which includes the on-chip background calibration. Fig. 5 shows measured SNDR and SFDR vs. input frequency. SNDR is better than 43.7dB in the first Nyquist zone. Measured ADC spectrum for a 158MHz 0dBFS input signal with an SNDR of 43.7dB and SFDR of 59.5dB is shown in Fig. 6. Measured DNL and INL are improved from +1.7/-1 LSB and +2.3/-0.7 LSB respectively to +0.8/-0.9 LSB and +0.6/-0.9 LSB respectively with background calibration enabled as shown in Fig. 7.

Table I summarizes the performance of the proposed ADC. The ADC achieves a FOM that is in line with state-of-the-art SAR ADCs with single-channel speeds ≥250MS/s and resolutions ≥8b and is the smallest for implementations that resolve single-bit per cycle in bulk CMOS. Simple logic, fully dynamic comparators, and eliminated CDAC latches enable
the proposed architecture to achieve a good balance between power and speed. FOM can be further improved by sizing down MSB comparators as in [7].

V. CONCLUSION

This paper presented an 8b loop-unrolled SAR ADC with background offset calibration. Incorporating redundancy simplifies the offset mismatch problem for the MSB comparators. Both MSB and LSB comparators are calibrated at their corresponding common mode voltage in normal operation. The proposed calibration maintains the high-speed merit of the loop-unrolled architecture and enables robust operation under process, voltage, and temperature variations.

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