A Scaling-Friendly Low-Power Small-Area ΔΣ ADC With VCO-Based Integrator and Intrinsic Mismatch Shaping Capability

Kyoungtae Lee, Yeonam Yoon, and Nan Sun, Member, IEEE

Abstract—This paper presents a first-order scaling-friendly VCO-based closed-loop ΔΣ ADC. It uses the VCO as both quantizer and integrator, and thus, obviates the need for power-hungry scaling-unfriendly OTAs and precision comparators. It arranges two VCOs in a differential manner, which cancels out even-order distortions. Most importantly, it has an inherit mismatch shaping capability that automatically addresses the DAC mismatches. The prototype ΔΣ ADC in 130 nm CMOS occupies a small area of only 0.03 mm² and achieves 66.5 dB SNDR over 2 MHz BW while sampling at 300 MHz and consuming 1.8 mW from a 1.2 V power supply. It can also operate with a low analog supply of 0.7 V and achieves 65.8 dB SNDR while consuming 1.1 mW.

Index Terms—Analog-to-digital converter (ADC), clocked averaging, continuous-time ΔΣ ADC, mismatch shaping, phase-domain analog signal processing, ring oscillator, time-domain ADC.

I. INTRODUCTION

C
ONVENTIONAL ΔΣ ADCs rely on the use of operational transconduction amplifiers (OTAs). This well-established design methodology may encounter difficulties in advanced nanometer-scale CMOS processes due to reduced power supply voltages and transistor intrinsic gains. First, since the analog signal is represented and processed in the voltage domain, a smaller power supply directly leads to a smaller signal swing and decreased dynamic range. Second, the conventional integrator depends on the high gain of the OTAs to guarantee precision and linearity. However, the required high gain is very hard to achieve with a small transistor intrinsic gain. A low power supply further increases the difficulty, as it prevents the use of gain boosting techniques that require stacking transistors vertically. Hence, in order to obtain the required voltage gain, long-channel transistors, large analog supplies, and multistage amplifier topologies have to be used, leading to significant performance penalties in chip power, area, and speed. In addition, the reduced power supply voltage also makes it harder to design a multibit quantizer. Its offset requirement becomes tougher to meet and the comparator metastability rate increases.

The advent of nanometer CMOS technology calls for a new design framework for multibit ΔΣ ADCs that not only do not suffer from reduced power supplies and transistor intrinsic gains, but actually take advantage of the strengths of CMOS scaling. One clear merit of CMOS scaling is that the transistor speed \( f_T \) keeps increasing and the logic delay keeps decreasing. Thus, it is highly desirable to process the analog signal in the time domain or phase domain.

There have been emerging efforts in the research community to use ring voltage-controlled oscillators (VCOs) to construct phase-domain ΔΣ ADCs [1]–[6], [15]. Ring VCOs provide intrinsic integration and quantization capability in the phase domain. Its natural integration from frequency to phase provides infinite gain at DC, which is better than conventional OTA-based integrators with only finite gain. Its phase is also naturally quantized, and thus, a multibit quantizer can be simply built by sampling the output nodes of a multistage ring VCO. There is no need to generate an array of evenly spaced comparison voltages. The metastability rate is also much lower [3], [4]. In addition, there are several other advantages for using VCOs to replace conventional integrator and multibit quantizer: 1) they contain only simple inverters, and thus, are easy to design; 2) they are area and power efficient; 3) they operate well under low power supply; and more importantly 4) they are scaling friendly. As technology advances, the inverter delay decreases and the timing resolution increases. As a result, the performance of VCO-based ΔΣ ADCs improves naturally with CMOS scaling.

Despite the many advantages mentioned above, VCO-based ΔΣ ADCs suffer from the VCO's nonlinear voltage-to-frequency conversion. Typically, the linearity of an open-loop VCO is limited to 6-bit or below 40 dB. To overcome this nonlinearity problem, several design techniques have been proposed. One way as shown in Fig. 1(a) is to use digital back-end calibration to correct the nonlinearity of the VCO [1], [2]. The merit of this scheme is that it is mostly digital, but the drawback is that it requires accurate replica matching, which is hard to guarantee under process, voltage, and temperature (PVT) variations. The other way to solve the VCO nonlinearity problem is to put the VCO in a closed loop with an analog filter \( H(s) \) preceding it [see Fig. 1(b)] [3]. The gain provided by \( H(s) \) helps suppress the VCO nonlinearity. Moreover, this scheme has an intrinsic dynamic element matching (DEM) capability. Due to the digital differentiation at the VCO output, the elements in the feedback DAC are naturally selected in

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The authors are with the Department of Electrical and Computer Engineering, University of Texas at Austin, Austin, TX 78712 USA (e-mail: kyoungtae.lee@utexas.edu; irunjunrun@utexas.edu; nansun@mail.utexas.edu). Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

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a barrel-shifted fashion, which implicitly implements data weighted averaging (DWA) [8]. As a result, the DAC mismatches are automatically shaped to the first-order. However, the disadvantage of this scheme is that the analog filter $H(s)$ is scaling unfriendly and consumes large power and area. In addition, because of the digital differentiation, the integration capability of the VCO is canceled out. As a result, the VCO, together with the differentiator, acts only as a quantizer, instead of an integrator. The overall transfer function gain from the VCO input to the ADC output is limited. Thus, the VCO input still sees a large signal swing, which results in large distortions and limits the overall ADC linearity. To address this issue, the authors of [4] propose to use the VCO phase, instead of its frequency, as the output [see Fig. 1(c)]. The VCO phase is measured by comparing it with a reference phase derived from the sampling clock. Since there is no differentiation in the loop, the VCO acts as an integrator, which increases the loop gain. The VCO input swing is substantially reduced, and thus, its nonlinearity problem is solved. The price for using this technique is that the intrinsic DEM capability is lost, as the VCO phase output is thermometer coded. To address the DAC mismatch problem, an explicit DEM block has to be used, which leads to additional design complexity, increased loop delay, as well as more power and area.

To simultaneously use the VCO as an integrator and maintain an intrinsic DEM capability, we propose a novel first-order VCO-based $\Delta \Sigma$ ADC architecture shown in Fig. 1(d). We arrange two VCOs in a differential manner. The phase output of the dual VCO is measured by comparing the phase of one VCO with that of the other. The advantage of this scheme is that the feedback loop operates only on the difference between the two VCO phases and does not control the VCO center frequency. As a result, unlike [4], the VCO center frequency does not have to be locked to a fraction of the sampling frequency; it can be freely chosen. As a result, we can lower the VCO frequency to save power and reduce phase noise [9]. More importantly, as will be explained in Section III-A, the proposed scheme results in a natural rotation of the DAC selection pattern with the speed of twice of the VCO center frequency. This effectively realizes the data-independent DEM scheme of clocked averaging (CLA) [10]. In other words, the proposed ADC architecture has an intrinsic CLA capability. CLA modulates the DAC mismatch errors to the twice of the VCO center frequency and moves them out of the signal band. As a result, no explicit DEM technique is needed. Furthermore, because the dual VCO is used as an integrator, it provides a large loop gain to suppress the VCO nonlinearity. Its pseudo-differential structure also helps cancel out even-order distortions. Additionally, a large number (e.g., 25) of VCO stages can be used to increase the effective phase quantizer resolution and further suppress the signal swing at the VCO input. As a result, the analog filter $H(s)$ is no longer needed from the linearity point of view.

The proposed $\Delta \Sigma$ ADC architecture does not need any analog filter, external DEM, or calibration. It is only comprised of VCOs, phase quantizers, and DACs. Thus, it is highly scaling friendly; it occupies a small area and consumes low power, especially in advanced processes. A prototype ADC implemented in 130 nm CMOS occupies an active area of only 0.03 mm$^2$. It achieves 66.5 dB SNDR over 2 MHz bandwidth (BW) while consuming only 1.8 mW from a 1.2 V power supply. It can also work with a low analog supply of 0.7 V and achieves 65.8 dB SNDR while consuming only 1.1 mW.

We have reported part of this work at conferences [11], [12]. However, due to page limitation, many important details and measurement results are omitted. The contribution of this paper is that it provides thorough analyses on the proposed ADC operation and covers all the key design considerations. This paper is organized as follows. Section II explains the proposed ADC's phase-domain operation. Section III discusses its intrinsic CLA and PWM behavior. Section IV presents the detailed circuit design. Section V shows the measurement results. The conclusion is in Section VI.

II. ADC PHASE DOMAIN OPERATION

In the proposed closed-loop $\Delta \Sigma$ ADC, the subtraction between the ADC input and the DAC output is realized in the cur-
Fig. 2. Three possible scenarios during initial ADC power up for 5-stage CCOs: (a) CCO1 leads CCO2 by $\pi/5$; (b) CCO1 leads CCO2 by $4\pi/5$; and (c) CCO1 lags CCO2 by $\pi/5$. $f_i$ and $\phi_i$ represent the frequency and the phase of CCO$_i$. DAC$_i$ represents the $i$th unit DAC element.

<table>
<thead>
<tr>
<th>CCO</th>
<th>Digital output</th>
<th>Current</th>
<th>Frequency</th>
<th>When loop is stable</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCO1</td>
<td>Increase</td>
<td>Decrease</td>
<td>Decrease</td>
<td>Always leads CCO2</td>
</tr>
<tr>
<td>CCO2</td>
<td>Increase</td>
<td>Increase</td>
<td>Decrease</td>
<td>Always lags CCO1</td>
</tr>
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</table>

Table I: Summary of the CCO operation assuming a DC input

The integration and quantization are realized by two ring oscillators in the phase domain. Since it is easier to view the ADC operation in the current domain, we consider the oscillators as current controlled oscillators (CCOs), even though it is also valid to view them as VCOs. The ADC digital output corresponds to phase difference between the two CCOs, which can be simply taken out by letting them refer to each other. In steady state, the feedback loop ensures that the center frequencies for the two CCOs are the same and their phase difference is proportional to the analog input $V_{in}$. If the ADC digital output $D_{out}$ increases, CCO1 current decreases while CCO2 current increases. The detailed relationship for the two CCOs are summarized in Table I.

To understand how the ADC works, let us first consider a zero input $V_{in} = 0$ and two 5-stage CCOs for simplicity. As shown in Fig. 2, the inner and outer loops are CCO1 and CCO2, respectively. The outputs of the two CCOs are compared with each other using XOR gates.

When inverters are not flipping, their inputs and outputs are opposite. Since there is an odd number (e.g., 5) of inverters in the VCO ring, one inverter must have the same input and output (both high or both low), and is in transition. This transitioning point indicates that the CCO phase has propagated to that inverter.

Note that an entire CCO period corresponds to going around the CCO ring twice. This is because an inverter’s output is flipped after only one transition. Two transitions are needed to return to the original state. Since one CCO period corresponds to the phase of $2\pi$, going around the CCO ring once means that the CCO phase has only propagated by $\pi$. Thus, the phase circle shown at the center of Fig. 2 corresponds to the CCO phase range from $-\pi/2$ to $\pi/2$, not from $-\pi$ to $\pi$. The DACs after the XOR gates are the feedback current-steering unary DAC elements [see Fig. 1(d)]. If the XOR output is 1, the corresponding unit DAC drains current away from CCO1, decreasing its frequency. By contrast, if XOR output is 0, it decreases CCO2 current and frequency.

When the ADC is initially powered up, the phase of the two CCOs are placed at random locations. There are three possible scenarios for the relationship between the initial phases of the two CCOs: 1) CCO1 leads CCO2 by less than $\pi/2$; 2) CCO1 leads CCO2 by more than $\pi/2$; and 3) CCO1 lags CCO2, which is an unstable situation, as the XOR-based phase detector has a negative gain.

Fig. 2(a) shows an example of case 1) where CCO1 leads CCO2 by $\pi/5$. The digital output $D_{out}$, which is the sum of all XOR outputs, is 1. Only DAC5 draws current from CCO1 while all other DAC elements draw current from CCO2. Thus, the CCO1 frequency is higher than that of CCO2. This makes CCO1 phase propagate faster than CCO2 phase. As a result, their phase difference increases until it reaches $\pi/2$, which is the steady state where $D_{out}$ oscillates between 2 and 3.

Fig. 2(b) illustrates case 2) where CCO1 leads the CCO2 by $4\pi/5$ and the digital output is 4. Since only DAC4 input is 0 and all other DAC inputs are 1, there is more current flowing through CCO2, making its frequency greater than that of CCO1. Thus, the phase difference decreases, and eventually, the loop also goes into the steady state where the phase difference of the two CCOs stays around $\pi/2$.

Fig. 2(c) corresponds to case 3) where CCO1 lags CCO2 by $\pi/5$. Only DAC4 input is 1 and all others’ inputs are 0. This means that the current flowing into CCO1 is higher than that for CCO2. Thus, CCO1 phase propagates faster than that of CCO2. After certain time, CCO1 phase catches up and surpasses CCO2.

1This may appear inconsistent with the convention that going around one cycle should be $2\pi$ instead of $\pi$. Note that here the phase label is referring to the global CCO phase instead of the CCO ring.
Fig. 3. Example phase domain operation for the proposed ADC with 25-stage CCOs and zero input.

Fig. 4. (a) Phase diagram of the proposed ADC with 25-stage CCOs and nonzero input; (b) example phase domain operations.

Each 1-bit DAC element $\Delta A_{n}$ can be mapped to a CCO phase. Assuming there are $N$ CCO stages and DAC elements, $\Delta A_{n}$ is mapped to the CCO phase of $(n-1)\pi/N$ for $n < N/2$ and $(n - N - 1)\pi/N$ for $n > N/2$. The input to $\Delta A_{n}$ is 1 if its corresponding phase is between the phases of CCO1 and CCO2. In our prototype ADC, each CCO consists of 25 stages. The phase diagram is shown in Fig. 3. As explained earlier, assuming $V_{n} = 0$ and the loop is in steady state, CCO1 leads CCO2 by $\pi/2$, and $D_{out}$ oscillates between 12 and 13.

We can consider CCO1 and CCO2 together as a dual CCO. Its common-mode phase $\phi_{center}$ is the center phase of the two CCOs, which propagates at the speed of $f_{center} = (f_1 + f_2)/2$ [see Fig. 4(a)]. Note that the ADC input does not change $\phi_{center}$ because the input current feeds into the two CCOs in a differential manner. When input changes, it speeds up one CCO but slows down the other. What varies with input is the phase difference between CCO1 and CCO2, or the differential-mode phase $\phi_{in} = \phi_1 - \phi_2$. Fig. 4(b) shows an example of the phase domain operation with a sinusoidal input. The CCO phase difference $\phi_{in}$ is proportional to the input, but its center phase $\phi_{center}$ propagates with a constant speed independent from the input.

At every clock cycle, $\phi_{in}$ is sampled and quantized, producing the ADC digital output. The understanding of the phase domain operation is critical for understanding the intrinsic DEM capability for the proposed CCO-based $\Delta \Sigma$ ADC.
III. INTRINSIC DAC MISMATCH SHAPING CAPABILITY

A. Intuitive Explanation

DAC mismatch is a major issue for multi-bit ΔΣ ADC. Since the mismatch error directly adds to the input, it can severely degrade the ADC linearity. To see this, we simulated a first-order ΔΣ ADC with a 25-element DAC selected in a thermometer-coded way. In the absence of mismatch, the SNDR at the oversampling ratio (OSR) of 75 is 80 dB. However, as shown in Fig. 5(a), the SNDR decreases to only 54 dB with 1% element mismatch. There are large in-band harmonic distortions.

The proposed ADC has an intrinsic CLA capability that effectively addresses the DAC mismatch issue without any hardware cost. One intuitive way to understand it is as follows. As discussed in Section II and shown in Fig. 4, the middle point of the DAC selection pattern corresponds to the dual CCO common-mode phase \( \phi_{\text{center}} \). Since one CCO period means going around the ring twice, the DAC middle point rotates at \( 2f_{\text{center}} \). This leads to the DAC selection pattern shown in Fig. 5(b), where we assume \( f_{\text{center}} = f_s/50 \). This selection pattern matches the behavior of the CLA technique [10]. The DAC mismatch errors are up-converted to \( 2nf_{\text{center}} \) and moved out of the signal band [see Fig. 5(b)]. Thus, the SNDR is significantly improved to 77 dB, which is only 3 dB lower than the ideal case with no mismatch. This intrinsic CLA allows the use of small DAC elements. It reduces the design complexity, shortens the excess loop delay, and saves chip area and power.

B. Comprehensive Analysis of Dual-CCO-Based Quantizer

The prior subsection intuitively explains the intrinsic CLA scheme. To understand it thoroughly, we need to investigate the behavior of the proposed dual-CCO phase quantizer, which is quite different from that of a conventional voltage-domain quantizer. For a DC input, the conventional quantizer always outputs a fixed value. By contrast, for the proposed phase quantizer, even if its equivalent quantizer input, which is the differential phase \( \phi_{\text{in}}(t) = \phi_1 - \phi_2 \), stays unchanged, its output oscillates between two adjacent levels. This is because the common-mode phase \( \phi_{\text{center}} = (\phi_1 + \phi_2)/2 \) constantly moves ahead at \( f_{\text{center}} \).

The proposed dual-CCO phase quantizer essentially performs a pulse width modulation (PWM) of its input \( \phi_{\text{in}}(t) \). To explain it clearly, let us examine the CCO phase dynamics shown in Fig. 4. The input to DAC1 (i.e., the output of the single-bit phase quantizer XOR1) is 1 when its corresponding phase, which is 0, is in between \( \pi/2 \) and \( \pi \). Mathematically speaking, this means

\[
\phi_1(t) = \phi_{\text{center}}(t) + \phi_{\text{in}}(t)/2 > 0 \quad (1)
\]

\[
\phi_2(t) = \phi_{\text{center}}(t) - \phi_{\text{in}}(t)/2 < 0 \quad (2)
\]

which combines into

\[
-\frac{1}{2}\phi_{\text{in}}(t) < \phi_{\text{center}}(t) < \frac{1}{2}\phi_{\text{in}}(t). \quad (3)
\]

The time domain waveforms for \( \phi_{\text{center}}(t) \) and \( \phi_{\text{in}}(t)/2 \) are plotted in Fig. 6(a). As explained in Section II, in steady state, \( \phi_1 \) always leads \( \phi_2 \), and their difference oscillates around \( \pi/2 \). Thus, \( \phi_{\text{in}}(t)/2 \) is centered around \( \pi/4 \) and is bounded by \( (0, \pi/2) \). The shaded region in Fig. 6(a) is where the inequality of (3) is satisfied, leading to DAC1 input being 1. This can be simplified to Fig. 6(b), in which \( +\phi_{\text{center}}(t) \) are merged into one triangular wave. The corresponding DAC1 input is in Fig. 6(c). It can be considered as the output of a comparator that compares \( \phi_{\text{in}}(t)/2 \) with the triangular wave. Such operations
For a PWM signal, its information is captured in the pulse width. Fig. 8 shows a simulated digital input of a single DAC element for a sinusoidal ADC input. Its spectrum is shown in Fig. 9. As is well known, PWM does not produce distortions in the signal band, but has tones around the carrier frequency and its higher order harmonics.

Other DAC elements operate in the same way as DAC1. For example, DAC2, whose corresponding CCO phase is \(\pi/25\), has an input of 1 when \(\phi_{\text{in}}(t)/2\) is greater than the same triangular wave but phase shifted by \(\pi/25\). Thus, we can build a voltage-domain model that accurately describes the behavior of the proposed ADC, which is shown in Fig. 10. Negative ports of the comparators are the phase shifted triangular waves. When 25 digital outputs are summed up, the up-converted PWM tones do not show up in the output spectrum assuming perfect matching in the CCO stages and DACs. This is because the PWM tones have the same magnitude but with evenly spaced phase offsets; their vector sum is 0. Nevertheless, because DAC elements have mismatches, the overall DAC output still has PWM tones, as shown earlier in Section III-A. However, there is no distortion in band due to the PWM behavior. Thus, as long as the up-converted tones are out of the signal band, the DAC mismatch issue is solved in the proposed ADC architecture. By contrast, in the ADC architecture of [4], since the \(f_{\text{center}}\) is locked to \(f_s/4\), the DAC middle point rotates at \(f_s/2\) in the DAC selection pattern. This means that the modulated DAC mismatch tones at \(4nf_{\text{center}}\) overlap at DC, leading to large in-band distortions and requiring an external DEM block to address the DAC mismatch errors.

### C. DAC Dynamic Error Analysis for CLA

In addition to the static mismatch error, another major error source for DAC is the dynamic switching error during DAC element transitions. Different from the static mismatch error, the dynamic switching error is present even for a single-bit DAC. It arises from clock feedthrough, clock skew, device parasitic capacitance, and memory effects. It can be considered as a form of inter-symbol-interference (ISI) [17]–[19].

In general, the amount of dynamic error is proportional to the DAC element transition rate. Thermometer coding has the smallest dynamic error due to its lowest transition rate, but it cannot handle the static mismatch error [17]. By contrast, DWA is effective at addressing the static mismatch error, but it has the largest dynamic error. Its DAC transition rate is the highest among all DEM techniques [18], [19]. This is because DWA generally turns off previous selected elements and turns on new ones. Moreover, its transition rate is highly dependent on the DAC input \(d\). It is easy to derive the average transition rate for DWA as (including both up (0 \(\rightarrow\) 1) and down (1 \(\rightarrow\) 0) transitions) [18]

\[
\tau_{\text{DWA}} = \begin{cases} 
2d \\
2 - 2d 
\end{cases} \quad \text{if} \; d \leq 0.5, \quad \text{if} \; d > 0.5.
\]

where \(\tau_{\text{DWA}}\) and \(d\) are normalized values in between 0 and 1. This relationship is plotted in Fig. 11. At \(d = 0.5\), during every clock cycle, half DAC elements are switched off and the rest are turned on. Thus, all DAC elements are in transition, leading to the peak \(\tau_{\text{DWA}} = 1\). The triangular relationship between \(\tau_{\text{DWA}}\)
and $d$ (see Fig. 11) leads to a large second-order distortion [20], [21]. As a result, DWA is hardly used in high-resolution continuous-time $\Delta \Sigma$ modulators. Instead of being a nonlinearity suppressor, it can act as a tone generator [17]–[19].

The proposed intrinsic CLA has much smaller DAC dynamic error compared to DWA. The reasons are as follows. First, its number of DAC element transitions is much fewer than that for DWA. As shown in Fig. 5(b), the intrinsic CLA keeps the majority of the DAC inputs unchanged. There are large overlaps between adjacent selected elements. Since the DAC element rotation speed is $2f_{\text{center}}$, and there are 2 transitions (1 up and 1 down) for each DAC element during every rotation, the average DAC element transition rate for CLA is given by (as long as the DAC input level is not too low or too large)

$$r_{\text{CLA}} = \frac{4f_{\text{center}}}{f_s}.$$  

(5)

Hence, having a small $f_{\text{center}}$ mitigates the dynamic error. The proposed ADC allows $f_{\text{center}}$ to be changed without affecting the feedback loop operation, and thus, we can decrease $f_{\text{center}}$ to reduce the dynamic error. For example, if we set $f_{\text{center}} = 4.5$ MHz and $f_s = 300$ MHz as in the prototype ADC, the DAC transition rate $r_{\text{CLA}}$ is only 6%, which is much smaller than $r_{\text{DWA}}$, as shown in Fig. 11. Furthermore, unlike DWA, $r_{\text{CLA}}$ does not depend on $d$. This leads to much smaller harmonic distortion. Note that although the average transition rate $r_{\text{CLA}}$ is input independent, its instantaneous number of DAC transitions is still input dependent. Thus, CLA cannot completely avoid dynamic error induced distortion. In practice, the relationship between the dynamic error and the instantaneous DAC transition rate is nonlinear. Thus, generally, it is preferred to lower the DAC element transition rate, so that not only the total amount of dynamic error but also its nonlinear portion are reduced.

The analyses above are confirmed via behavioral simulations in MATLAB. Fig. 12 shows the simulated ADC output spectra with 0.1% dynamic switching error. When DWA is used, there is a large second-order distortion, limiting the SFDR to only 67 dB. By contrast, when CLA is used, the in-band distortion is much smaller, which is due to its significantly reduced DAC transition rate and input dependence.

Fig. 11. Simulated DAC element transition density versus input level.

IV. PROPOSED ADC DESIGN AND ANALYSIS

A. Circuit Implementation

Fig. 13(a) shows the circuit implementation of the proposed ADC. The input voltage is converted to a current by a resistor $R_{\text{in}}$, which is placed off-chip for tunability. $R_{\text{in}}$ is chosen to be large enough (2.4 kΩ) so that it allows a large input swing of 2.4 V Vpp and contributes a small noise current. The input current flows into two 25-stage CCOs. Each delay cell consists of 4 inverters [see Fig. 13(b)]. The inner cross-coupled inverters, whose width is one third of that of the outer ones, ensure differential operation and a sharp transition edge. The replica buffers are used to isolate kickback noise from the comparators. Its schematic is similar to that of the delay cell except that it has a tail transistor with a fixed bias [see Fig. 13(c)]. The comparators, which adopt a two-stage topology for faster regeneration [see Fig. 13(d)], sample the output of the replica buffers. XORs then take the phase difference. The digital output feeds back to the input by a 25-element current-steering DAC. Most of the feedback DAC current are pulled from the CCO, assuming $R_{\text{in}}$ is large enough. The bias current to the CCOs and the feedback DAC is supplied by the PMOS current sources and the common-mode current through $R_{\text{in}}$.

Interestingly, if the CCO center frequency is set to be low enough to reduce its power consumption, the PMOS current sources are no longer required, and thus, all DC current needed by the DAC and CCOs can be supplied by $R_{\text{in}}$. In this case, since the CCO only requires a low voltage of 400 mV, the analog power supply can be lowered to 0.7 V. This bias setup will be referred to as the low-power mode. In this case, the ADC input common mode is set to 0.7 V, which is the analog power supply. This significantly reduces the analog power consumption. Being able to operate under a low power supply of 0.7 V is another merit for using CCOs to construct $\Delta \Sigma$ ADCs. The trade-off for using a 0.7 V analog supply is that to provide enough DC current, $R_{\text{in}}$ needs to be small, which reduces the input swing from 2.4 V Vpp to 0.95 V Vpp. A smaller $R_{\text{in}}$ leads to increased input referred noise current. It also reduces the amount of feedback DAC current going into the CCO, which lowers the loop gain. They together result in a slight degradation in the SNR (see the measurement result in Section V).

The reason for using current to control frequency is that it is more linear than using voltage, which is shown in the measured
CCO tuning curves of Fig. 14(a) and (b). A qualitative explanation is that there is a direct relationship between the CCO frequency and current. For a ring oscillator, its frequency is proportional to how fast charges move in and out of its internal nodes, which is directly related to the CCO current. When choosing the CCO center frequency, we want it to be small to reduce power and DAC dynamic error, but we also want it to be large enough so that: 1) the frequency tuning is linear; 2) the up-converted DAC mismatch errors are out of the signal band; and 3) the CCO input impedance, inversely proportional to [see Fig. 14(c)], is small enough to receive the majority of feedback DAC current. After balancing these tradeoffs, we set it to be around 4.5 MHz which leads to a low current consumption of 0.14 mA, a small control voltage of 400 mV, and the input impedance of 1 $k\Omega$. During the ADC testing, we set $f_{\text{center}}$ by adjusting the CCO current using the bias voltages of the PMOS current sources (see M1 to M4 in Fig. 13).

The effective quantizer resolution for a 25-stage CCO is 4.6-bit. The loop gain is proportional to the CCO current-to-frequency gain $K_c$ and the DAC current. The measured $K_c$ is about 200 GHz/A and the unit DAC current is 26 $\mu$A. This leads to an estimated SQNR of 78 dB at the OSR of 75.

### B. CCO Mismatch Analysis

Because the proposed ADC uses two CCOs, their mismatch may cause performance degradation. To focus our analysis on the CCO mismatch, let us assume that the ADC input is fully differential and the DAC elements are matched. Thus, the input current to the dual CCO is fully differential, and the CCO frequencies can be expressed as follows:

$$\begin{align*}
    f_1(t) &= f_{01} + K_1 \cdot i(t) + \epsilon_1 \cdot i^2(t) \\
    f_2(t) &= f_{02} - K_2 \cdot i(t) + \epsilon_2 \cdot i^2(t)
\end{align*}$$

where $f_{0j}$ ($j = 0, 1$) is the CCO center frequency, $K_j$ is the CCO current to frequency gain, $i(t)$ is the CCO current, and $\epsilon_j$ is the coefficient for the dominant second-order distortion. Thus, the differential mode frequency for the dual CCO is given by

$$f_d(t) = f_{01} - f_{02} + (K_1 + K_2)i(t) + (\epsilon_1 - \epsilon_2)i^2(t).$$

The mismatch in the CCO center frequency $f_{0j}$ and $f_{02}$ acts like an offset. It does not cause distortion, but it decreases the differential signal swing. However, as long as $f_{01}$ and $f_{02}$ are close, the signal swing attenuation is negligible. The variation in $K_1$ and $K_2$ only slightly changes the differential current to frequency gain. This does not cause distortion either. Since the proposed ADC is first-order, small variations in differential CCO gain have only minor effects on the overall ADC performance. The mismatch between $\epsilon_1$ and $\epsilon_2$ causes the imperfect cancelation of the second-order distortion. Nevertheless, as long as $\epsilon_1$ and $\epsilon_2$ match reasonably well, the majority of the second-order distortion is still canceled out, which is much better than using a single CCO without any distortion cancelation. Also, the ADC feedback loop minimizes $i(t)$. As a result, the proposed ADC architecture is reasonably robust against CCO mismatches. As shown in the measurement results (see Section V), without any CCO calibration, the ADC is able to
TABLE II

<table>
<thead>
<tr>
<th>Input referred current noise PSD (pA/√Hz)</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input resistors</td>
<td>3.7</td>
</tr>
<tr>
<td>PMOS current sources</td>
<td>6.9</td>
</tr>
<tr>
<td>Feedback DAC</td>
<td>6.6</td>
</tr>
<tr>
<td>CCOs</td>
<td>4.8</td>
</tr>
<tr>
<td>Total</td>
<td>11.3</td>
</tr>
</tbody>
</table>

achieve 73 dB SFDR while using small area VCO cells with large mismatches.

C. Thermal Noise Analysis

The thermal noise in the proposed ADC comes from four components: the input resistor, the bias current source, the feedback DAC, and the CCO. Since the circuit works in the current domain, it is more straightforward to compute input referred noise current. The power spectral density (PSD) of the noise current produced by the input resistor is given by $4kT/R$, and is computed to be $3.71 \text{ pA/√Hz}$ for two resistors. The bias PMOS current sources (see M1-M4 in Fig. 13) and the DAC current sources produce channel thermal noise whose PSD formula is $4kTg_m$. Their SPICE simulated values are $6.94 \text{ pA/√Hz}$ and $6.56 \text{ pA/√Hz}$, respectively.
For the CCO, its phase variance over one clock period \( T_s \) is given by

\[
\langle \phi_n^2 \rangle = 2DT_s
\]

where \( D \) is the phase diffusion constant and can be obtained from phase noise simulation [22]. To compute the input referred CCO noise current, we need to divide (8) by the overall gain from the CCO input current to the CCO phase propagation over one clock period, which is \( 2\pi K_c T_s \)

\[
\langle i_n^{2,\text{CCO}} \rangle = \frac{\langle \phi_n^2 \rangle}{(2\pi K_c T_s)^2}.
\]

Finally, using Parseval’s theorem, we can derive the PSD of the input referred CCO noise current

\[
\text{PSD}_{\text{CCO}} = \frac{\langle i_n^{2,\text{CCO}} \rangle}{L^2} = \frac{D}{\pi^2 K_c^2}.
\]

Based on the SPICE simulated \( D \) at \( f_{\text{center}} = 4.5 \) MHz, we calculate the dual CCO input referred noise current PSD to be 4.8 \( \mu \text{A}/\sqrt{\text{Hz}} \). It is well known that the CCO phase noise decreases as the CCO operating frequency decreases [9]. Therefore, this is another merit of the proposed dual-CCO based architecture where \( f_{\text{center}} \) can be decreased to minimize the phase noise.

Table II summarizes the thermal noise values. The total input referred current noise PSD is 11.3 \( \mu \text{A}/\sqrt{\text{Hz}} \), which translates to a thermal noise limited SNR of 83 dB assuming a 2 MHz signal bandwidth and a 2.4 V peak-to-peak differential input signal swing.

V. ADC MEASUREMENT RESULTS

A. Normal and Low-Power Mode Measurement Results

The prototype ADC is implemented in 0.13-\( \mu \text{m} \) CMOS process with an active area of only 0.03 \( \text{mm}^2 \) as shown in Fig. 13(c). The sampling frequency and the signal bandwidth are 300 MHz and 2 MHz, respectively. We choose the OSR of 75 to balance the trade-off between the signal bandwidth and the SNDR. Fig. 15 shows the measured time domain output waveform. The full digital output swing is from 0 to 25, as the CCO consists of 25 delay cells. There is an offset of about 2 LSB due to mismatches between the two CCOs.

Fig. 16 shows the ADC output spectrum in the normal mode with a 1.2 V analog power supply and a 0.9 dBFS 661.5 kHz input. The 20-dB/dec first-order noise shaping is clearly seen. There are tones centered around the CCO harmonics, which is the effect of the intrinsic CLA as explained in Section III. The hump at around 40 MHz is due to the excess loop delay [23] and the parasitic pole at the CCO input node [5], which alter the loop transfer function. The excess loop delay comes from the comparator, the XOR, and the DAC. It is about 20% of the clock period. It does not affect the in-band performance of the proposed \( \Delta \Sigma \) ADC as it is only first order. To simplify the circuit, we choose not to compensate the excess loop delay [24].
The measured SFDR of 73 dB is limited by the second-order distortion, which is likely due to DAC mismatches and CCO mismatches that cause imperfect cancelation of even order distortions. The measured SNDR and SNR are 66.5 dB and 68 dB, respectively. The in-band noise consists of quantization noise, thermal noise, DAC mismatch noise, and noise due to clock jitter and signal dependent comparator delay [23]. The main contributor is the DAC mismatch error. Based on the height of up-converted DAC mismatch tones, the estimated DAC element mismatch is about 2%, which by itself limits the SNR to about 71 dB. The DAC mismatch arises mainly from transistor variations, limited by the small unit DAC element area of only 6 μm by 4.5 μm.

The ADC output spectrum in the low-power mode with a 0.7 V analog power supply and a 0.9 dBFS 661.5 kHz input is shown in Fig. 17. SNDR slightly decreases to 65.8 dB for the reasons explained in Section IV, but the total power is reduced to 1.06 mW which includes the current supplied by the off-chip input resistor.

The measured SNDR and SNR with varying input amplitudes for both normal and low-power modes are shown in Fig. 18. It can be seen that the ADC maintains a good performance over a wide signal range. The peak SNDR is achieved at the input amplitude of −0.9 dBFS.

B. PSRR Measurement

Since the core of the ADC is a ring oscillator, a major concern is its power supply rejection ratio (PSRR). To test it, a 100-mV (−27.6 dBFS) 94.5 kHz sinusoidal signal is injected into the 1.2 V analog power supply. Fig. 19 shows the ADC output spectrum. A tone at 94.5 kHz with the amplitude of 67 dBFS (i.e., 1.1 mV when referred to the ADC input) is clearly seen. According to the convention, we define the PSRR as the amplitude ratio of the input tone injected at the supply over the detected tone at the ADC output, and thus, we compute the PSRR as

\[ \text{PSRR} = 67 - 27.6 = 39.4 \text{ dB}. \]  

This shows that the proposed ADC can attenuate power supply noise by around 100 times. Thus, it is reasonably robust against power supply noise. Even if there are 10-mV rms noise on the analog supply line, the SNDR degradation is negligible.

C. Experimental Studies of CLA

To experimentally study the intrinsic CLA behavior, \( f_{\text{in}} \) and \( f_{\text{center}} \) are varied. Fig. 20 shows the output spectra with varying \( f_{\text{in}} \) while keeping all other conditions the same. As \( f_{\text{in}} \) increases, the gap between the tones located near \( 2n f_{\text{center}} \) increases, but the gap size is always equal to \( f_{\text{in}} \). Fig. 21 shows the output spectra with varying \( f_{\text{center}} \). As expected, the frequencies of the PWM tones increase as \( f_{\text{center}} \) increases. These measured results match well with the PWM behavior, which firmly validates the analyses in Section III.

D. Performance Summary

In the normal mode, the measured analog power is 1.13 mW, which includes the CCOs, the DAC, the replica buffers, and the comparators. The measured digital power is 0.62 mW, which includes the XORs, flip-flops, and the thermometer-to-binary encoder. When operating in the low-power mode, the analog power drops to 0.45 mW. The corresponding Walden figure-of-merits (FOMs) with 1.2 V and 0.7 V analog power supplies are 0.25 pJ/conversion-step and 0.17 pJ/conversion-step, respectively. Table III compares this work with other VCO-based ΔΣ ADCs and recently published conventional ΔΣ ADCs. In terms of FOM, this work achieves the comparable performance especially considering its relatively old technology of 130 nm.
Because of its scaling friendly architecture, further substantial performance enhancement can be attained in more advanced CMOS processes.

Since the chip area is directly linked with cost, it is also an important metric. Fig. 22 shows the area and FOM for this work, cited works, and recently published (~2015) ΔΣ ADCs in ISSCC and VLSI conferences [41]. The red dots are for this work under both normal and low-power modes. The cited works are displayed as blue dots. This comparison result clearly shows that the prototype ADC is both power and area efficient given its old 130 nm process.

VI. CONCLUSION

The paper presented a scaling-friendly low-power small-area VCO-based ΔΣ ADC. It does not need OTA and precision comparators; instead, it uses ring oscillators as both integrator and quantizer. The proposed ADC also has an intrinsic DAC mismatch shaping capability. It represents a future trend for ΔΣ ADC design in the era of nanometer-scale CMOS processes. It takes advantage of the strength of CMOS scaling by processing analog information in the phase domain, and obviates the limitations of reduced transistor intrinsic gain and decreased power supply voltages. It is envisioned that the performance of the proposed ADC can be further substantially enhanced if implemented in advanced processes, such as 32 nm and beyond.

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REFERENCES


Kyoungtae Lee received the B.S. degree from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2011, and the M.S. degree from the University of Texas at Austin, Austin, TX, USA, in 2013.

From 2012 to 2013, he was a Graduate Technical Intern at Intel Corporation, Austin, TX, USA. He is currently working on developing the core technologies for fifth generation mobile communication system at KAIST Institute, Daejeon, South Korea.

His research interests include 5G cellular system, VCO-based delta sigma ADCs, and biosensors.

Yeonam Yoon received the B.S. and M.S. degrees from Seoul National University, Seoul, South Korea, in 2004 and 2008, respectively. His master research topic was on the small-signal modeling of RF CMOS.

He joined the Electrical and Computer Engineering Department, University of Texas at Austin, Austin, TX, USA, as a Ph.D. degree student in Fall 2011.

He worked as a circuit designer and test engineer for Samsung Electronics for three years from 2008. His current research focuses on VCO-based delta sigma ADCs.

Nan Sun (M’11) received the B.S. degree from Tsinghua University, Beijing, China, in 2006, where he ranked top in his major, and the Ph.D. degree from Harvard University, Cambridge, MA, USA, in 2010.

He is an Assistant Professor at the University of Texas at Austin, Austin, TX, USA. His research interests include: 1) analog, mixed-signal, and RF integrated circuits; 2) miniature spin resonance systems; 3) magnetic sensors; 4) developing micro- and nanoscale solid-state platforms (silicon ICs and beyond) to analyze biological systems for biotechnology and medicine.

Dr. Sun is the recipient of Samsung Fellowship, Hewlett Packard Fellowship, and Analog Devices Outstanding Student Designer Award in 2003, 2006, and 2007. He won Harvard Teaching Award three times from 2008 to 2010. He also received NSF Career Award in 2013.