A 174.3dB FoM VCO-Based CT $\Delta\Sigma$ Modulator with a Fully Digital Phase Extended Quantizer and Tri-Level Resistor DAC in 130nm CMOS

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Abstract—This paper presents a high dynamic range (DR), power efficient VCO-based continuous time $\Delta\Sigma$ modulator (CTDSM). It introduces a simple, robust and low power fully digital phase extended quantizer (PEQ) that doubles the VCO quantizer resolution compared to conventional XOR-based phase detector with minimum overhead. A tri-level resistor DAC is also introduced as complementary to the new quantizer, enabling high DR while creating a dynamic power saving mechanism for the proposed design. Fabricated in 130nm CMOS, the ADC achieved peak Schreier FoM of 174.3dB with a high DR of 89dB over 0.4MHz BW, consuming only 1mW under 1.2 V power supply. It also reaches a peak Walden FoM of 59fJ/conv with 74.7dB SNDR over 2MHz BW.

Keywords—CTDSM, Time Domain, VCO-based ADC, Phase Detector

I. INTRODUCTION

Time domain signal processing has been regarded as a promising candidate for the next-generation ADC technique due to its scaling-friendly nature. For instance, utilizing the natural frequency-phase integration one can implement an integrator with ring VCO. Such integrator provides infinite DC gain with little headroom and device intrinsic gain limitation, bringing great benefit to $\Delta\Sigma$ modulators (DSMs) design in advance processes. Nevertheless, the large voltage to frequency non-linearity of the VCO posted major challenge for VCO-based DSM design. Open loop architecture proposed in [1] [2] tackled this issue with digital calibration, but the effectiveness relied on the replica path matching. Some design chose to embed the VCO inside a conventional $\Delta\Sigma$ loop and used phase as output [3] [4]. They minimized VCO input swing, thus achieving high linearity without calibration, but in turn required explicit DEM and occupied large area in order to suppress the non-idealities from the feedback DACs. Another close loop design that used 2 VCOs serving as the reference to each other not only minimized the VCO input swing, but also implemented the intrinsic clocked averaged (CLA) based DEM [5]. However, using dual-VCO doubled the number of flip flops in the sampler, limiting the power benefit. Also, though CLA desensitizes DAC mismatch, it raises the noise floor and degrades DR when large DAC mismatch presents. Another recent work [6] combined both phase and frequency as output, relaxes the power and linearity trade off.

This paper proposes a close loop continuous time VCO-based DSM featuring a novel, purely digital phase extended quantizer (PEQ). It uses simple combinatorial logic gates to extract the lead-lag information of the dual-VCO. The lead-lag information is subsequently used to increase the resolution of the VCO quantizer by 1 bit. Therefore, this PEQ effectively eliminates the sampler power overhead due to the excessive flip flops in [5], restoring the power benefit of VCO-based DSM. Since the proposed PEQ is purely digital, it is highly compatible with advance processes and the merits of time domain signal processing.

The proposed work also highlights the use of a tri-level resistor DAC (RDAC). RDAC exhibits superior matching and low noise performance compared to standard current steering DAC (IDAC) while occupying smaller area, enabling us to reach high DR performance. Though the output impedance of RDAC is reduced, it only brings slight and tolerable compromise to the loop gain. On top of that, the RDAC proposed in this work is designed with a tri-level control that specifically facilitates the output pattern of the PEQ. The combination of the PEQ and tri-level RDAC creates a dynamic power saving mechanism that automatically reduces the power consumption when input activity is low.

The paper is organized as follows. Section II introduces the proposed extended phase detection scheme used in this ADC. Section III presents the circuit implementation and its measurement results will be discussed in Section IV. Conclusion of the proposed work is brought up in Section V.

II. EXTENDED PHASE DETECTION SCHEME

A. Proposed Phase Extended Quantizer

Conventional VCO-based DSMs used XOR phase detector (PD) for its simplicity, but the lead-lag status between the VCO and reference is lost as XOR only acts as a level comparator. In other words, XOR PD only outputs the absolute value of the phase difference. If the lead-lag status can as well be utilized, it can essentially double the resolution without extra VCO stages, leading to great power efficiency. Lead-lag detection is conventionally implemented by the phase-frequency detector (PFD). However, due to the state-machine nature of the PFD, we discovered that incorrect state
cancellation would occur when being used in the sampler, as the sampling nature of an ADC will occasionally corrupt the continuum of the phase edges propagation. It also harms the loop gain. Therefore, in this work we proposed an improved lead-leg detection scheme, which is inspired from the PFD, but implemented as an extension of the XOR PD with only combinatorial components. Compared to PFD, our pure scheme is highly robust and has fewer trade-offs when being used in DSMs.

Fig. 1 illustrates the phase extension mechanism in this proposed work. The graph shows a simplified schematic of a multi-phase dual-VCO ring sampler along with XOR PD, similar to the one used in [5]. The numbers represent the logic level of the gates at an arbitrary sampling instant. Due to the nature of ring VCO, the XOR PD always produces a barrel-level of the gates at an arbitrary sampling instant. Due to the cell will source current from the feedback point. Therefore, in this work we proposed an improved lead-leg detection scheme, which is inspired from the PFD. When an XOR output is low, the corresponding DAC cell will drain current to the feedback point. When an XOR output is high, its corresponding DAC cell will source current from the feedback point. Therefore, in the conventional XOR PD bi-level control scheme, a DAC cell is always activated in either sourcing or draining state, regardless of the input activity. As a result, the DAC array consumes constant amount of current.

In addition to the power saving in DAC, the elimination of the static phase error in the PEQ also reduce the number of element transitions between samples at low input. This in fact

On the other hand, under the proposed phase extended detection scheme, we can reinterpret the DAC cell control in a tri-level fashion, which can be illustrated in Fig. 2(b). In the tri-level control scheme, a DAC cell is only activated when the corresponding XOR output is high, with its current direction guided by the sign bit, i.e. the lead-lag. When an XOR is low, it deactivates its DAC cell. Under the tri-level control scheme, the number of activated DAC cells is thus signal dependent. And this is a key property for the dynamic power saving. In a well-designed fully differential loop with no offset, when there is no input, the loop will try settling down at the mid-point of its linear range to achieve feedback symmetry. Hence, in conventional XOR PD, as shown in Fig. 1(b), a static phase error of \( \pi/2 \) is required to sustain its loop dynamic, whereas in the proposed PEQ, the static phase error is eliminated. The resulting PD output patterns for the conventional and proposed scheme are thus quite different. An example of the PD output pattern with -20 dBFS input for both scheme is shown in Fig. 3. It can be seen that very few DAC cells are needed to be activated under the PEQ scheme when input is low. If we can implement a tri-level DAC that burns very low power in the inactive state, the DAC power consumption can be minimized when input is inactive, resulting in dynamic power saving. In this proposed work, we chose to use resistor DAC over conventional IDAC, not only because it offers better matching and noise, but also because it does not require keeping the current source on at the inactive state compared to the IDAC counterpart, which truly brings out the benefit of dynamic power saving.

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lowers the switching activity in the retiming latch and DAC driver, maximizing the dynamic power saving by lowering the digital power in these parts.

III. PROPOSED ADC DESIGN

The schematic of the proposed VCO-based CTDSM is shown in Fig. 4(a). The dual-VCO phase output architecture is adopted. It provides superior forward path linearity due to minimum VCO input swing, as well from the cancellation of 2nd order non-linearity. This architecture also features intrinsic CLA that shuffles the DAC cell selection to desensitize DAC mismatch. As shown in Fig. 4(a), the differential input voltage is first turned into current by R_in and subtracted by the DAC current before being fed into two 15-stage current-starved VCOs, or simply CCOs. The CCO delay cell is pseudo differential as shown in Fig. 4(b), which gives us better Sense amplifier flip flops (SAFF) kick-back noise immunity. The CCOs performs current-frequency translation as well as the inherent frequency to phase integration. SAFFs sample each node of the CCOs. The sampled phases of the 2 CCOs are then processed by the PEQ to quantize the phase difference as thermometer code (D[14:0]), and importantly, extracting the lead-lag status (SIGN). The quantized phase difference is then multiplied with the SIGN to generate tri-level controls (S+1, S-1, S_0) that governs the tri-level RDAC operation.

The detail implementation of the PEQ is also shown in the highlighted area of Fig. 4(a). XOR1 serves as the conventional PD, which outputs the magnitude of the phase difference. An additional XOR2 is inserted between adjacent CCO_P nodes to detect the transition point (TP1). Adjacent XOR1 outputs are also fed to AND1 to detect the front edge (FE) of D[14:0]. TP1 and FE are then checked for alignment through AND2, as previously described in Fig. 1. When there is alignment between TP1 and FE, AND2 will produce a bit stream that contains a logic ‘1’ (essentially a one-hot code), where the ‘1’ location indicates the alignment point. If there is no alignment between TP1 and FE, AND2 will produce a string that has only logic ‘0’. We then use a one-hot adder, which is simply OR-logic to check whether the AND2 output contains logic ‘1’ and produce the lead-lag indicator SIGN. In this proposed work, when CCO_P leads CCO_N, SIGN is designated high, and vice versa. The Tri-Level Gen block is then combines the PD output and SIGN to create DAC control signal.

Schematic of the tri-level RDAC is presented in Fig. 4(c). The shunt capacitors (C_P, C_N) across the resistors in the RDAC provides desensitization for the CCO input parasitic pole. There are two highlights for this RDAC. The first is that resistors exhibit excellent matching over FETs. From Monte-Carlo we confirmed that the mismatch standard deviation for resistors is 5X smaller than FETs with similar size. It also produces lower noise due to the passive nature. These 2 features offer our work high linearity and dynamic range, proven by test results. Yet another highlight is that, as mentioned previously, at low input activity most of the DAC cells are inactive due to lack of static phase error. Thus most of the DAC cells have a high S_0 and its resistors are connected to V_CM. The other side of the resistor also see similar voltage from the summing node (VCTRL). Hence, little static current is consumed at this state. The RDAC only draws current as input gets more active, giving the proposed work the ability of dynamic power saving according the input activity.

IV. MEASUREMENT RESULTS

The proposed work was fabricated in 130nm 1P8M CMOS process and occupied an active area of 0.13 mm^2 (Fig. 5). Running at 250MS/s, it consumes 1.05mW under 1.2V with full input signal swing, out of which 0.78mW is from digital. The measured output PSD is shown in Fig. 6 for 100kHz, 300kHz and 500kHz tones respectively. SFDR is over 84 dB across different input cases, demonstrating high linearity. The SNDR and SNR vs input magnitude plot for 3 different BWs is shown in Fig. 7. Due to dynamic power saving, the total power drops to 0.6mW when input is inactive, as shown in Fig. 8(a). As shown in Fig. 8(b), a peak Walden FoM of 59fJ/conv with SNDR of 74.7dB is achieved at 2MHz. The best DR performance is obtained at 0.4MHz BW. We are able to reach 88.5dB DR and achieve 174.3dB Schreier FoM. To the authors’ best knowledge, it outperforms all existing VCO based ΔΣ ADCs despite the relatively old 130nm process. We strongly believe that the scaling-friendly nature will bring
substantial performance improvement for our ADC in advanced processes.

![Fig. 5. Chip die photo (left) and layout (right)](image)

over prior arts. A prototype chip was fabricated in 130 nm technology, with solid measurement result demonstrating high performance brought by the proposed techniques. The scaling-friendly and dynamic power saving nature of the proposed ADC makes it a very good candidate for future mobile application in advanced technology nodes.

![Fig. 8. (a) Power vs. input magnitude. (b) Measured FoM vs. BW.](image)

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**REFERENCES**


