A 12b-ENOB 61μW Noise-Shaping SAR ADC with a Passive Integrator

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Abstract—This paper presents a novel noise shaping SAR architecture that is simple, robust and low power. It is fully passive and only needs minor modification to a conventional SAR ADC. Through a passive integrator, quantization noise, comparator noise and DAC noise are shaped with a noise transfer function of \((1 - 0.75z^{-1})\). Unlike conventional multi-bit delta-sigma ADCs, both the noise transfer function and the error transfer function of DAC mismatches are immune to process-voltage-temperature variations. A prototype chip is fabricated in a 0.13μm CMOS process. At 1.2V and 2MS/s, the chip consumes 61µW power. SNDR increases by 6dB and the Schreier FoM increases by 3dB with OSR doubled. At an OSR of 8, SNDR is 74dB and the Schreier FoM is 167dB.

I. INTRODUCTION

For medium-resolution applications, successive approximation register (SAR) ADC is of great popularity due to its high power efficiency in nanometer technology. However, as the target resolution goes beyond 10-bit, its efficiency quickly diminishes due to its tight requirement on comparator noise. Moreover, the exponentially increasing capacitor DAC array not only costs large chip area and power, but also makes it difficult to drive. For high-resolution application, delta-sigma (ΔΣ) ADC is a more widely-used architecture. Taking advantage of oversampling and noise shaping, it can use a low-resolution quantizer to reach high resolution. Nevertheless, its realization usually requires OTA-based active integrators which are power hungry and scaling unfriendly. This has motivated the development of voltage-controlled oscillators (VCO)-based ΔΣ ADCs that use VCO as integrators [1]–[3]. However, VCO performs a voltage-to-phase/frequency conversion, which is nonlinear and sensitive to process-voltage-temperature (PVT) variations.

Recently, there have been emerging efforts in the research community trying to develop hybrid ADC architectures that combine the merits of SAR and ΔΣ ADCs [4], [5]. The first noise-shaping (NS) SAR ADC is published in [4], but it still needs an OTA to realize a \(1^{\text{st}}\)-order noise transfer function (NTF) zero at 0.64. It also requires a FIR DAC that introduces extra noise and increases chip area. Later, a fully-passive \(1^{\text{st}}\)-order NS SAR ADC is published in [5]. It obviates the need for any OTA, but its noise-shaping performance is very limited, as its NTF zero is located at 0.5 rather than 1. Moreover, its input signal is attenuated by 2 times during normal conversion, leading to the 6-dB penalty in SNR or quadrupled analog power for the same SNR. In addition, it requires 2-time more capacitance, increasing chip area.

Fig. 1. NTF magnitude comparisons with zeros from [4], [5] and this work.

This paper proposes a novel NS SAR architecture that is simple, robust, and low power. It gets rid of the OTA-based active integrators and realizes a NTF zero at 0.75 with a passive integrator. The passive integrator only requires one switch and two capacitors. The zero location is fully determined by the capacitor ratio, which is insensitive to PVT variations and ensures the robustness of the architecture. Compared to [4] \((z = 0.64)\) and [5] \((z = 0.5)\), the proposed NS SAR ADC achieves the best noise shaping performance with a zero closest to 1. Fig. 1 compares the NTF magnitude with zeros from [4], [5] and this work. As can be seen, this work achieves around 3dB more in-band attenuation than [4] and 6dB more in-band attenuation than [5]. Furthermore, the proposed architecture does not cause any signal attenuation, and requires less capacitance than [5]. With minimum modification to the original SAR ADC architecture, the proposed NS SAR ADC altogether shapes the quantization noise, comparator noise, and DAC noise with a NTF of \((1 - 0.75z^{-1})\). It allows the use of a low-resolution DAC and relaxes the requirement on comparator noise, making it possible to reach high-resolution and high-power efficiency simultaneously.

To demonstrate the proposed NS SAR ADC, the paper is organized as follows. Section II introduces the circuit architecture. Section III analyzes the detailed signal flow diagram and its non-ideal effects. Section IV presents the chip measurement results. Finally, Section V draws the conclusion.
II. CIRCUIT ARCHITECTURE

Fig. 2 shows the architecture of the proposed 1st-order NS SAR ADC. Compared to conventional SAR operations, two more clock cycles, \( \phi_{ns0} \) and \( \phi_{ns1} \), are added. Before \( \phi_{ns0} \) cycle, the SAR ADC does the normal conversion. Different from [5], there is no capacitor connected to \( V_{res} \) node during normal conversion, and thus, the signal attenuation problem is avoided. To realize 1st-order noise shaping, the key is to integrate the residual voltage \( V_{res} \) and feed it back to the comparator input.

During \( \phi_{ns0} \) cycle, a small capacitor, \( C_2 = C/3 \), is merged with the DAC capacitor, \( C_1 = C \), to get the residue voltage, \( V_{res} \). At the end of \( \phi_{ns0} \) cycle, \( C_2 \) will carry \( 0.75V_{res} \). In the following \( \phi_{ns1} \) cycle, \( C_2 \) dumps its charge onto another capacitor, \( C_3 = C \), effectively realizing a passive integration. The voltage integrated on \( C_3 \) is labelled as \( V_{int} \), which is fed back to the comparator input. Now the comparator has 2-path inputs, one of which is connected to \( V_{res} \) while the other is connected to \( V_{int} \). However, there is a limitation with passive integration that only a fraction of \( V_{res} \) is integrated, which degrades the noise shaping performance. It seems that OTAs are still required to provide a gain to compensate the attenuation of \( V_{res} \). Fortunately, as the comparators result is a 1-bit sign, what is required here is only a relative gain between \( V_{int} \) and \( V_{res} \), which can be realized by simply sizing the comparator input transistors correspondingly. As shown in Fig. 2, to provide a gain of 4 on \( V_{int} \) path for a proper NTF, we size its corresponding input transistors 4 times larger than the \( V_{res} \) path. After \( \phi_{ns1} \) cycle, the charge on \( C_2 \) is cleared in next \( \phi_{ns} \) cycle to be ready for getting the new residual voltage. In real implementation, a mode signal is used to pull down \( V_{int} \) to ground so that the SAR ADC can be easily reconfigured to the conventional mode in case of Nyquist-rate applications. Additionally, foreground calibration on DAC mismatch can also be conducted in the Nyquist mode.

III. ANALYSIS

To provide a better understanding of the proposed NS SAR architecture, Fig. 3 shows the general signal flow diagram assuming \( C_1 = C_3 = C \), \( C_2 = a/(1-a)C \), and the integration path gain of \( g \). As can be seen from the derived NTF in \( D_{out} \) equation, there is a zero located at \( (1-a) \) and a pole located at \( (1-a)(1-ga) \). When \( g = 1/a \), the pole is gone and only
left is the zero. In this design, we choose \( a = 1/4 \) and \( g = 4 \), realizing a NTF of \((1 - 0.75z^{-1})\). With \( a = 1/4 \), \( C_2 \) value is \( C/3 \) and consequently only 4/3 times more capacitors are required for the 1st-order NS. Note that the NTF is completely set by component ratios \( a \) and \( g \), and thus, is insensitive to PVT variations. To ensure stability, the pole needs to be within the unit circle. The stability condition is shown in Fig. 3. Given that the current stability condition is \( 4/3 < g < 28/3, g = 4 \) determined by the comparator input transistor ratio is very far from the unstable boundary. Therefore, the proposed NS SAR architecture is highly robust.

With \( g = 1/a \), Fig. 4 further investigates the non-ideal effects including thermal noises and DAC mismatch errors in the flow. \( n_1 \) is the \( kT/C \) sampling noise which directly adds to the input signal. \( n_2 \) is the noise voltage on \( C_2 \) at the end of \( \phi_{n_{so}} \) while \( n_3 \) is the noise voltage on \( C_3 \) at the end of \( \phi_{n_{s1}} \). Fig. 4 also shows the noise power for \( n_2 \) and \( n_3 \). With \( a = 1/4 \), \( n_2 = 9kT/4C \) and \( n_3 = kT/4C \). As shown in the \( D_{out} \) equation, \( n_1, n_2, \) and \( n_3 \) directly pass through without being shaped while the comparator noise \( n_4 \), the DAC noise \( n_5 \), and the quantization noise \( Q \) added at the same location are altogether shaped to the 1st-order.

Another interesting merit of the proposed NS SAR ADC is its simplified digital DAC mismatch calibration. For conventional multi-bit \( \Delta \Sigma \) ADCs, in order to completely remove the DAC mismatch error in the digital domain, we need to accurately extract not only the DAC mismatch percentage but also the DAC mismatch error transfer function (ETF), as the ETF may not be exactly 1 due to PVT variations. As a result, special techniques such as inserting a binary pseudo-random test signal [6] are required to measure the ETF. By contrast, the ETF in the NS SAR ADC is always 1 for any NTF under any PVT variation. The key reason is that the quantizer and the feedback DAC use the same capacitor array in a NS SAR ADC. It is different from conventional multi-bit \( \Delta \Sigma \) ADCs whose DAC and quantizer are unrelated. As shown in Fig. 4, \( \varepsilon_1 \) represents the quantizer error due to capacitor mismatch, and \( \varepsilon_2 \) represents the feedback mismatch error. Since they are from the same origin in the NS SAR, it is easy to derive that \( \varepsilon_2(z) = -\varepsilon_1(z) \). As a result, the ETF is 1 regardless of the values of \( a \) and \( g \) (see the eqn. in Fig. 4). Even though there exist capacitor mismatches, it is equivalent to a NS SAR that uses a non-binary DAC array. As long as the capacitor mismatches are estimated, we can fully remove them in the digital domain. In this design, we reconfigure the NS ADC in the conventional Nyquist SAR mode at first and apply classic foreground calibration techniques [7] to estimate the DAC mismatch errors.

### IV. CHIP MEASUREMENT RESULTS

As a proof of concept, a prototype 1st-order NS SAR ADC is fabricated in a 0.13\( \mu \)m CMOS process. Fig. 5 shows its die photo and layout. The core area is 0.13mm\(^2\). The DAC array capacitor \( C_1 \) is 10-bit with a total capacitance of 2.1pF\( \times \)2 and a unit MOM capacitor of 2fF. The passive integrator capacitors \( C_2 \) and \( C_3 \) are implemented using high-density MIM capacitors so that they consume much less area than \( C_1 \) (see Fig. 5). The sampling frequency is 2MS/s. At 1.2V supply, the chip consumes 60\( \mu \)W power. 63% of the total power comes from the clock generation and the SAR logic, which are fully digital and can be greatly reduced with the CMOS scaling. With a 95.37KHz, -2dBFS sinusoidal input, the measured output spectrum is shown in Fig. 6. At an OSR of 8, SNDR and SFDR are 74dB and 95dB, respectively. Fig. 7 shows the measured SNR/SNDR with different input
amplitudes. Fig. 8 shows the measured SNDR/Schreier FoM ($FoM_S$) trend with different OSRs. As shown in Fig. 8(a), with OSR doubled, $FoM_S$ increases by 6dB which matches the NTF of $(1 − 0.75z^{−1})$. Therefore, according to $FoM_S = SNDR + 10\log_{10}(BW/Power)$, the $FoM_S$ increases by 3dB with OSR doubled. As shown in Fig. 8(b), when OSR is 8, the chip achieves a $FoM_S$ of 167 dB.

![Fig. 8. With different OSRs: (a) Measured SNDR and (b) Schreier FoM.](image)

PVT variations and highly robust. Compared to prior NS SAR ADC works, it gives the best noise shaping performance with a zero close to 1. A 0.13&mu;m CMOS prototype chip achieves the highest ENOB and the best Schreier FoM.

**TABLE I**

Comparisons between the proposed work and previous NS SAR ADC works.

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture</td>
<td>Need OTA</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td>Need FIR filter</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td>Signal attenuation</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td>NTF zero location</td>
<td>0.64</td>
<td>0.5</td>
</tr>
<tr>
<td>Chip performance</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Technology (nm)</td>
<td>65</td>
<td>65</td>
<td>130</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>1.2</td>
<td>0.8</td>
<td>1.2</td>
</tr>
<tr>
<td>Bandwidth (MHz)</td>
<td>11</td>
<td>6.25</td>
<td>0.125</td>
</tr>
<tr>
<td>Power (µW)</td>
<td>806</td>
<td>120.7</td>
<td>64</td>
</tr>
<tr>
<td>ENOB (bit)</td>
<td>10</td>
<td>9.35</td>
<td>12</td>
</tr>
<tr>
<td>FoM$_S$ (dB)</td>
<td>163</td>
<td>165</td>
<td>167</td>
</tr>
</tbody>
</table>

$FoM_S = SNDR + 10\log_{10}(BW/Power)$

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**REFERENCES**


