Proposal - “ITC’99” Benchmarks

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Background

• ISCAS’85 and ‘89 benchmarks pushed ATPG, DFT research
• Now badly outdated - too simple, too small.
• University research hampered by lack of real examples.

Proposal

• Collect a new set of realistic circuits
• Release in early 1999.
• Presentations of results at ITC ‘99.

Got Circuits? Let me know (don’t send any yet!)
Circuit Characteristics

- Embedded RAM, ROM, CAM - single and multiport.
- Embedded cores.
- Multiple clock domains - synchronized and unsynchronized.
- Internal tristate busses
- Bidirectional I/O
- Boundary scan
- Mixed FF/latch designs - falling and rising edges.
- Pass gate muxes
- Dynamic Logic
- Critical paths to constrain DFT.