# 3rd Annual
# Austin Conference on Integrated Systems & Circuits
# 2008 Publication

| KEYNOTE ADDRESS<br>**Dr. Necip Sayiner,**<br>***President, CEO, and Board Member***<br>***Silicon Laboratories*** | |
|---|---|
| Track 1:<br>DIGITAL DESIGN-1<br>**Session Chair:**<br>***Mike Seningen*** | Track 2:<br>ANALOG/BIO<br>**Session Chair:**<br>***Ka Leung*** |
| 1-1<br>Design Automation and Verification Methodology Challenges of the Intel Atom Processor<br>***Rajesh Gupta*** | ***2-1***<br>***Invited Paper:***<br>Biosensor Microarrays in CMOS<br>***Arjang Hassibi*** |
| 1-2<br>Reducing Flip-Flop Power for DSP Design<br>***Bassam Mohd,*** *Martin Saint-Laurent****, Paul Bassett, and Shahid Imam*** | 2-2<br>Rail to Rail Fully Differential Sample and Hold Based on Clocked Diffrential Difference Amplifier using Resistive Local Common Mode Feedback<br>***Jaime Ramirez-Angulo, Clara Lujan-Martinez, Carlos Rubia-Marcos, Ramon G. Carvajal, and Antonio Lopez-Martin*** |
| 1-3<br>Adaptive Voltage Tuning for Dual-Vdd ASICs<br>***Stephen Bijansky and Adnan Aziz*** | 2-3<br>Buck-Boost Converter Based Power Conditioning Circuit for Low Excitation Vibrational Energy Harvesting<br>***Arvindh Rajasekaran, Abhiman Hande, and Dinesh Bhatia*** |
| Track 3:<br>CAD-1<br>**Session Chair:**<br>***Michael Solka*** | Track 4:<br>COMPUTER ARITHMETIC<br>**Session Chair:**<br>***Earl Swartzlander*** |
| 3-1<br>Modeling of NBTI-Induced PMOS Degradation under Arbitrary Dynamic Temperature Variation<br>***Bin Zhang and Michael Orshansky*** | ***4-1***<br>***Invited Paper:***<br>Automated Multiplier Design<br>***K'Andrea C. Bickerstaff and Earl Swartzlander*** |

| | |
|---|---|
| 3-2<br>ELIAD: Efficient Lithography Aware Detailed Router with Compact Post-OPC Printability Prediction<br>***Minsik Cho, Kun Yuan, Yongchan Ban, and David Z. Pan*** | 4-2<br>Full Adder Evaluation and Selection for a Parallel Multiplier<br>***Mike Spear, Gaurav Tuteja, and Earl Swartzlander*** |
| 3-3<br>COOLER - A Fast Multiobjective Fixed-Outline Thermal Floorplanner<br>***Debarshi Chatterjee, Theodore Manikas, and Igor Markov*** | 4-3<br>Dual Vdd Design Optimization of Fast Multipliers<br>***Eun Jung Jang, Earl Swartzlander, and Jebediah Keefe*** |
| 3-4<br>Dynamic Compaction with Recursive Learning for Delay Test<br>***Zheng Wang and Duncan M. H. Walker*** | 4-4<br>A Hybrid Approach to Last Stage Addition for Wallace and Dadda Multipliers<br>***James Haydn Nelson, Eiman Ebrahimi, Mahnaz Sadoughi, and Earl Swartzlander*** |
| TUTORIAL<br>Fractional-N PLL<br>***Dr. Axel Thomsen,***<br>***Silicon Labs*** | |
| KEYNOTE ADDRESS<br>**Dr. Jason Rhode,**<br>***President and CEO***<br>***Cirrus Logic*** | |
| Track 5:<br>DIGITAL DESIGN-2<br>**Session Chair:**<br>***Adnan Aziz*** | Track 6:<br>ANALOG AND RF<br>**Session Chair:**<br>***TR Viswanathan*** |
| ***5-1***<br>***Invited Paper:***<br>A Sub 1W to 2W Low Power IA Processor for Mobile Internet Devices in 45nm Hi-K Metal Gate CMOS<br>***Gianfranco Gerosa, Steve Curtis, Mike D'Addeo, Bo Jiang, Belliappa Kuttanna, Feroze Merchant, Binta Patel, Mohammed Taufique, Haytham Samarchi, and Christopher Weaver*** | ***6-1***<br>***Invited Paper:***<br>Receivers Design: Case Studies<br>***Hesam Amir-Aslanzadeh and Edgar Sanchez-Sinencio*** |
| 5-2<br>A High Speed 128-Point Fast Fourier Transform Circuit for OFDM Systems<br>***Tung-Yeh Wu and Jacob Abraham*** | 6-2<br>Feed-Forward Interference Suppression for Broadband Systems<br>***Xin Wang and Ranjit Gharpurey*** |

| | |
|---|---|
| 5-3<br>Hardware Trojan Modeling and Detection Techniques<br>***Daniel G. Saab, Fatih Kocan, and Jacob Abraham*** | 6-3<br>A Linear Transconductor using Series-Connected CMOS Quad<br>***Venkatesh Acharya, Bhaskar Banerjee, and TR*** *Viswanathan* |
| ***5-4***<br>***Invited Paper:***<br>Migration of<br>Cell Broadband Engine<br>from 65nm SOI to 45nm SOI<br>***Osamu Takahashi***<br>***(Scott Cottier presenting)*** | 6-4<br>Indirect Compensation Techniques for Three-Stage CMOS Op-Amps<br>***Vishal Saxena, Jacob Baker, and TR Viswanathan*** |
| Track 7:<br>CAD-2<br>**Session Chair:**<br>***Michael Orshansky*** | Track 8:<br>SYSTEMS & ARCHITECTURES<br>**Session Chair:**<br>***Mattan Erez*** |
| 7-1<br>3D Resistance Extraction with Lithographic and Scattering Effect<br>***Ying Zhou, Zhuo Li, and Weiping Shi*** | 8-1<br>Power Analysis of a Path-Based Perception Branch Predictor<br>***Justin Friesenhahn, Lizy Kurian John, and Mark McDermott*** |
| 7-2<br>Accelerating Statistical Static Timing Analysis using Graphics Processing Units<br>***Kanupriya Gulati and Sunil Khatri*** | 8-2<br>Hardware / Software Tradeoffs in Multicore Architectures<br>***Steven Guccione*** |
| 7-3<br>Autonomous Optical Proximity Correction: The New Frontier of Design for Manufacturing?<br>***Shanhu Shen, Peng Yu, and David Z. Pan*** | 8-3<br>Workload Slicing for Detailed Pre-Silicon Power Estimation<br>***Hassan Al-Sukhni, James Holt, David Lindberg, and Michele Reese*** |
| TUTORIAL<br>Holistic Coupling of Manufacturing and Design<br>***Dr. Sani Nassif,***<br>**IBM** | |
| TUTORIAL<br>Out of Order Superscalar Architecture<br>***Dr. Derek Chiou,***<br>**University of Texas at Austin** | |
| TUTORIAL<br>Constraint Solving for Functional Verification<br>***Dr. Andreas Kuhlmann,***<br>**Cadence Berkeley Labs** | |

# Rail to Rail Fully Differential Sample and Hold Based on Clocked Differential Difference Amplifier Using Resistive Local Common Mode Feedback

*J. Ramirez-Angulo[1], C. I. Lujan-Martinez[2], C.Rubia-Marcos[2], R.G. Carvajal[2] and A. Lopez-Martin[3]*

[1]Klipsch School of Electrical and Computer Engineering, New Mexico State University, Las Cruces, NM USA [2]University of Seville, Seville, Spain [3]Public University of Navarra, Pamplona, Spain

*Abstract.* An efficient clocked class AB fully differential rail to rail differential difference amplifier is introduced. It is based on a two stage operational amplifier architecture with resistive local common mode feedback and uses floating gate transistors in the input stages and in the common mode feedback network. Its application in fully differential rail to rail high performance sample and hold circuit is discussed. Other applications discussed include fully differential buffers and single ended to fully differential converters with enable input. Experimental results of a test chip prototype fabricated in 0.5µm CMOS technology validate the proposed scheme. The fabricated sample and hold has an SFDR=70DB with a with a clock frequency of 5MHz and $1V_{pp}$, 1MHz input signals.

## I. Introduction.

Differential Difference Amplifiers (DDA) [1]-[2] are versatile analog building blocks with a host of applications in analog signal processing. For example in CMOS line drivers [3]. A DDA can be considered an extension of the conventional op-amp with two differential inputs instead of one (Fig. 1). In a DDA with negative feedback the op-amp virtual short circuit rule ($V_d$=0) is replaced by the more general expression $V_{d1}+V_{d2}=0$ (where $V_{d1}$, $V_{d2}$ are the two differential input voltages, see Figs. 1a,b). Fully differential DDAs (denoted here FD-DDAs) as well as generalized (universal) op-amps with n differential weighted inputs have been also reported [4],[5]. An FD-DDA has two differential input stages (Fig. 1b) with equal voltage gain $A_1$ .Their outputs are connected in parallel. They share a common output stage with gain $A_2$. The common output voltage of the first stages $V_{dx}$ is given by $V_{dx}=A_1(V_{d1}+V_{d2})$. The output voltage of the FD-DDA is given by $V_o=A_1A_2(V_{d1}+V_{d2})= A_{ol}(V_{d1}+V_{d2})$. Negative feedback with large open loop gain $A_{ol}=A_1A_2$ leads to the condition indicated above $V_{d1}+V_{d2} = 0$. To the present no rail no rail DDA or FD-DDA implementations have been reported. In this paper we propose a clocked rail to rail FD-DDA that uses resistive local resistive local common mode feedback [6]-[7] to achieve class AB operation. It also uses the floating gate technique reported in [8]-[10] to achieve rail to rail input/output signal swing and to implement a rail to rail continuous-time common mode capacitive sensing network. Fig. 1c shows the symbol of the proposed clocked DDA. It has two additional terminals used to apply non overlapping clock signals phi and $phi_{no}$. Fig. 1d shows the internal structure of the proposed clocked FD-DDA (CFD-DDA) that includes six switches. Two pairs of

switches are controlled by phi and connect the output of the first stage ($V_{dx}$) to the input of the second stage and the output of the second stage to the CFD-DDA output terminals respectively. The remaining two switches are controlled by $phi_{no}$ and connect the output of the first stage to an AC ground. We discuss the application of the CFD-DDA for the implementation of high performance rail to rail track and hold, sample and hold circuits, fully differential buffers and single ended to fully differential converters with enable inputs.

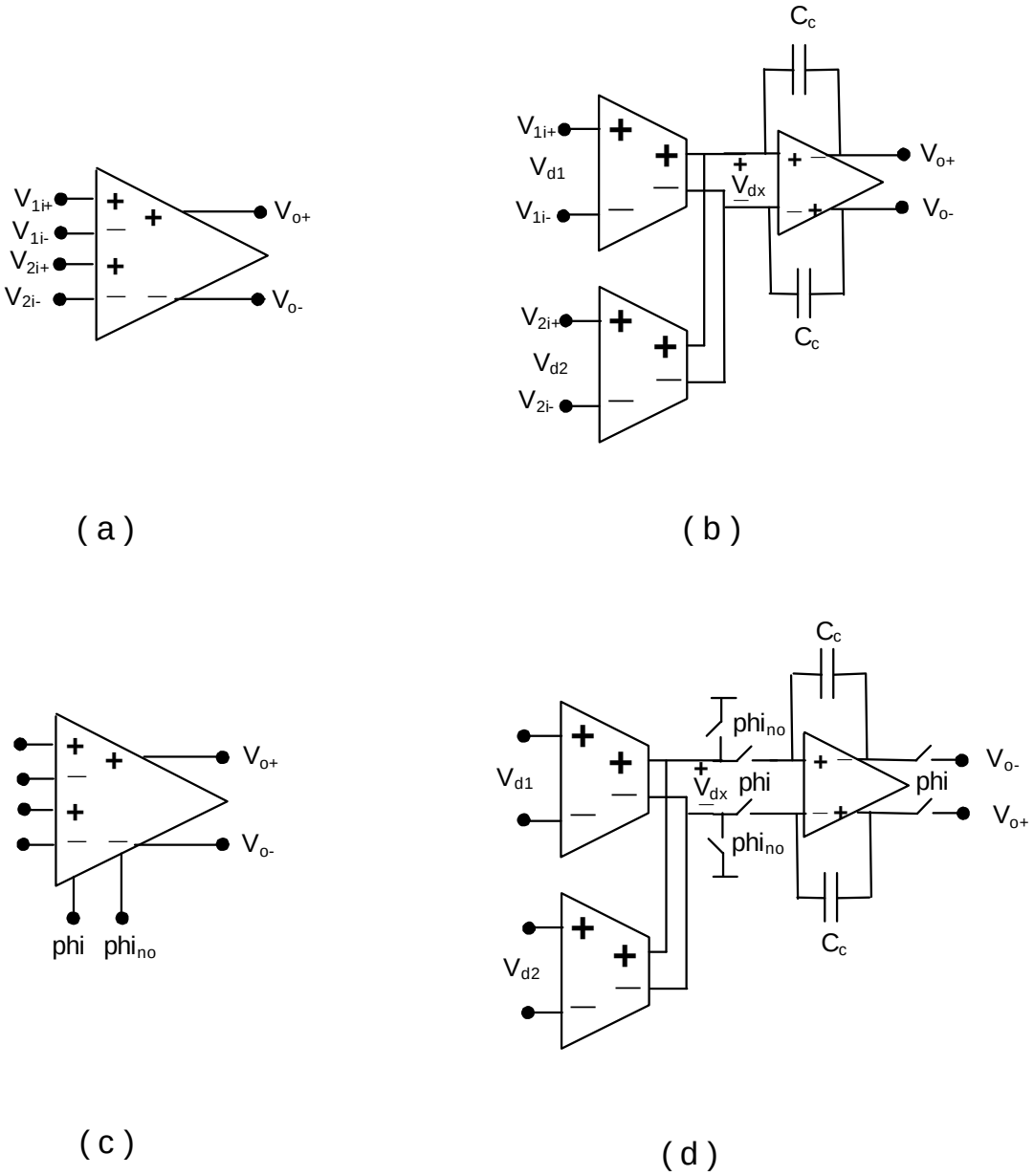



Fig. 1 Fully differential difference amplifier (FD-DDA) (a) Symbol, (b) Internal structure. (c) Clocked Fully Differential DDA or CFD-DDA(d) Internal structure of CFD-DDA

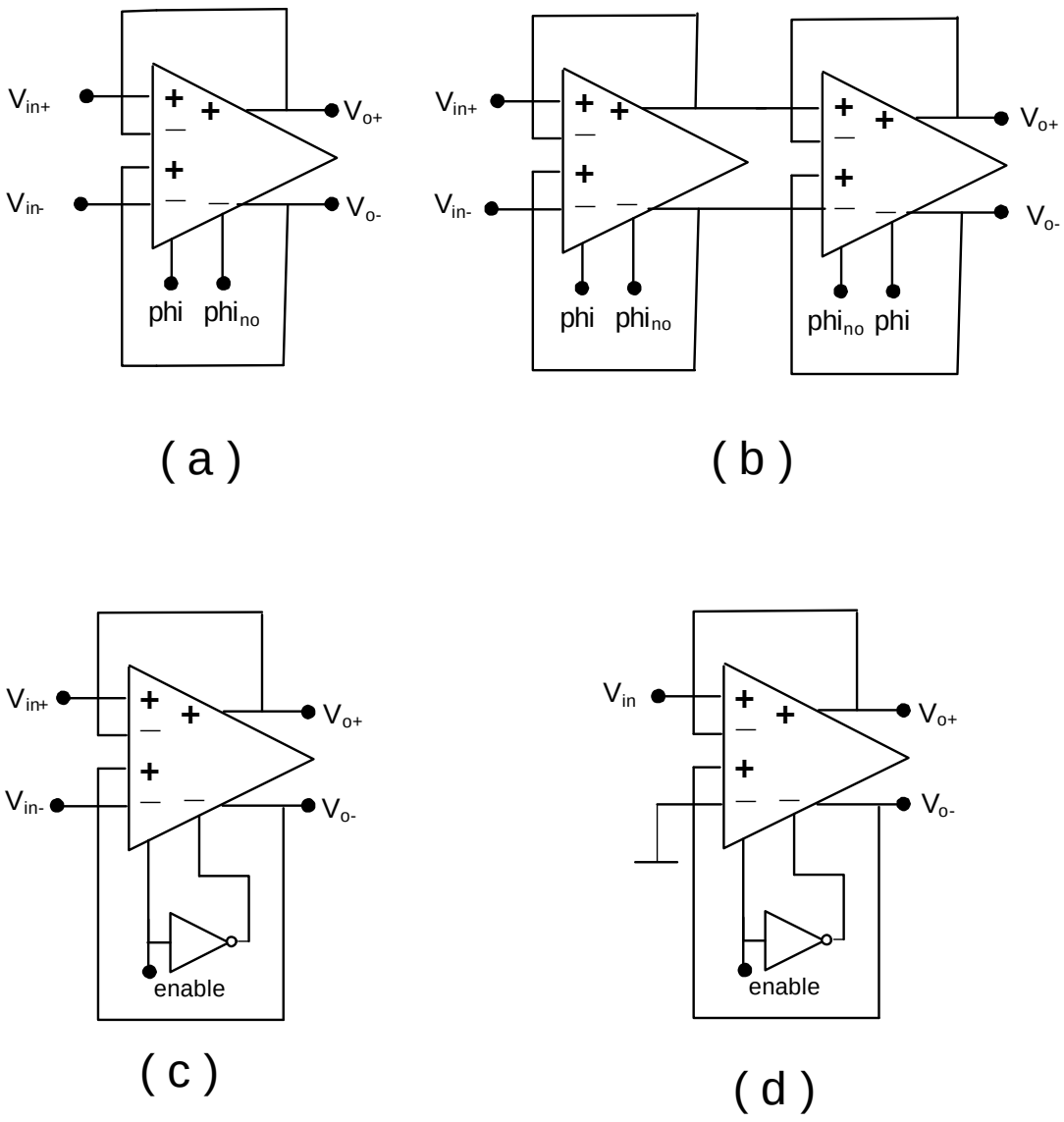



Fig. 2 Applications of Clocked Fully Differential Difference Amplifier (CFD-DDA): (a) Track and hold amplifier (b) Sample and Hold amplifier (c) Fully differential buffer with enable (d) Single ended to differential converter enable

## II. Clocked Fully differential DDA

*2.1 Operation* Fig. 3 shows the implementation of the clocked fully differential DDA. Floating gate transistors M1-M2 and M3-M4 form two differential pairs (amplifiers $A_1$) that generate current signals $i_I = (g_m V_{d1})/2$ and $i_{II} = (g_m V_d)/2$ respectively Their outputs are

connected in parallel to common nodes A and B Resistors R form a resistive local common mode feedback network [7] that has zero current under quiescent conditions ($V_{d1}=V_{d2}=0$, $V_X=V_A-V_B=0$) and generates equal quiescent voltages at nodes A,B and Y with values $V_Y=V_A=V_B=V_{DD}-V_{SG5,6.}$ Where $V_{SG5,6}$ is the quiescent source-gate voltage of M5-M6. These transistors have always a constant current Ib and a constant gate voltage $V_Y$. Upon application of differential signals $V_{d1}$, $V_{d2}$ currents $i_I=(g_mV_{d1})/2$ and $i_{II}=(gmV_{d2})/2$ are generated in M1-M2 and M3-M4 respectively ($g_m$ is the transconductance gain of M1-M4). The division by factor 2 is due to the attenuation of the capacitive divider at the input of the floating gate transistors. These capacitive dividers use two equal valued capacitors C at the input of each floating gate transistors in M1-M4.(Fig. 3c) This divider has two purposes: a) by connecting one of the inputs of the divider to the upper rail $V_{DD}$ the DC quiescent gate voltage of M1-M4 is shifted in the positive direction and increases the headroom for the differential pairs. b) it attenuates the differential signals $V_{d1}$ and $V_{d2}$. The combined effect of a) and b) allows input rail to rail to rail operation with low supply voltages according to the technique reported in [8]-[10]. Signals $V_{d1}$ and $V_{d2}$ generate complementary signal voltages $v_A=(i_I-i_{II})R$, $v_B=-(i_I-i_{II})R$ at nodes A and B while node Y remains at a constant voltage $V_Y = V_{DD}-V_{SG5,6}$ The differential voltage $v_X=v_A-v_B=2(i_I-i_{II})R \| r_{o5,6} =A_1(V_{d1}+V_{d2})$ is applied to the output stage formed by M7-M9 and M8-M10. This stage has a gain $A_2= g_{m7,8}\, r_{o7,8}\| r_{o9,10.}$ As reported in [6] the complementary and large signal swing at nodes A and B caused by the local common mode feedback network .provides class AB operation to the output stage. This is due to the fact that the swing at A and B is only limited by the upper rail $V_{DD}$. This allows output transistors to generate signal currents which are essentially larger than their quiescent current and provides high slew rate to the CFD-DDA. In order to operate as a sample and hold and buffer as discussed in section 3, the common mode sensing network must be able to operate also with rail to rail output signals. Fig. 3b shows a rail to rail continuous time capacitive common-mode feedback network proposed in [10] and used in the CFD-DDA. It senses the common mode output voltage using a capacitive divider formed by the capacitors C at the input of the floating gate transistors $V_{oCM}=(V_{o+} + V_{o-})/2$. This voltage is compared to the reference value $V_{refCM}$ and a signal $V_{cntCM}$ proportional to the difference $V_{oCM}-V_{refCM}$ is generated. The control signal is applied at the gates of M9,M10 and sets the output common mode voltage to the reference value $V_{refCM}$ . Rail to rail operation of the output common mode sensing circuit is based on the same principle discussed above. The circuit of Fig. 3 can operate with rail to rail signals and a single supply voltages $V_{DD}=V_{TPMOS}+4V_{DSsat}$ The gain bandwidth product of the DDA is given by the same expression as a two stage amplifier $GBW=(1/4\pi)(g_{m1}/C_C)$. The additional attenuation factor of 2 is due to the capacitive dividers at the input of M1-M4

*2.2 Slew Rate Analysis.* Slew rate is determined by the maximum gate source voltage of M7,8, which happens when the current through resistors R is maximum. This maximum current is $I_B$. For a large input step voltage,

$$V_{SG7,8}^{\max} = V_{SG5,6}^{Q} + RI_B = |V_{THP}| + \sqrt{\frac{2I_B}{\beta_{5,6}}} + RI_B$$

Assuming output transistors M7,8 are scaled a factor 2 larger than transistors M5,6 the maximum output current is given

$$I_o^{\max} = \frac{\beta_{7,8}}{2}\left(V_{SG7,8}^{\max} - |V_{THP}|\right)^2 = \frac{\beta_{7,8}}{2}\left(\sqrt{\frac{2I_B}{\beta_{5,6}}} + RI_B\right)^2$$

$$= \frac{\beta_{7,8}}{\beta_{5,6}} I_B\left(1 + R\sqrt{\frac{\beta_{5,6} I_B}{2}}\right)^2 = 2I_B\left(1 + R\sqrt{\frac{\beta_{5,6} I_B}{2}}\right)^2$$

and the slew rate is given by $SR = I_{oMax}/(C_c+C_L)$

*2.3 Remarks on CMRR and offset compensation.* Local common mode feedback provides high CMRR to the CFD-DDA. Due to symmetry, the effective load for common mode signals is relatively low and given by $R_{LCM}=1/g_{m5,6}$ while the effective load for differential signals is relatively high and given by $R_{Ld}=R||r_{o5,6} \sim r_o/2$. CMRR can be show to be given by

$$CMRR=(g_{m1,2}R||r_{o5,6})(g_{m5,6}\,2r_{bias}).$$

Where $r_{bias}$ is the impedance of the current biasing source $I_b$.

Offset compensation can be included in the CFD-DDA by adding to capacitors $C_{os}$ between node A (B) and switches S1,S3 (S2,S4).(see Fig. 4) These capacitors would store an amplified version $A_1V_{os}$ of the input offset voltage $V_{os}$ during the hold phase.$phi_{no}$ Offset would be compensated by the voltage stored capacitors $C_{os}$ during the sampling phase phi

## 3. Applications of CFD-DDA

*3.1Track and Hold and Sample and Hold amplifiers.* The circuit of Fig. 3 has the pairs of switches. They are controlled by non-overlapping clock phases phi and $phi_{no}$ respectively. The switches are used to operate the circuit of Fig. 3 as a Track and Hold amplifier as illustrated in Fig. 2a. In this application nodes A and B are connected to the gates of M7 and M8 during phase phi. Two external switches establish global negative feedback by connecting the outputs of the CFD-DDA to their inputs (Fig. 3a). In this phase the signals at nodes A and B are amplified by the second stage providing the circuit with a large open loop gain so that the DDA rule $V_{d1}+V_{d2}=0$ is satisfied. This causes the output differential voltage to follow the input differential voltage: $V_o=V_{in}$. During the non-overlapping phase $phi_{no}$ the external switches are turned off and gates of M7 and M8 are disconnected from nodes A and B so that the output voltage of the previous phase is held in the compensation capacitors Cc. In this phase nodes A and B are connected to node Y. This bypasses resistors R and prevents nodes A and B from saturating which otherwise would slow down the operation of the circuit. Clock injection at the gates of M7 and M8 caused by turning off switches S1 and S2 is approximately equal and signal independent. Clock injection introduces an approximately equal offset error at both positive and negative outputs ($V_{o+}$ and $V_{o-}$) and does not introduce an error in the differential output

voltage $V_o=V_{o+} - V_{o-}$ during the hold phase $phi_{no}$. A sample and hold amplifier can be implemented by connecting in cascade two track and hold amplifiers with complementary control signals as shown in Fig. 2b. This technique is in a similar line to the single ended sample and hold based on a two stage op-amp [10]

*3.2 Fully differential buffers and single ended to differential and differential to single ended converters.* Fig. 2c and 2d show the application of the CFD-DDA as a low voltage rail to rail fully differential buffer and as single ended to differential converter with enable input. Terminals phi and phino can be used as enable inputs (with enable signals phi=Vdd, $phi_{no}$=Vss). In this case the global feedback and connection of the output of the first stage to the input of the second stage is enabled and the rule $V_{d1}+V_{d2}=0$ applies. This leads to $V_{d1}=V_{d2}=0$ or equivalently to $V_{o+}=V_{in+}$ , $V_o-=V_{in-}$ or $V_o=V_{in}$ in the case of the fully differential buffer. In the case of the single ended to fully differential buffered converter it leads to $V_{o+}=-V_{in}/2$, $V_{o-}=V_{in}/2$ and $V_o=V_{in}$ (with $V_{d1}=V_{in}/2$ and $V_{d2}=-V_{in}/2$). A simple reconnection (not shown for the sake of space) allows the same circuit to be used as a differential to single ended buffered converter.

3.3 *Considerations for implementation of the CFD-DDA in deep submicrometer CMOS technology.* The blocks described above can be very useful in low-voltage fully differential analog signal processing. Their two stage architecture, class AB operation with rail to rail characteristics and low supply requirements make them specially attractive for applications in deep submicrometer CMOS technologies that uses single supply voltages close to 1V. In these technologies the amplifier gain has a strong dependence on the drain-source voltage [12]-[13]. Small drain source voltages lead to low gains and for this reason conventional cascode architectures that operate with low $V_{DS}$ on each transistor (like the folded cascode or telescopic op-amp) can not achieve high gain. This makes two stage architectures like that in Fig. 3 (where output transistors can have high $V_{DS}$) attractive to achieve high open loop gain. As example consider typical 90nm CMOS technology with $V_{TPMOS}\approx V_{TNMOS}\approx 0.35V$, $V_{DSsat}=0.1V$. In this case operation with high slew rate can achieved with a single supply $V_{DD}=1V$. Output switches can be replaced by straight connections and gate leakage can be compensated for by including two additional switches that connect (refresh) the gates of M1-M4 to $V_{DD}$ (or some other bias voltage) during $phi_{no}$.

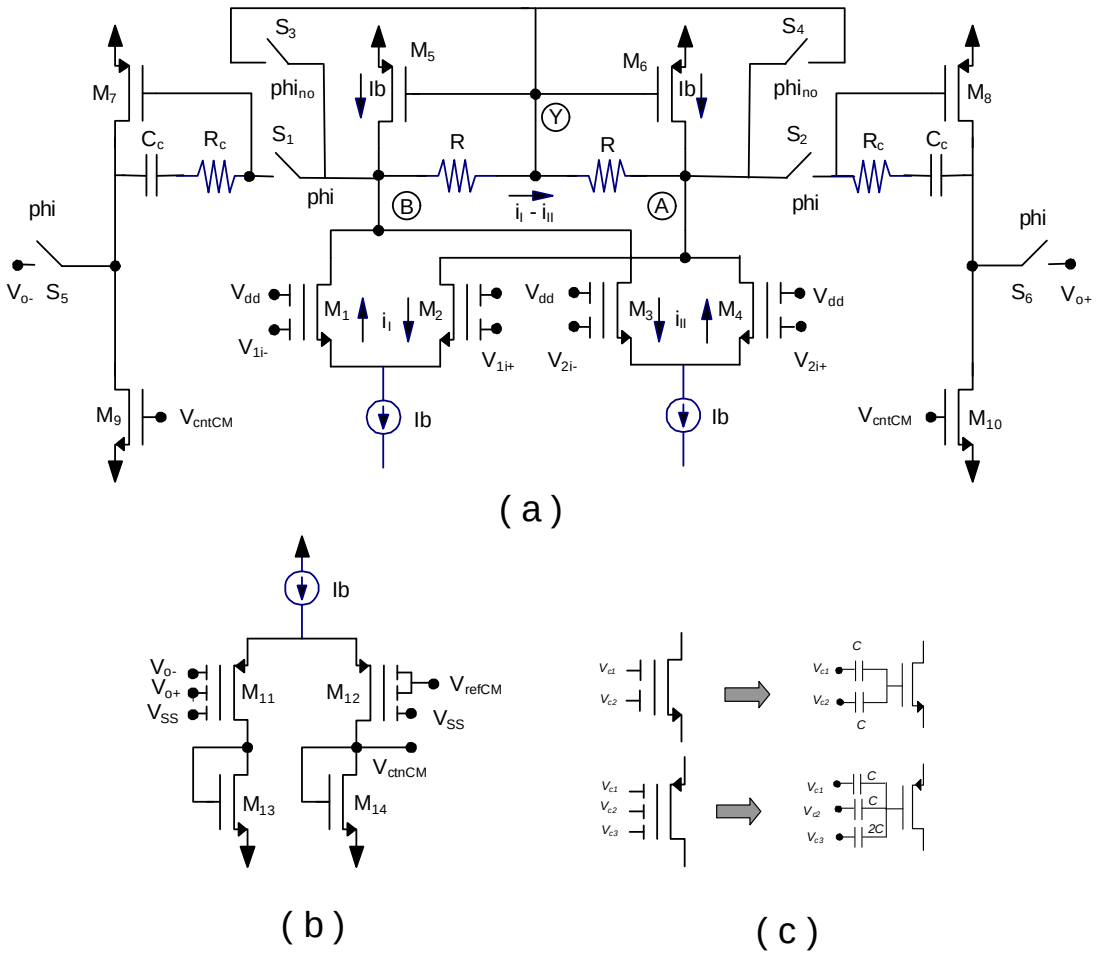



Fig. 3 (a) Rail to rail two stage fully differential difference amplifier using local resistive common mode feedback, (b) Rail to rail capacitive Common mode feedback network (c) Symbols and equivalent circuits of 2 and 3 input floating gate transistors

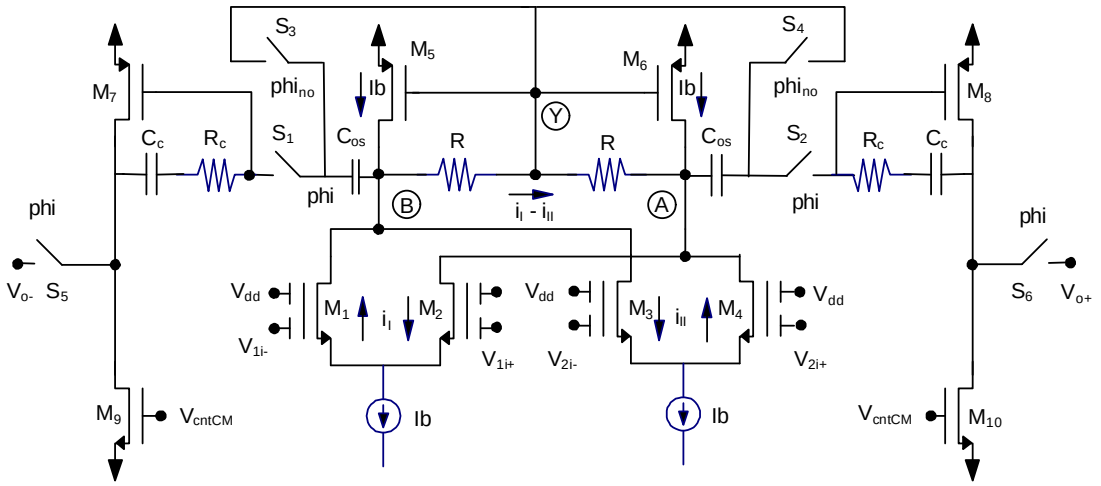



Fig. 4 CFD-DDA with offset compensation capacitors $C_{os}$ at output of first stage

## 4. Experimental results

A test chip prototype of the circuit of Fig. 3 was fabricated in the MOSIS available 0.5µm CMOS technology with following transistors sizes M1-M4:M13-M14 W/L=50/1, M5-M8, M13-M14: W/L=240/1 bottom biasing current sourcesW/L=50/1 M11-M12: top biasing current source W/L=120/1 M9-M10: W/L=100/1, R=50kΩ, $R_C$=1.5kΩ, C=1pF, Cc=5pF, $C_L$=70pF. It had only one clock input terminal and included a conventional circuit to generate non overlapping clocks phi and $phi_{no}$ from the external clock [12]. Fig. 5 shows a micrograph of the fabricated chip. The circuit was tested with $V_{DD}$=1.1V, $V_{SS}$=-1.1V, Ib=200µA.

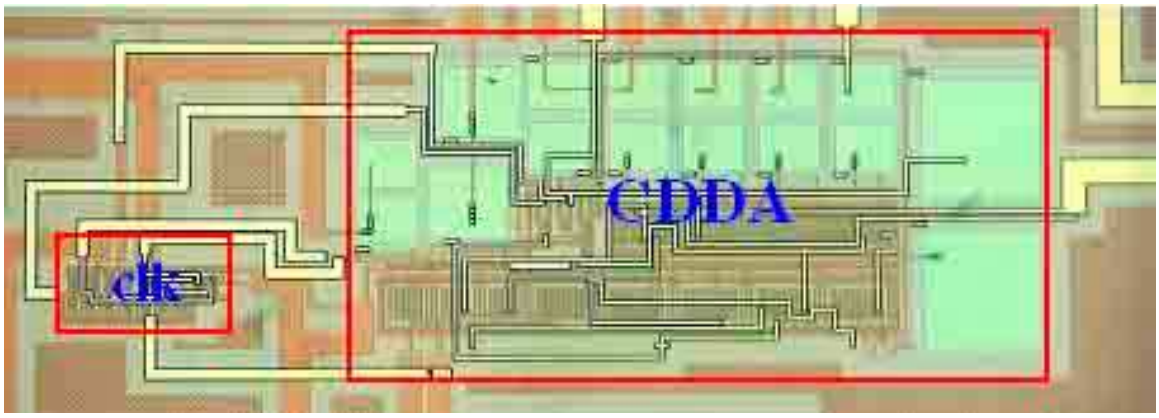
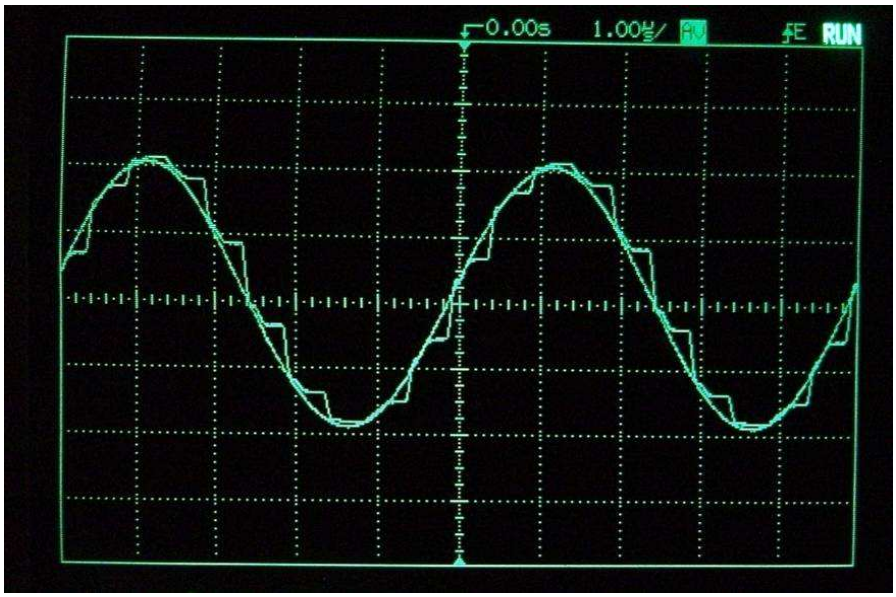
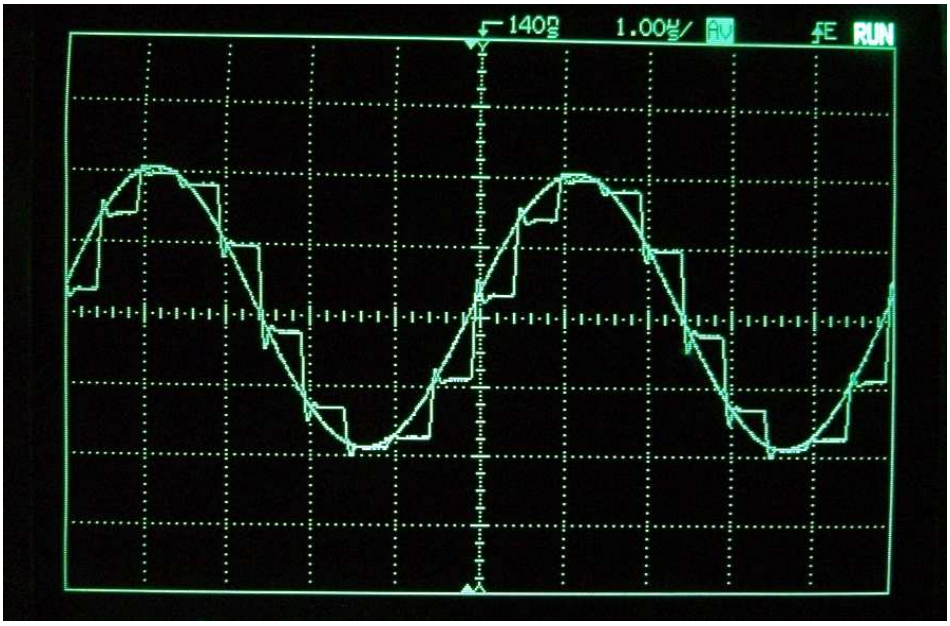



Fig. 5 Micrograph of fabricated chip showing. Red boxes outline clocked DDA (CDDA area 740x310um$^2$) and non overlapping clock generator (clk area: 180x70um$^2$)

Fig. 6 shows experimental waveforms of the circuit used as a track and hold and as a sample and hold with a rail to rail 200kHz input signals and 1MHZ clock. The track and hold was implemented by connecting two chips with complementary control signals externally . The track and hold operated with clock signals up to 5MHz with an SFDR of -70dB. Figs. 7 and 8 show the input and output waveforms of the circuit used as a fully differential buffer and as a single ended to fully differential converter with rail to rail input/output signals. In this case terminals phi and $phi_{no}$ were set to constant voltages Vdd and Vss respectively. Measured bandwidth was 9.5MHz.




( a )




( b )

Fig. 6. Experimental input and output differential waveforms of (a) track and hold circuit of Fig. 2a for 4.4Vpp (b) sample and hold circuit of Fig. 2b for 1.1V pp 200kHz input sinusoidal signal and 1MHz clock frequency. Horizontal 1us/div, vertical 1V/div

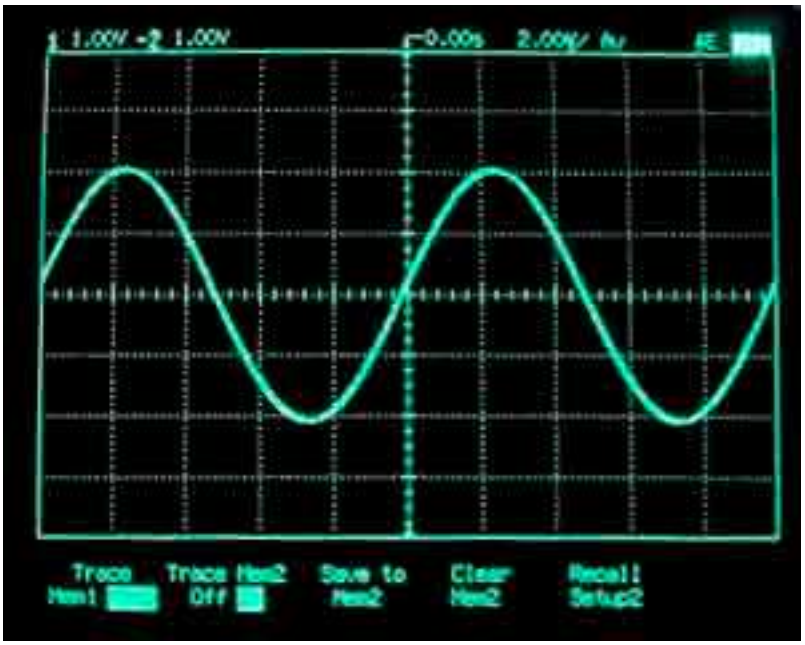



Fig. 7. Experimental input and output differential waveforms of differential buffer circuit of Fig. 1c for rail to rail 4.4Vpp 100KHz input sinusoidal signal with 70pF capacitive load on each output . Horizontal 5us/div, vertical 1V/div

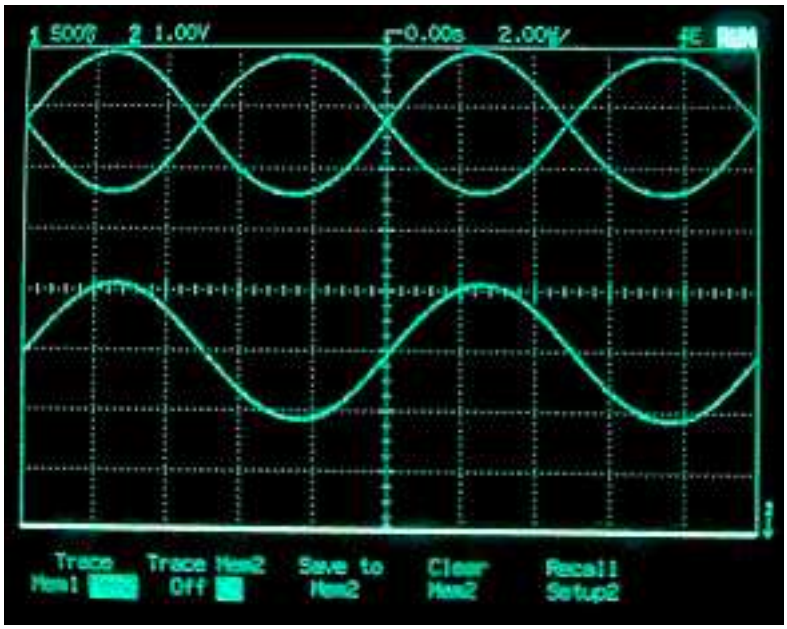



Fig. 8. Experimental input (bottom) and output (top) differential waveforms of single ended to differential converter of Fig. 1d for rail to rail 2.2Vpp 100kHz input sinusoidal signal. Horizontal 5 us/div, vertical: 0.5V/div (top waveform) 1V/div (bottom waveform)

## 5. Conclusions

A very compact implementation of a class AB low voltage rail to rail fully differential DDA was introduced. Its application as a track and hold, sample and hold, fully differential buffer and single ended to differential converters with enable inputs was discussed. The implementation of the circuit in deep sub-micrometer CMOS technology was also discussed. Experimental results of a test chip prototype in 0.5um validated experimentally the circuit operating with rail to rail signals and a 5MHz clock frequency with SFDR=70dB.

## References


[1] E. Sackinger and W. Guggenbuhl, "A versatile building block: the CMOS differential difference amplifier," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 2, p. 294, Apr. 1987.

[2] S. A. Mahmoud and A. M. Soliman, "The differential difference operational floating amplifier: a new block for analog signal processing in MOS technology," *IEEE Trans. Circuits Syst. II, Analog. Digit. Signal Process.*, vol. 45, no. 1, pp. 148–158, Jan. 1998.

[3] N.P. Ramachandran, H. Dinc, A.I. Karsilayan , "A 3.3-V CMOS Adaptive Analog Video Line Driver with Low Distortion Performance," *IEEE Journal of Solid State Circuits*, Vol. 38, No. 6, June 2003 pp:1051 – 1058.

[4] J. F. Duque Carillo, G. Torelli, R. Perez-Aloe, J. M. Valverde, and F. Maloberti, "Building blocks based on fully differential difference amplifiers with unity gain feedback," *IEEE Trans. Circuits Syst. I, Fundam. Theory and Appl.*, vol. 42, no. 3, pp. 190–192, Mar. 1995.

[5] "The Universal Op-Amp and Applications in Continuous-time Linear weighted Voltage addition," J. Ramirez-Angulo and F, Ledesma, *IEEE Transactions on Circuits and Systems II* , Volume 53, Issue 5, May 2006 Page(s):283 – 285

[6] "Simple technique using Local CMFB to enhance Slew Rate and bandwidth of one-Stage CMOS op-amps," Jaime Ramirez-Angulo and Michael Holmes. *Electronics Letters*, vol. 38, No 23, pp. 1409-1411, November 7th 2002,

[7] "Low-Voltage Super Class AB CMOs OTA Cells with very high Slew Rate and Power Efficiency,"Antonio J. López-Martín , S. Baswa , J. Ramirez-Angulo, and R. G. Carvajal, *IEEE Journal of Solid State Circuits*, Vol. 40, No. 5, May 2005. pp. 1068-1077.

[8] "Low-Voltage OTA architectures Using Multiple Input Floating gate Transistors," J. Ramírez-Angulo, S.C. Choi, G. Gonzalez-Altamirano, *IEEE Transactions on Circuits and Systems*, vol. 42, No. 12, pp.971-974, November 1995.

[9] J. Ramirez-Angulo, R. G. Carvajal, J. Tombs, and A. Torralba, "Low-voltage CMOS Op-amp with rail-to-rail signal swing for continuous-time signal processing using multiple-input floating-gate transistors," *IEEE Transactions on Circuits and Systems, special issue on applications of floating gate transistors*, vol. 48, No. 1, Jan. 2001, pp. 110-116

[10] J. Ramirez-Angulo and A. Lopez, "MITE Circuits: The Continuous time counterpart to switched capacitor circuits," *IEEE Transactions on Circuits and Systems, special issue on applications of floating gate transistors*, vol. 48, No. 1, January 2001, pp. 45-55

[11] P. Lim and B.A. Wooley, A High Speed Sample and Hold Technique Using a Miller Hold Capacitance," *IEEE Journal of Solid State Circuits*, Vol. 26, No. 4, pp. 643-651, April 1991

[12] D. Johns, K. Martin, **Analog Integrated Circuit Design**, John Wiley and Sons, 1997, section 10.1, page 398.

[13] B. Razavi, "CMOS Technology Characterization for Analog and RF Design," IEEE J. of Solid State Circuits, vol. 34, No. 3 March 1999, pp. 268-276

[14] A. J. Annema, B. Nauta, R. Langevelde and H. Tuinhot, "Analog Circuits in Ultradeep Submicron CMOS, IEEE. J. of Solid State Circuits, vol. 40, No. 1, January 2005.

# Rail to Rail Fully Differential Sample and Hold Based on Clocked Differential Difference Amplifier Using Resistive Local Common Mode Feedback

Jaime Ramirez-Angulo[1], Clara Lujan-Martinez[2],
Carlos Rubia-Marcos[2],
R. G. Carjaval[2], A. J. Lopez-Martin[3]

[1]Klipsch School of Electrical and Computer Engineering,
New Mexico State University
[2]University of Seville, Spain [3]Public University of Navarra, Spain.

# Outline

- Introduction
- Clocked Fully Differential DDA
- Rail to rail class AB low voltage Implementation
- Experimental Results
- Conclusions

# I. Introduction

## Differential difference amplifier (DDA):

- Extension of op-amp with two differential inputs
- Described by Vd1+Vd2=0 (instead of Vd=0 as in conventional op-amp)

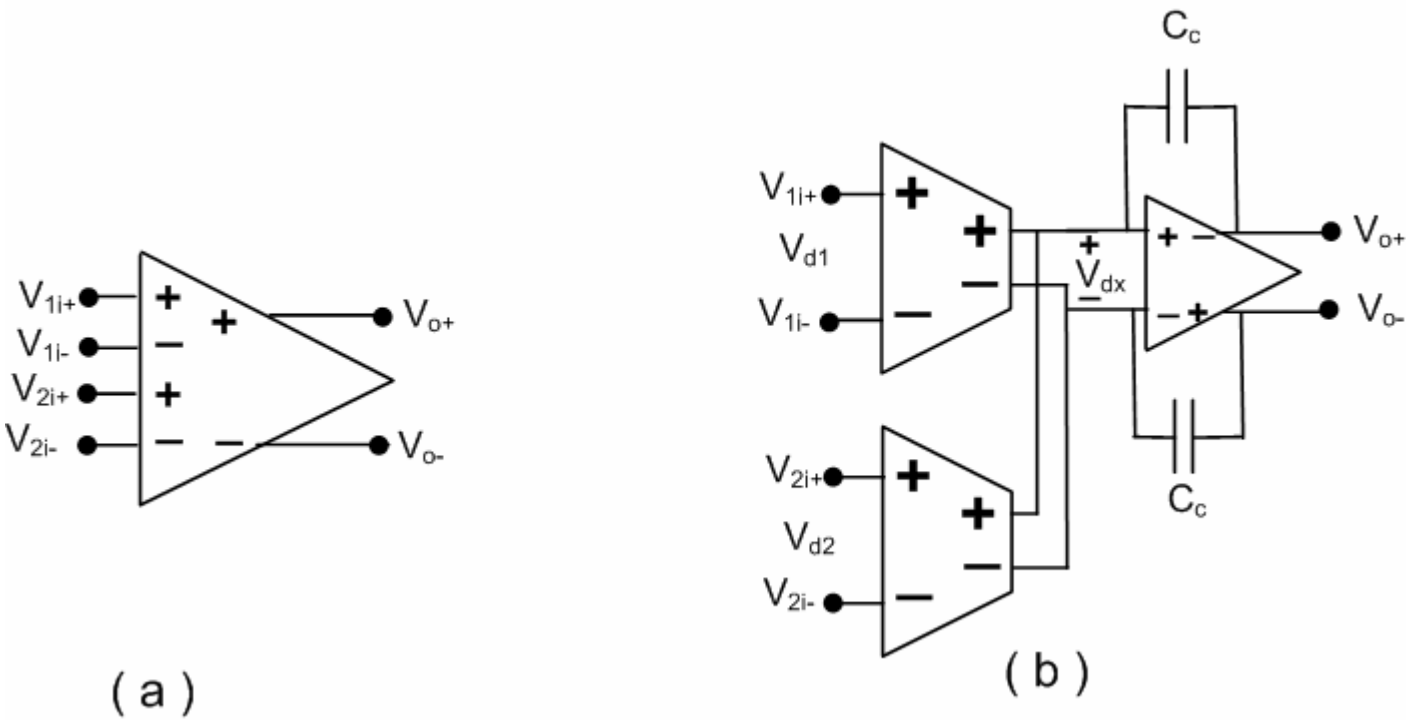



Fig. 1 Fully differential DDA: (a) Symbol (b) Internal architecture

# I. Introduction

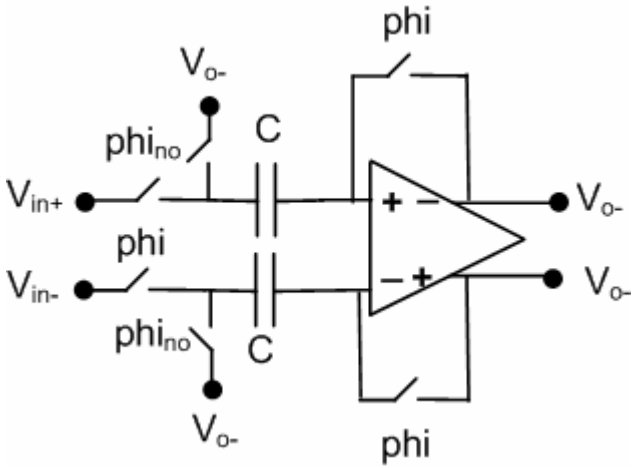
## Important Features of existing DDAs:

- Input/output common mode range very limited in low supply environment in deep submicrometer CMOS technology
- Fully differential architectures
- Versatile building block for analog signal processing

## We discuss in this presentation:

Application of differential DDA for implementation of high performance low voltage rail to rail sample and hold circuits

# I. Conventional fully differential sample and hold




Drawbacks:

- Outputs Reset during phi to zero. It requires op-amp with high slew rate → slow speed
- Supply voltage requirements: twice headroom of differential pair→ large supply requirements
- Separate capacitors for op-amp compensation and for holding signal →slow speed, large silicon area
- Signal dependent clock injection → low resolution

# II. Clocked fully differential DDA

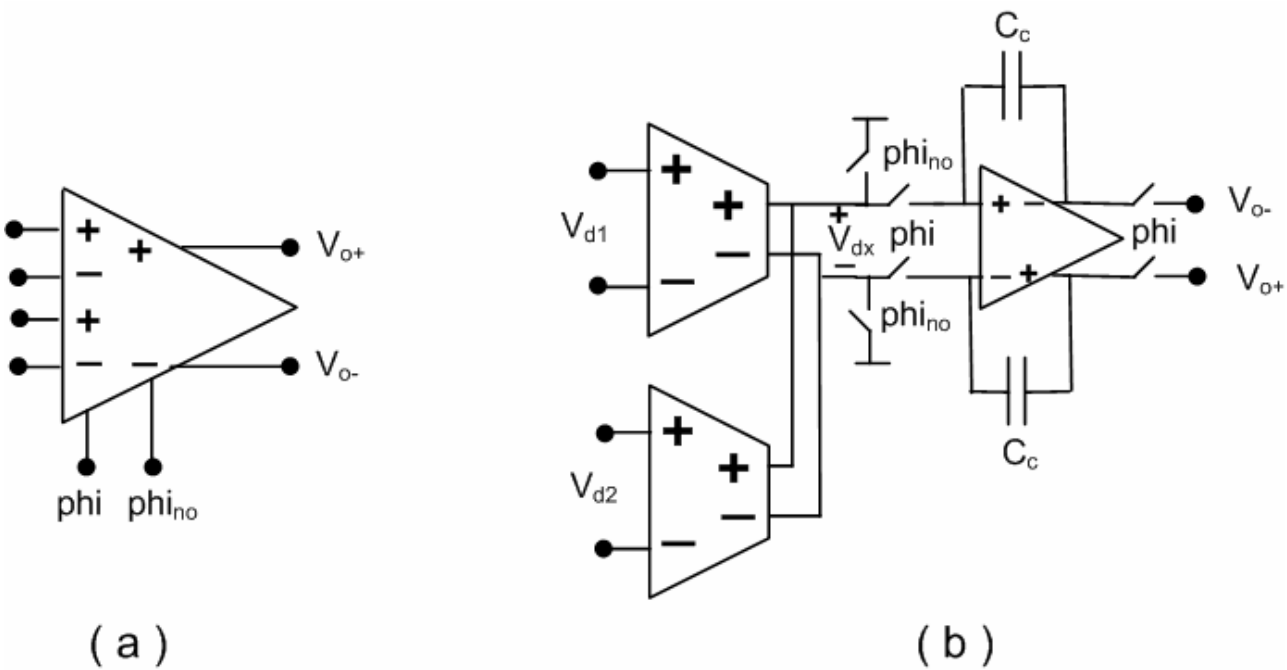



Fig. 3 CFD-DDA: (a) Symbol (b) Internal structure

# II. Clocked DDA

## Tracking Phase phi:

- Common outputs of first stages connected to input of second stage, outputs of second stage connected to DDA outputs

  → Large open loop gain $A_{ol}=A_1A_2$

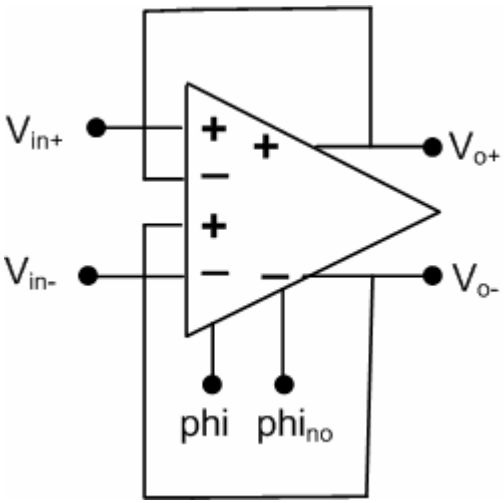
  → with negative feedback: $V_{d1}+V_{d2}=0$; $V_1=0$, $V_2=0$, $V_{o+} = V_{in+}$, $V_{o-} = V_{in-}$

$$V_o=V_{in}$$

# II. Clocked DDA

## Hold Phase $phi_{no}$:

- Outputs of first stage connected to AC ground
- Inputs of second stage floating
- Compensation capacitor $C_c$ holds $V_o$




CFD-DDA connection as a track and hold buffer

# II. Fully differential clocked DDA

## Remarks:

- Approximately equal, signal independent clock injection from switches controlled by phi introduces same systematic error voltage in Vo+ , Vo-

  → Differential output voltage Vo free from clock injection errors

  → Small compensation capacitors Cc can be used. This allows high DDA bandwidth GB=$g_{m1}/C_c$
- Output does not reset to zero every cycle. For this reason it does not require op-amp with high slew rate
- Capacitors used both for compensation and for holding

# II. Clocked fully differential DDA

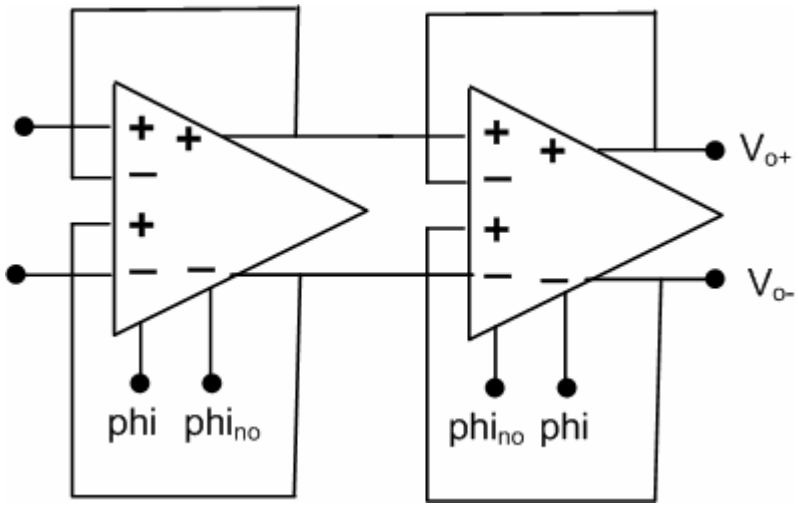



Fig. 5 Cascading two CFD-DDAs to implement sample and hold

# III. Rail to rail DDA implementation

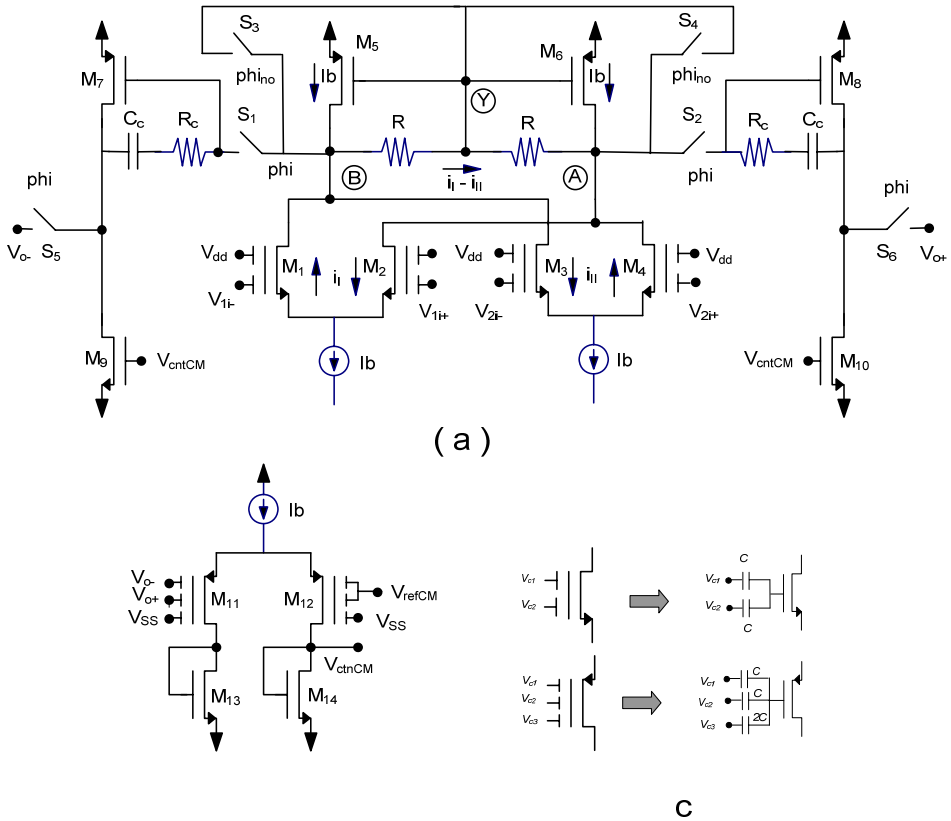



Fig. 6 (a) Rail to rail two stage fully differential difference amplifier using local resistive common mode feedback, (b) Rail to rail capacitive Common mode feedback network (c) Symbols and equivalent circuits of 2 and 3 input floating gate transistors

# III. Rail to Rail operation of clocked DDA

Based on floating gate technique. It allows to operate input stage and common mode feedback network with rail to rail voltages and supplies close to a transistor threshold's voltage [1, 2] . Capacitive divider at the input of the floating gate transistors has two purposes:

- It increases the headroom for the differential pair by shifting, in the positive direction, the DC quiescent gate voltage of $M_1$-$M_4$ as the result of connecting one of the inputs of the divider to the upper rail, $V_{DD}$.
- It attenuates the differential signals $V_{d1}$ and $V_{d2}$.

[1] J. Ramírez-Angulo, S.C. Choi, G. Gonzalez-Altamirano, "Low-Voltage OTA architectures Using Multiple Input Floating gate Transistors," *IEEE Transactions on Circuits and Systems*, vol. 42, No. 12, pp.971-974, November 1995.

[2] J. Ramirez-Angulo, R. G. Carvajal, J. Tombs, and A. Torralba, "Low-voltage CMOS Op-amp with rail-to-rail signal swing for continuous-time signal processing using multiple-input floating-gate transistors," *IEEE Transactions on Circuits and Systems, special issue on applications of floating gate transistors*, vol. 48, No. 1, Jan. 2001, pp. 110-116

# III. Class AB operation of clocked DDA

Based on resistive local common mode feedback [3, 4]

- Complementary large swing at nodes A,B leads to very large currents in output stage→ high slew rate since dynamic output current can be essentially larger than quiescent current

[3] "Simple technique using Local CMFB to enhance Slew Rate and bandwidth of one-Stage CMOS op-amps," Jaime Ramirez-Angulo and Michael Holmes. *Electronics Letters*, vol. 38, No 23, pp. 1409-1411, November 7th 2002,

[4] "Low-Voltage Super Class AB CMOs OTA Cells with very high Slew Rate and Power Efficiency,"Antonio J. López-Martín , S. Baswa , J. Ramirez-Angulo, and R. G. Carvajal, *IEEE Journal of Solid State Circuits*, Vol. 40, No. 5, May 2005. pp. 1068-1077.

# III. Offset compensation

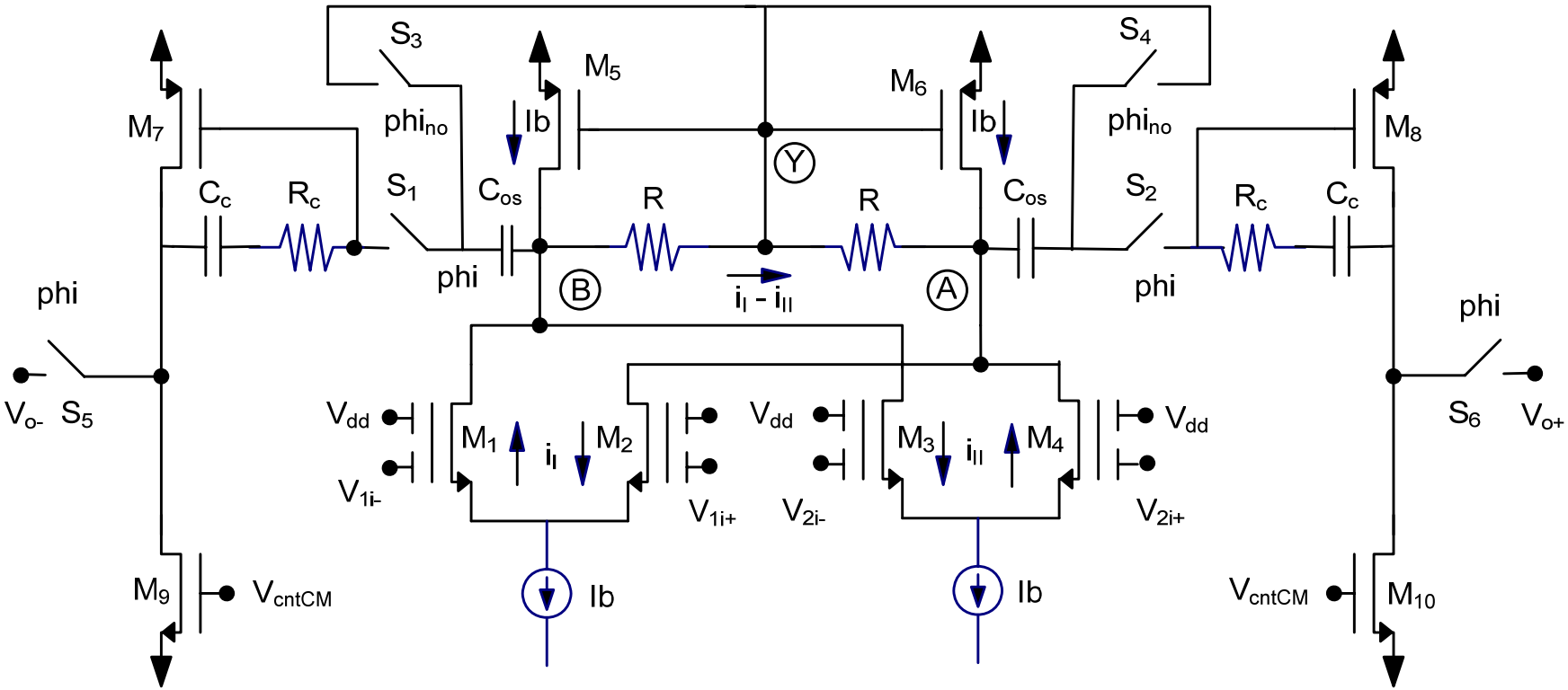
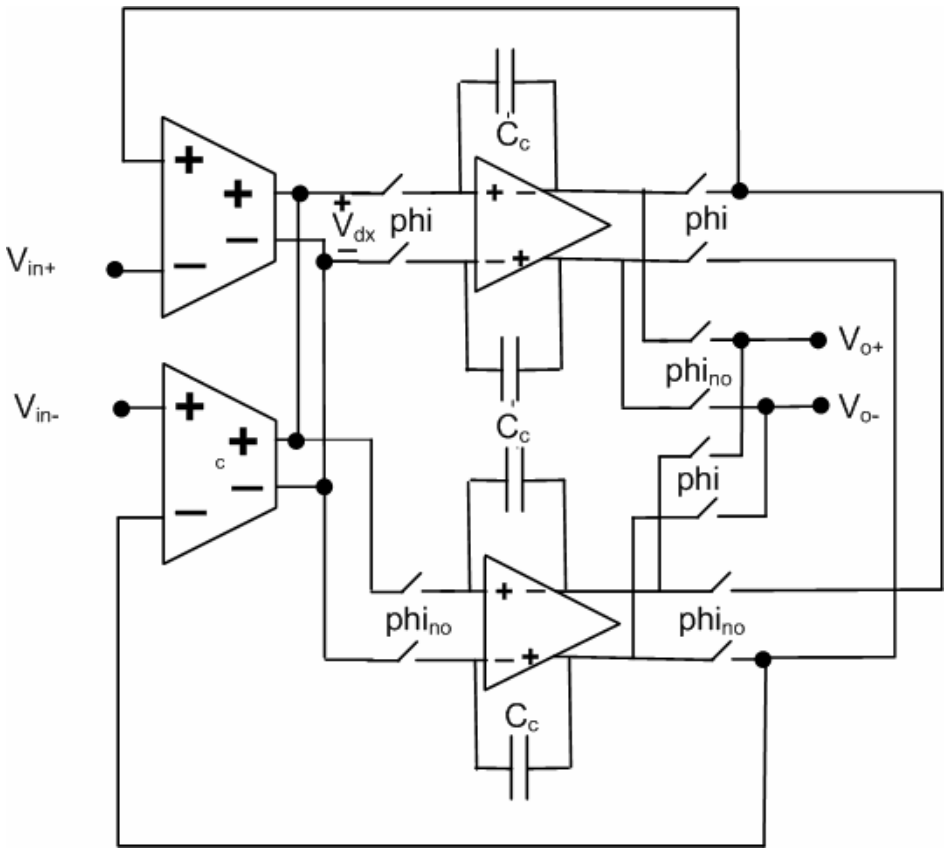



Fig. 7 CFD-DDA with offset compensation capacitors $C_{os}$ at output of first stage

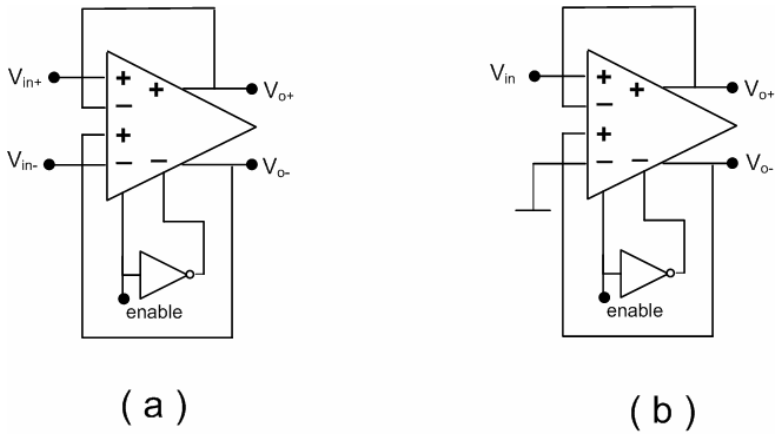
# III. True sample and hold with alternatively switched output stages



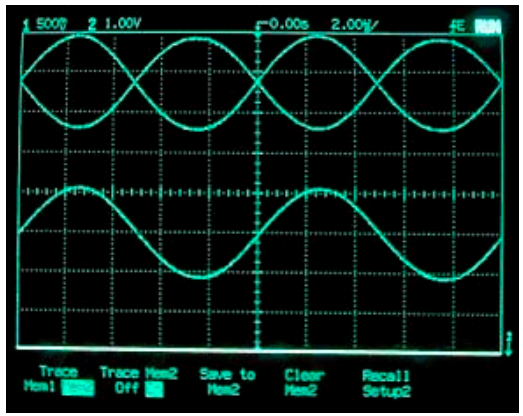
# III. Implementation of the CFD-DDA in deep submicrometer CMOS technology

- Two stage architecture, class AB operation with low supply, rail to rail characteristics specially attractive in deep submicrometer CMOS (DS-CMOS) technologies.
- Example: 90nm CMOS technology with $V_{TPMOS} \approx V_{TNMOS} \approx 0.35V$, $V_{DSsat}=0.1V$ operation from single supply $V_{DD}=1V$. Gate leakage can be compensated for by including two additional switches that connect (refresh) the gates of $M_1$-$M_4$ to $V_{DD}$ (or some other bias voltage) during $phi_{no}$.
- CFD-DDA redesigned in 90nm technology operates rail to rail with single 1V supply with 120MHz clock.

# III. Other applications of CFD-DDA



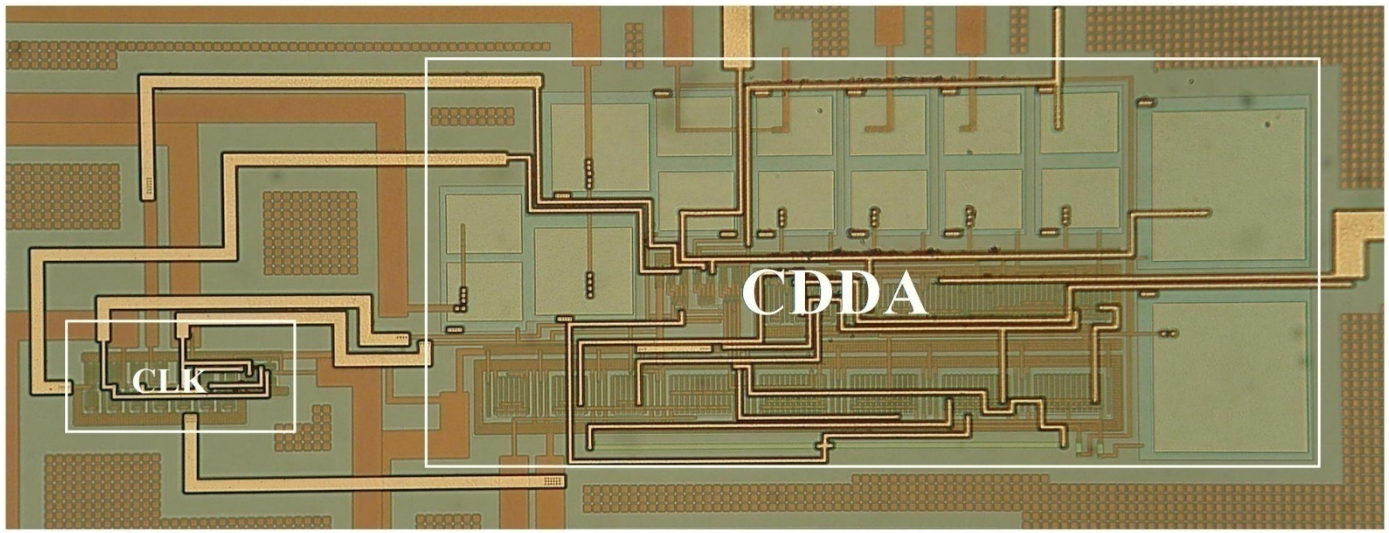

( a ) ( b )




( c )

(a) Fully differential buffer (b) Single ended to fully differential converter
(c ) experimental results: input trace (bottom), output traces (top)

# IV. Layout and Micrograph




**(180µm x 70µm)**

**Fig. 10 Layout and Micrograph of test chip in 0.5µm MOSIS CMOS technology**

# III. Transistor dimensions and device values

| *Transistor* | *W/L (µm/µm)* |
|---|---|
| $M_1$-$M_4$, $M_{13}$-$M_14$ | 50/1 |
| $M_5$-$M_8$ | 240/1 |
| $M_9$-$M_{10}$ | 100/1 |
| $M_{11}$-$M_{12}$ | 120/1 |
| ***Other devices*** | ***Value*** |
| R | 50 KΩ |
| $R_c$ | 1.5 KΩ |
| C | 1 pF |
| $C_L$ | 5 pF |
| Ib | 200µA |

TABLE I. TRANSISTORS DIMENSIONS AND OTHER DVICES VALUES

# IV. Chip Parameters

- VDD : 1.1V
- VSS : -1.1V
- Chip Fabricated : MOSIS
- Ib : 200 μ A
- Technology : 0.5μm AMI CMOS
- Simulation tool : Cadence Spectre
- Layout tool : Virtuoso layout editor

# IV. Experimental Results

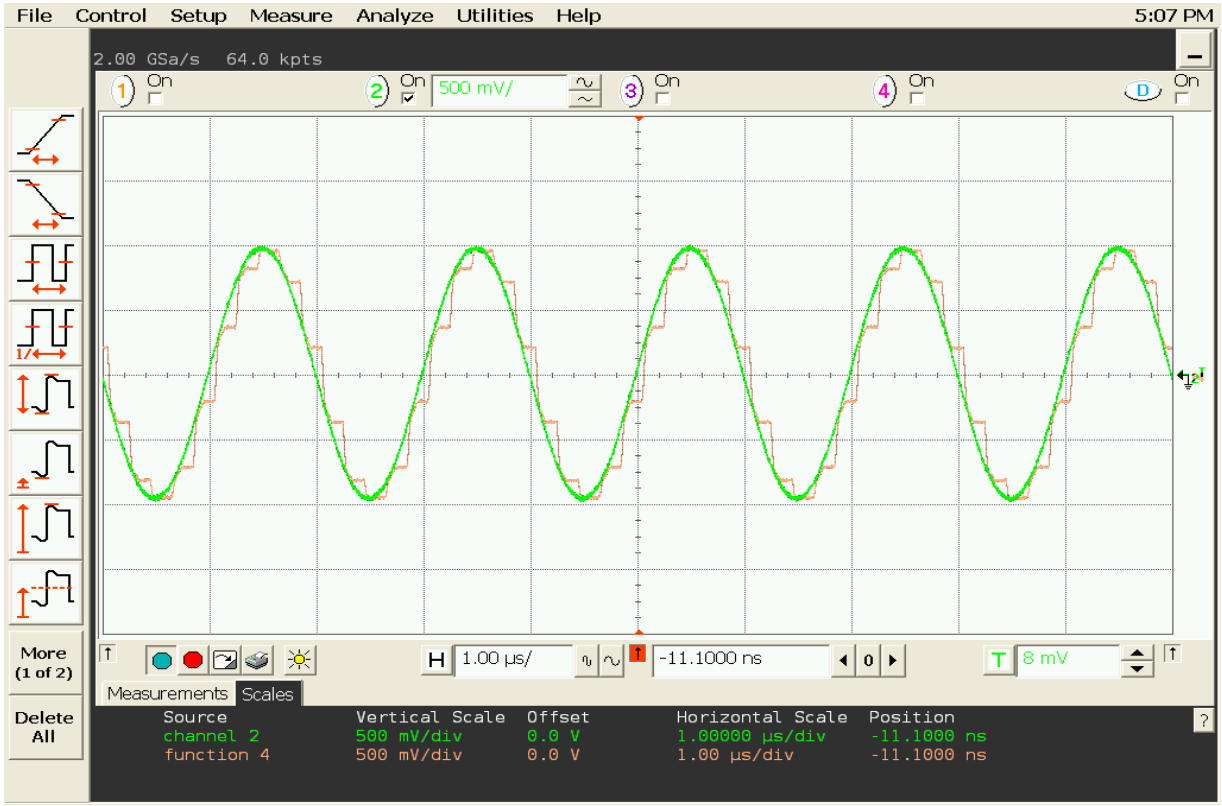



Fig. 11 Input and output differential waveform of the fabricated circuit ($2V_{pp}$ @ 500kHz input signal and 5MHz input clock). Horizontal 1µs/div, vertical 0.5V/div

# IV. Experimental Results

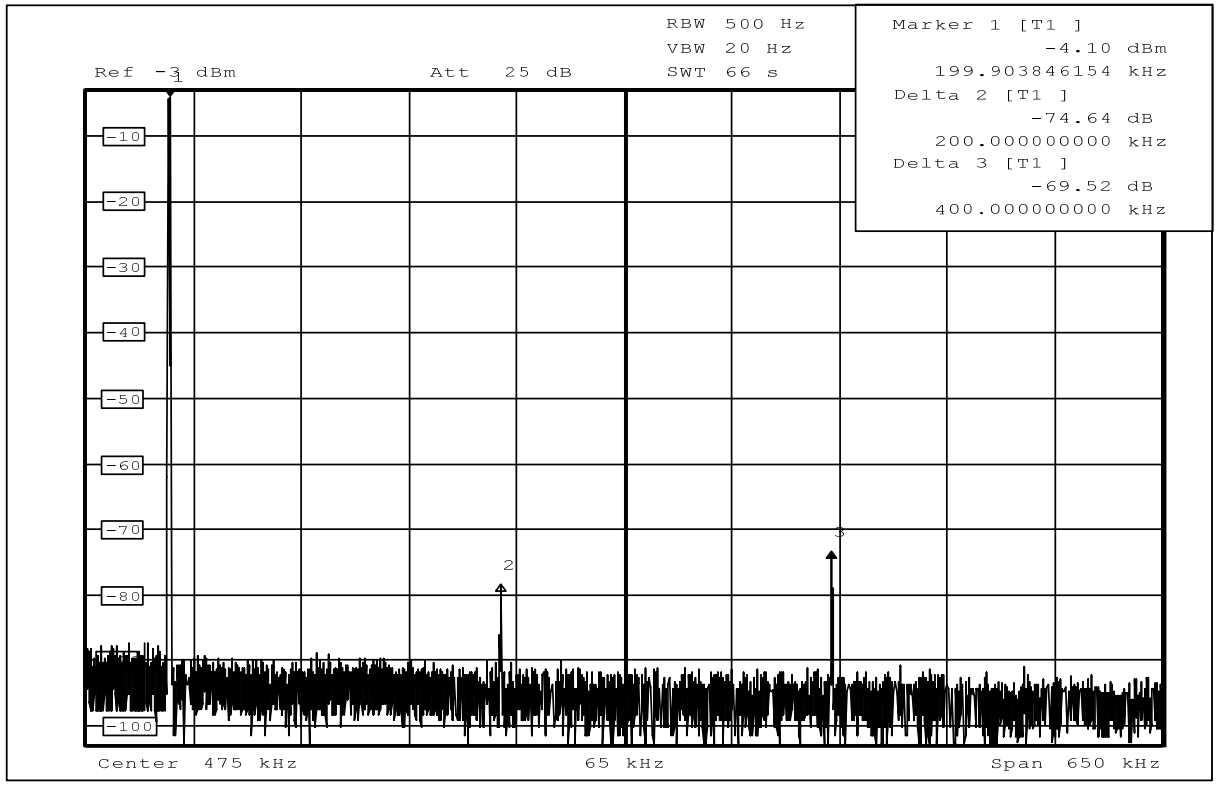



Fig. 12 THD for 2Vpp input signal at 200kHz and 2MHz input clock

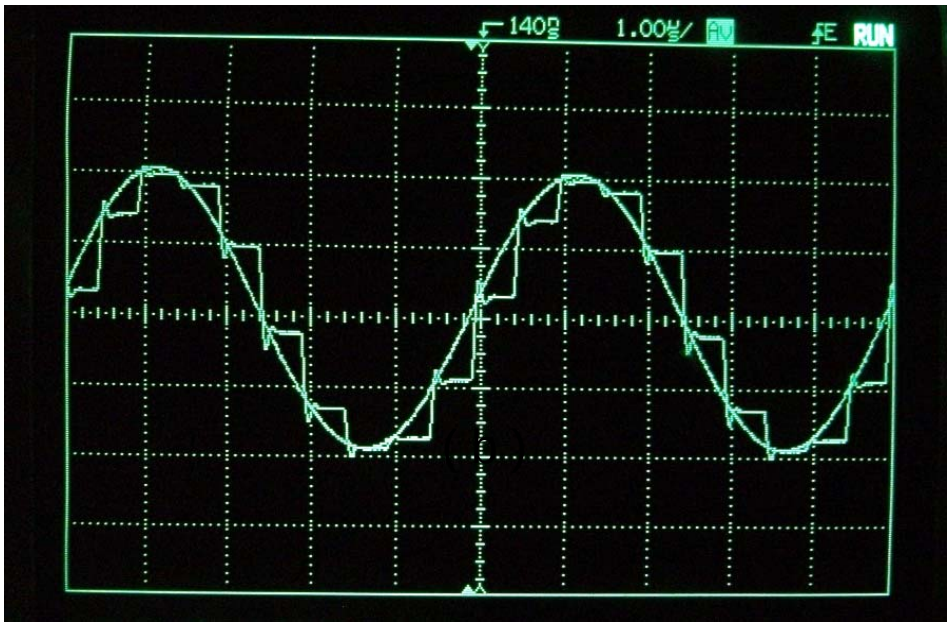



Fig. 13. Experimental input and output differential waveforms of sample and hold circuit of Fig. 2b for 1.1V pp 200kHz input sinusoidal signal and 1MHz clock frequency. Horizontal 1us/div, vertical 1V/div

# V. Conclusion and Future Strategies

- New Compact Sample and hold based on clocked fully differential DDA introduced.
- Experimental results form fabricated chip verify the operation of proposed circuit with Rail to Rail, class AB, low supply operation
- Accurate offset compensation at output of first stage easy to include
- True sample and hold using alternatively switched output stages
- Operation in deep submicrometer CMOS technology without floating gates possible.


# Thank you

# Buck-Boost Converter Based Power Conditioning Circuit for Low Excitation Vibrational Energy Harvesting


Arvindh Rajasekaran

Electrical Engineering Department
The University of Texas at Dallas
Richardson, TX 75252
Tel : 469-463-0702
e-mail : axr066200@utdallas.edu

Abhiman Hande

Texas Piezoelectric Inc.
Dallas, TX 75251
Tel : 469-916-6595
e-mail :
ahande@texasmicroenergy.com

Dinesh Bhatia

Electrical Engineering Department
The University of Texas at Dallas
Richardson, TX 75252
Tel : 972-883-2386
e-mail : dinesh@utdallas.edu



**Abstract - A method of harvesting low excitation vibrational energy using a buck-boost dc-dc converter to power active RFID tags is presented. Using the discontinuous conduction mode (DCM), the impedance of the converter is designed to match that of the piezoelectric transducer, thereby allowing maximum power transfer. It is shown that using multiple transducers in a parallel configuration is the optimum method for harvesting energy by increasing the available power, and reducing the transducer's effective impedance.**


## I. Introduction

Wireless applications are an integral part of our lives, and are only growing as technology enables smaller, lower power and more capable devices. One of the areas that is popular today and is finding new applications is wireless sensor networks (WSNs). The widespread need for WSNs is evident from the proliferation of short-range wireless standards such as Bluetooth, ZigBee, Wi-Fi, and RFID [1]. Sensor nodes for wireless personal area network (WPAN) that utilize smart mesh network protocols are traditionally designed to be optimized for low cost and low power. Each wireless node is intended for deployment in large quantities at remote locations to sense critical data and relay its measurements to other network nodes for monitoring and control purposes. In this new era of high security and vigilance, wireless sensors are being deployed at major events so as to predict catastrophes such as acts of terrorism [2]. Another application combines the data from vehicular sensors, such as wheel hub-odometers, tire pressure sensors, and asset tags to improve safety, reliability, and reduce fleet maintenance costs. As these types of applications proliferate, it will become necessary to deploy sensor nodes in hard to reach places. Once thousands of low-cost RF sensors are deployed for any given application, replacing batteries will become an impractical task. Therefore, self-sufficient devices that can operate for an indefinite period of time will be required.

Energy harvesting (EH) from solar, wind, vibrations, thermal, etc. to power wireless devices has been attracting considerable interest in the past few years [3]. While solar energy provides relatively higher energy density outdoors, its efficiency under indoor conditions is considerably lower. Similarly, vibrational EH using piezoelectric bimorphs, and electromagnetic and electrostatic generators require high excitation energy to provide reasonable power levels (of the order of a few mWs). However, many practical applications produce only low excitations (e.g. 0.05 - 0.5 $g_{peak}$) at low frequencies (e.g. 20 – 200 Hz). Consequently, off-the-shelf DC-DC converters and rectifiers, when coupled with off-the-shelf piezoelectric bimorphs, do not yield optimum results.

This paper focuses on the design of high efficiency power electronics for such vibrational EH systems. The specific application involves powering active vehicle RFID tags, from Axcess International Inc. [4], that are installed on the windshield of automobiles and front of truck trailers. The tags operate at 3 $V_{DC}$ and draw about 6 - 10 µA during sleep mode and about 15 - 20 mA for short periods of 20 msec when operational. This indicates average power consumption of about 18 - 30 µW per day. Experimental data shows that a majority of the vibrations for this application lie in the 10 - 30 Hz frequency range with low excitation levels of about 0.05 - 0.3 $g_{peak}$ [1].

The paper is organized as follows: Section II describes the system and the equivalent electrical model. The details of each unit are presented in Sections III and IV. Simulation results are discussed in Section V along with experimental data. Finally, Section VI concludes the paper.

## II. Energy Harvesting Circuit and Electrical Model

### *A. System Overview*

A typical EH system for a wireless sensor consists of a transducer, AC-DC conversion (in certain cases), a DC-DC converter, and a battery charging and power management module as shown in Fig.1.

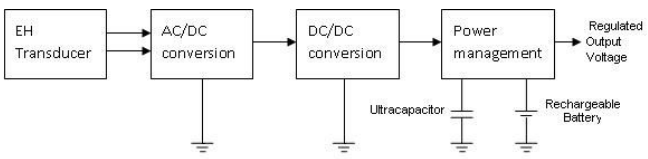



Fig. 1. EH block diagram.

In this paper, piezoelectric cantilever beams are used as the EH transducer. There are different types of piezoelectric materials used to harvest vibrational energy (PVDF, PZT-5, etc.) and each produces maximum power when excited in a certain fashion. The chosen material is a Macro Fiber Composite (MFC) consisting of multiple PZT-5A ceramic rods as a flexible patch [5]. Each patch is mounted on an aluminum beam in a cantilever type set up to allow $d_{31}$ mode of operation [3]. Since the output from a piezoelectric vibrational source is an AC voltage, an AC-DC converter is required. A full wave bridge rectifier has a relatively higher efficiency, and is ideal for AC-DC conversion. In addition, a DC-DC converter is necessary to convert the rectified DC voltage to levels acceptable to recharge an energy storage device (e.g. secondary battery). The rectified DC voltage is conditioned to enable maximum power transfer by carefully designing the DC-DC converter.

### *B. Simulation Model*

In order to simulate a piezoelectric vibrational transducer, an equivalent electrical model is first used. The piezoelectric cantilever is modeled for resonance operation with an appropriate AC voltage source and a series capacitance in PSpice [6]. Fig.2 shows the electrical model.

The model was found to closely match experimental results. The values of components in the simulation model can be modified to represent multiple cantilevers in series or parallel.

## III. AC-DC Conversion and Impedance Matching

Different types of rectifiers such as half-wave, full-wave, voltage doublers, etc. can be used to convert the AC transducer voltage to DC voltage. Power efficiency is an important criterion while choosing the rectifier topology. A full wave bridge rectifier has a relatively high efficiency and therefore, was chosen for the harvester (refer Fig.2). The challenges with such a rectifier however, are the minimum voltage requirements due to the forward voltage drop of two diodes in series and the leakage current when the diodes are reverse biased. For example, each silicon diode requires a 0.6 - 0.7 $V_{DC}$ voltage drop to be overcome before conduction begins. This forward voltage drop causes power loss during conduction and consequently, lower efficiency. Alternatively, germanium diodes have a relatively lower 0.3 $V_{DC}$ forward voltage drop. But this is still fairly large when input power flow from the piezoelectric cantilever structure is of the order of only hundreds of $\mu W/cm^3$. It is therefore very important to choose diodes that have a low leakage current and a small turn-on voltage. To meet these specifications, low forward voltage (0.2 $V_{DC}$) Schottky diodes which have a leakage of 200 nA are chosen. Also, synchronous rectifiers can be used instead of Schottky diodes to improve efficiency. Here, the body diode of a MOSFET is used instead of a discrete pn junction diode. The transistor is turned on when the body diode begins conduction. Due to the extremely low $R_{ds(on)}$ (few mohms) specifications of MOSFETs, the voltage drop across the body diode during conduction is negligible, consequently yielding very low power loss and high efficiency [6].

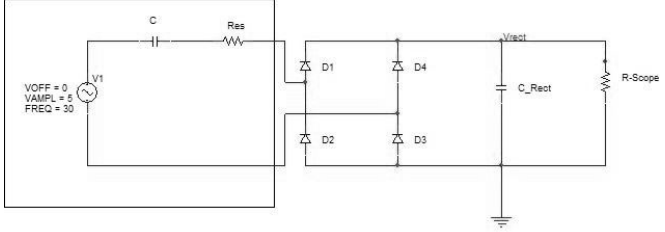



Fig. 2. Equivalent electrical model with rectifier circuit for a piezoelectric cantilever beam vibrating at its resonant frequency.

In order to obtain maximum power transfer, the impedance of the load should match that of the source. It is observed that the impedance of the transducer can be computed to be

$$Z_0 = \frac{1}{2\pi f_R C} \tag{1}$$

where: $f_R$ is the resonant frequency of the cantilever structure and C is the series transducer capacitance. Therefore, as the frequency decreases, the impedance increases.

Fig.3 shows about 210 µW maximum power obtained from a transducer comprising of one MFC M2814P2 patch mounted on an aluminum beam of adequate thickness and tip mass at 45 Hz $f_R$ and 0.5 $g_{peak}$ acceleration. The electrical model for such a cantilever structure (described in Fig.2) with C = 26 nF results in $Z_0$ = 136 kΩ.

Most transducers have such large impedances of the order of 100 kΩ to 1 MΩ. This results in a challenge in designing the DC-DC converter and consequently, harvesting maximum power.

## IV. DC-DC Conversion

The overall efficiency of the system depends upon efficiency of the rectifier in conjunction with the DC-DC converter. There are several DC-DC converter topologies to choose from. Typically, non-isolated switch-mode DC-DC converters seem to be the energy conversion device of choice due to relative ease in matching the transducer impedance. The three most basic converter topologies: buck (step-down), boost (step-up), and buck-boost (step-up/step-down) can all be used to achieve impedance matching. Alternatively, charge pumps or switched capacitor converters are also feasible in certain cases due to ease of integration on an integrated circuit (IC). These converters have the advantage of consisting of only capacitors and MOSFETs (no inductor).

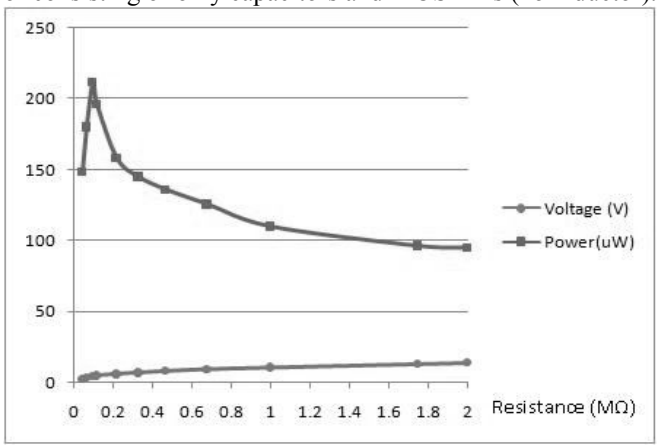



Fig. 3. Power and voltage plots for a single MFC M2814P2 patch based EH transducer.

However, from a maximum power transfer standpoint their input resistance cannot be easily tuned to match the output impedance of the transducer. Low drop out (LDO) regulators are not considered as candidates since they suffer from poor efficiency and can only step down the voltage (no step-up possible).

A buck-boost converter is observed to be most suitable for low excitation levels, and high efficiency requirements [1]. The buck-boost converter circuit is shown in Fig.4. Buck converters are not very efficient at low excitation levels. It has been shown that these converters require at least 35 $V_{DC}$ open circuit rectifier voltage to obtain 60 - 70% efficiency [7]. Moreover, buck-boost converters effectively work at input voltages above or below its output voltage ($V_{bat}$). Both these converters must operate in discontinuous conduction mode (DCM) for higher efficiency [7,8].

For a buck-boost converter operating in DCM, it has been noted that the average input resistance ($R_{in}$) is given by [7]

$$R_{in} = \frac{2Lf_{SW}}{D^2} \quad (2)$$

where: L= inductance, $f_{SW}$ = switching frequency, and D = duty cycle.

Therefore, for a given $f_{SW}$ and D, $R_{in}$ scales linearly with L. For large values of $R_{in}$, a larger L is necessary. However, this is not desirable since the losses due to the inductor ESR increase significantly as its value increases.

Condition for DCM operation is given by

$$V_{rect} < \frac{1-D}{D} V_{bat} \quad (3).$$

Note that if this condition is not adhered to, the converter enters continuous conduction mode (CCM) with

$$R_{in} = \left(\frac{1-D}{D}\right)^2 \frac{V_{bat}}{I_{bat}} \quad (4).$$

Here, $R_{in}$ is no longer constant, and the converter will require feedback for adjusting D to obtain constant $R_{in}$. This is a serious overhead resulting in lower efficiency, and therefore, must be avoided.

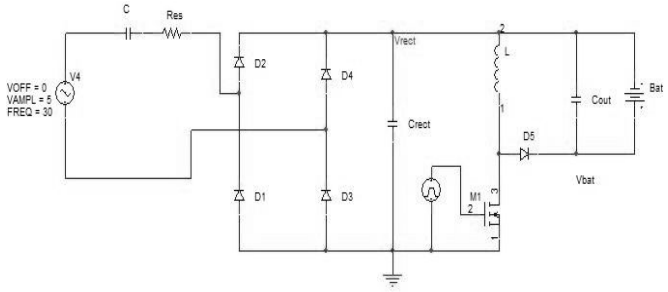



Fig.4. Buck-boost converter for piezoelectric EH.

## V. Simulations and Experimental Results

As indicated earlier, the Axcess active vehicle RFID tags were used as the sensor load. These tags operate at 3 $V_{DC}$ and draw about 6 - 10 µA during sleep mode and about 15 - 20 mA for short periods of 20 msec when active. This indicates average power consumption of about 18 - 30 µW over one day. Experimental data shows that a majority of the vibrations for this application lie in the 10 - 30 Hz frequency range with low excitation levels of about 0.05 - 0.3 $g_{peak}$. Given a constraint that vibrations are only available for four hours in a day, this requires about 108 - 180 µW be available to recharge the battery during that time.

The maximum power that can be harvested using a single cantilever structure with one M2814P2 MFC patch was observed to be about 70 µW at a resonant frequency of 30 Hz, and an excitation of 0.07 $g_{peak}$. This power is insufficient for the chosen application. Therefore, multiple MFC patches need to be used to achieve the necessary power. While cascading the transducers in series, it is observed that the power achieved scales with the number of transducers if all of them are vibrating in phase with each other. Such a scenario is difficult to obtain practically. Simulations show that the power falls off steeply for even slight variations in phase of individual transducers.

While transducers are connected in parallel, with independent rectifiers, the problem of out of phase inputs can be alleviated, and at the same time the effective impedance reduces. At this low resonant frequency, the impedance of a single transducer is approximately 200 kΩ. When eight such transducers are cascaded, the effective impedance reduces to 25 kΩ while providing 480 µW of maximum power. Fig.5 shows the simulated power comparison for 0.5 $g_{peak}$ at 45 Hz resonant frequency. In this case about 1.6 mW was obtained at 17 kΩ with eight cascaded transducers while only about 200 µW was obtained at a much higher impedance of about 100 kΩ with a single transducer.

Due to hardware and space constraints, experimental results are limited to a maximum of two transducers in parallel.

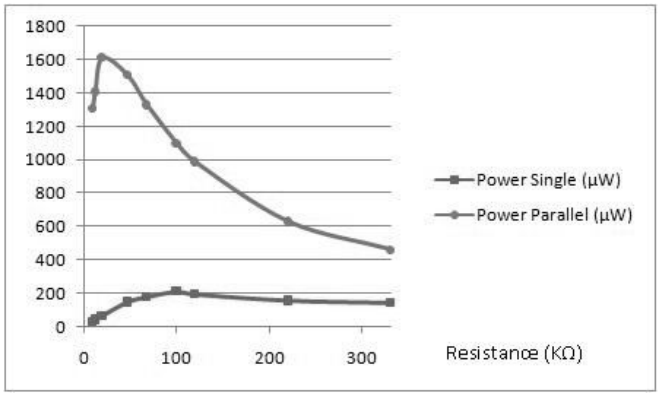



Fig.5. Power comparison for single vs. multiple MFC transducers.

The results from two parallel transducers match equivalent simulations, bringing the effective impedance down to 100 kΩ and providing a maximum rectifier power of 140 µW at 0.07 $g_{peak}$ acceleration and 30 Hz resonant frequency. This is effectively the input power to the DC-DC converter used for battery trickle charging. The output DC-DC converter power was measured to be 90 µW which indicates DC-DC converter efficiency of 64%.

The rectifier voltage, rectifier power and hence DC-DC converter output power increases with increased acceleration. It is observed that the rectifier power obtained from two transducers in parallel increases to about 230 µW for an acceleration of 0.09 $g_{peak}$. The DC-DC converter output power was measured to be 150 µW which indicates DC-DC converter efficiency of 65%. The rectifier voltage and DC-DC converter output power and efficiency plots obtained for varying acceleration values are shown in Figs. 6 – 8 respectively.

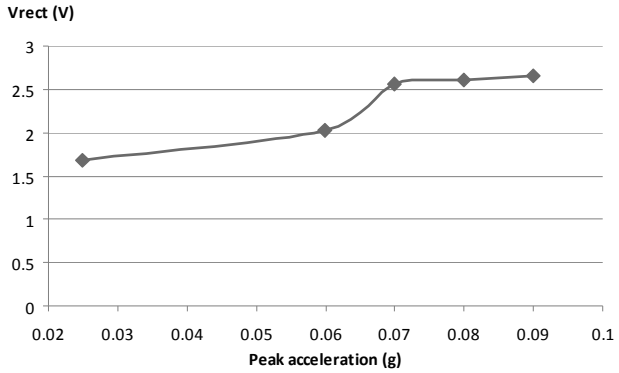



Fig.6. Rectifier voltage vs. acceleration.

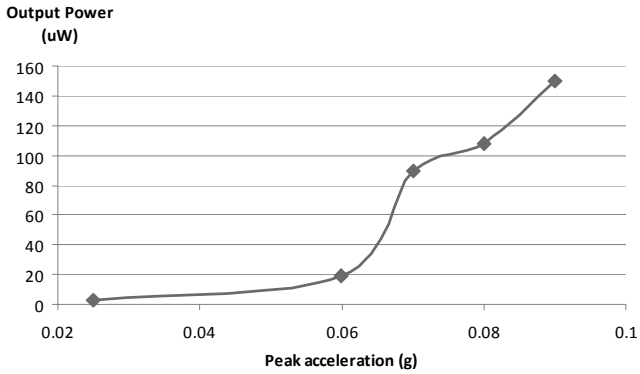



Fig.7. DC-DC converter output power vs. acceleration.

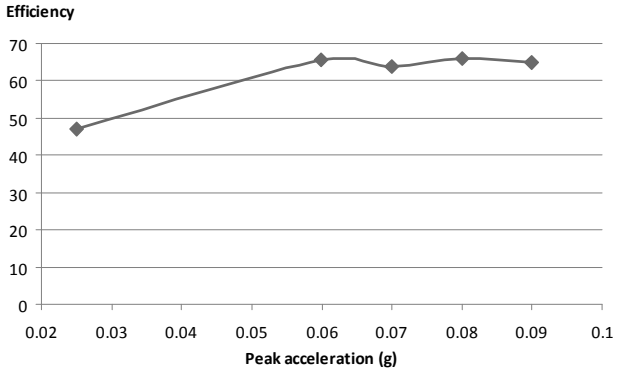



Fig.8. DC-DC converter efficiency vs. acceleration.

Higher values of acceleration resulted in the DC-DC converter entering CCM. This caused excessive loading on the transducer and therefore, poor power transfer. Needless to say, direct battery charging (without DC-DC converter) resulted in extremely poor power output and efficiency values.

## VI. Summary and Conclusions

The design of EH circuits for WSN nodes is very important primarily because of the rapid development of this market and secondly, due to the limited life of battery and consequently, replacement. This, in particular, adds cost and limits deployment of these devices to high-value asset and limited life applications. Feasible EH from vibrations can extend battery life and at the bare minimum replenish idle energy consumption which is a dominant factor in battery life reduction. Since off-the-shelf converters do not meet the specifications of transducers at low frequencies and excitation levels, it is essential to have efficient electronics to be able to harvest power in such applications. Further optimization and implementation on a chip could allow more widespread use of such circuits.

## Acknowledgement

This research was supported in part by Texas Piezoelectric Inc. under award no. UTD08-19. We wish to thank Raj Bridgelall (Vice President of Engineering and CTO, Axcess International Inc.) and Dr. Shashank Priya (Virginia Tech.) for their technical inputs.

## References

[1] A. Hande, R. Bridgelall, and D. Bhatia, "Energy Harvesting for Active RF Sensors and ID Tags", Energy Harvesting Technologies, Book chapter, Springer, 2008, ISBN: 978-0-387-76463-4.

[2] Axcess International Inc.," AXCESS Awarded $2 Million Contract for Integrated RFID and Sensor Port Security Solution in Barbados", Press Release, March 2007.

[3] S. Roundy, P. Wright, and J. Rabaey, "A Study of Low Level Vibrations as a Power Source for Wireless Sensor Nodes", Computer Communications, Vol. 26, pp. 1131–1144, July 2003.

[4] Axcess International Inc., http://www.axcessinc.com/products/tags.html, 2008.

[5] Smart Material, http://www.smart-material.com/Smart-choice.php?from=MFC, 2007.

[6] J. Han, A. Von Jouanne, T. Le, K. Mayaram, and T. Fiez, "Novel Power Conditioning Circuits for Piezoelectric Micro Power Generators", 19th IEEE Applied Power Electronics Conference, pp. 1541-1546, 2004.

[7] G. Ottman, H. Hofmann, and G. Lesieutre, "Optimized Piezoelectric Energy Harvesting Circuit using Step-down Converter in Discontinuous Conduction Mode", IEEE Transactions on Power Electronics, Volume 18, Issue 2, pp. 696-703, March 2003.

[8] E. Lefeuvre, D. Audigier, C. Richard, and D. Guyomar, "Buck-Boost Converter for Sensorless Power Optimization of Piezoelectric Energy Harvester", IEEE Transactions on Power Electronics, Vol. 22, No. 5, pp. 2018-2025, Sep 2007.

# Buck-Boost Converter for Low Excitation Vibrational Energy Harvesting

Arvindh Rajasekaran (UTD)

Abhiman Hande (TPI)

Dinesh Bhatia (UTD)

UTD

Texas Piezoelectric

# Purpose

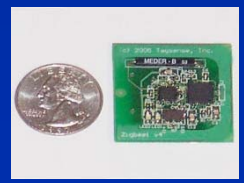
- A method of harvesting low excitation vibrational energy using a buck-boost dc-dc converter to power active RFID tags is presented.
- Factors such as impedance matching, converter comparison and different transducer configurations are discussed

# Outline

- RFID tags
- Need for energy harvesting (EH)
- Transducer design requirements
- AC/DC and DC/DC conversion
- Impedance matching criteria
- Vehicle/asset tracking application
- Different configurations/Experimental results
- Future roadmap

# RFID Tags

- Passive
  - Reflects RF energy to reader
  - Low cost
- Active
  - Emits rather than reflects RF energy
  - Better performance/Higher cost
  - Limits maintenance-free operational life
  - Needs energy harvester



# Comparison of Power Sources

| Energy Scavenging Source | Power Density ($\mu W/cm^3$) | Information Source |
|---|---|---|
| Solar (Outdoors) | 15,000 – Direct Sun<br>150 – Cloudy Day | Commonly Available |
| Solar (Indoors) | 6 – Office Desk | Experiments |
| Vibrations | 100 - 200 | Roundy et. al. |
| Acoustic Noise | 0.003 @ 75 dB<br>0.96 @ 100 dB | Theory |
| Daily Temp. Variation | 10 | Theory |
| Temp. Gradient | 15 @ $10^o$ Celsius | Stordeur & Stark 1997 |
| Piezo Shoe Inserts | 330 | Starner 1996 |

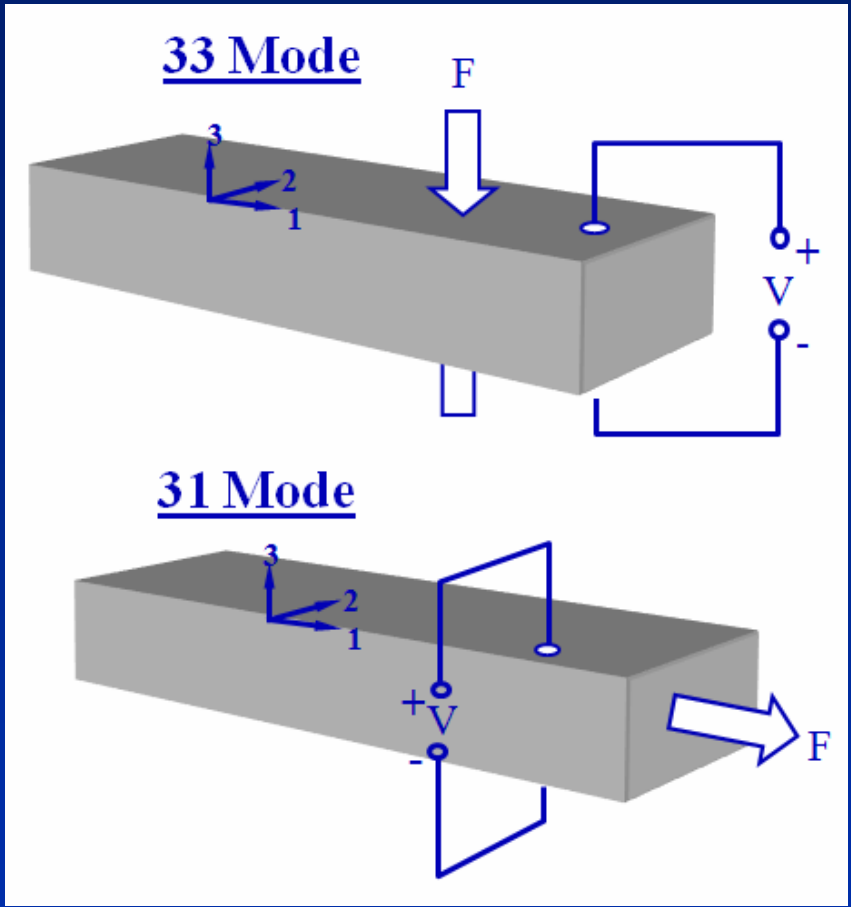
**Power densities of energy harvesting technologies.**

| Vibration source | $A$ ($m/s^2$) | $F_{peak}$ |
|---|---|---|
| Car engine compartment | 12 | 200 |
| Base of 3-axis machine tool | 10 | 70 |
| Blender casing | 6.4 | 121 |
| Clothes dryer | 3.5 | 121 |
| Person nervously tapping their heel | 3 | 1 |
| Car instrument panel | 3 | 13 |
| Door frame just after door closes | 3 | 125 |
| Small microwave oven | 2.5 | 121 |
| HVAC vents in office building | 0.2–1.5 | 60 |
| Windows next to a busy road | 0.7 | 100 |
| CD on notebook computer | 0.6 | 75 |
| Second story floor of busy office | 0.2 | 100 |

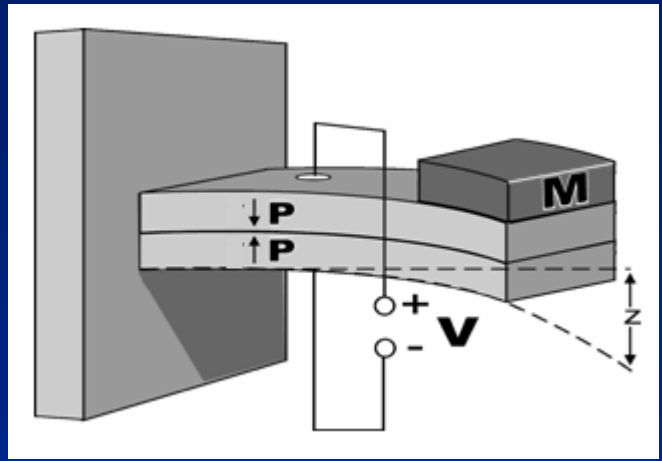
**Acceleration and frequency of various vibration sources.**

**Data source: Journal of Computer Communications, Vol. 26, S. Roundy, P. K. Wright, J. Rabaey, "A Study of Low Level Vibrations as a Power Source for Wireless Sensor Nodes", pp. 1131 - 1144, 2003.**

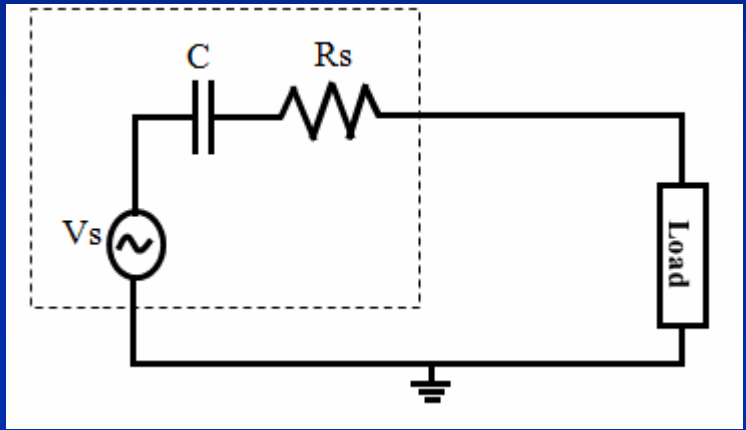
# Piezoelectric Conversion




Piezoelectric conversion modes




Cantilever configuration




Piezoelectric generator

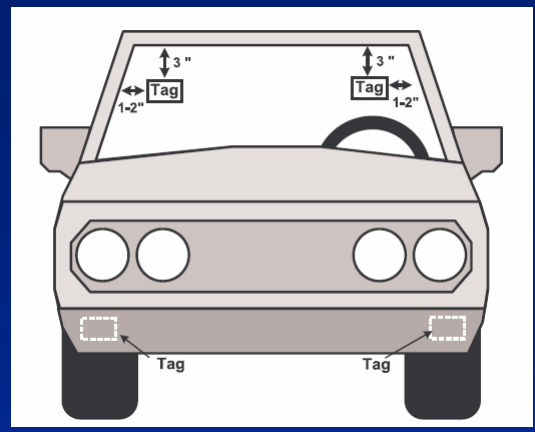
Figure courtesy: Shad Roundy, LV Sensors, Inc.

# Design considerations

- Study vibration profile of source
  - Frequency profile
  - Acceleration profile
- Design transducer to resonate at frequency of source
- Measure/calculate optimum load resistance (Ropt) for max power transfer
- Design converter @ Ropt
- Choice of rectifier topology
- Choice of converter topology

# RFID Tag Applications

- Vehicle tags
  - Access control
  - Payload security and inventory
  - Fleet turnaround management
  - Condition sensing
- Personnel tags
  - Time and attendance reporting
  - Asset utilization
- Asset tags
  - IT asset tags
  - Document containment
- Sensing tags
  - Cold chain delivery
  - Disaster recovery



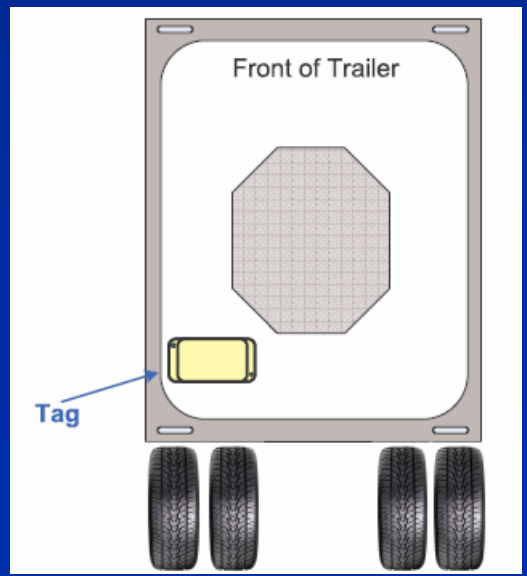
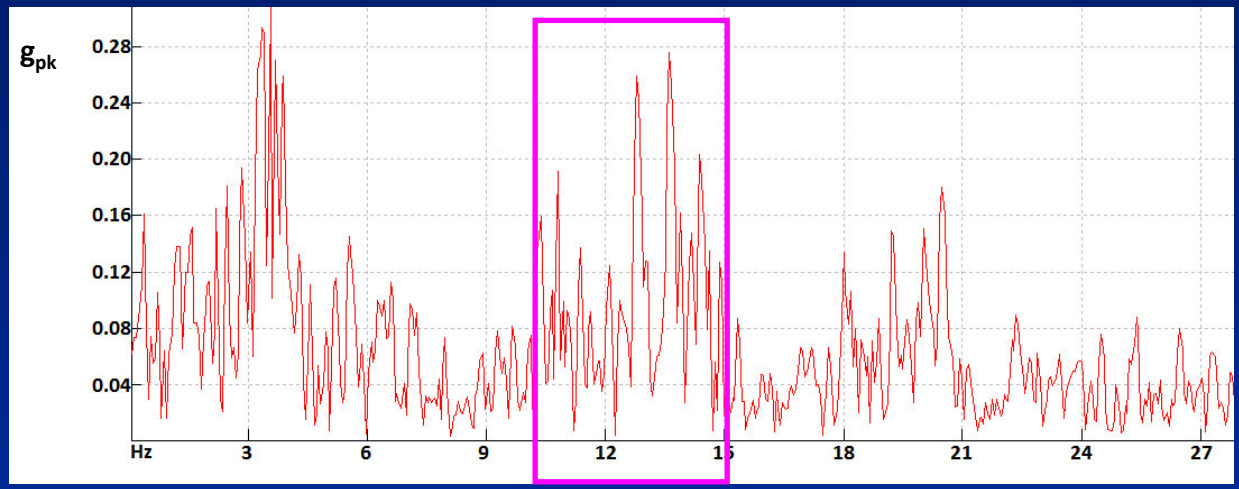
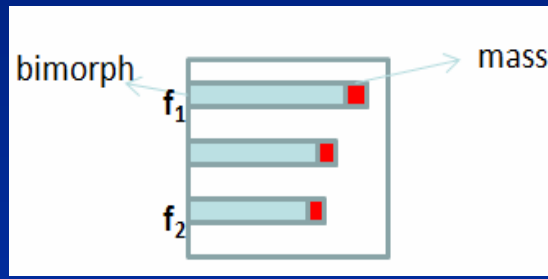
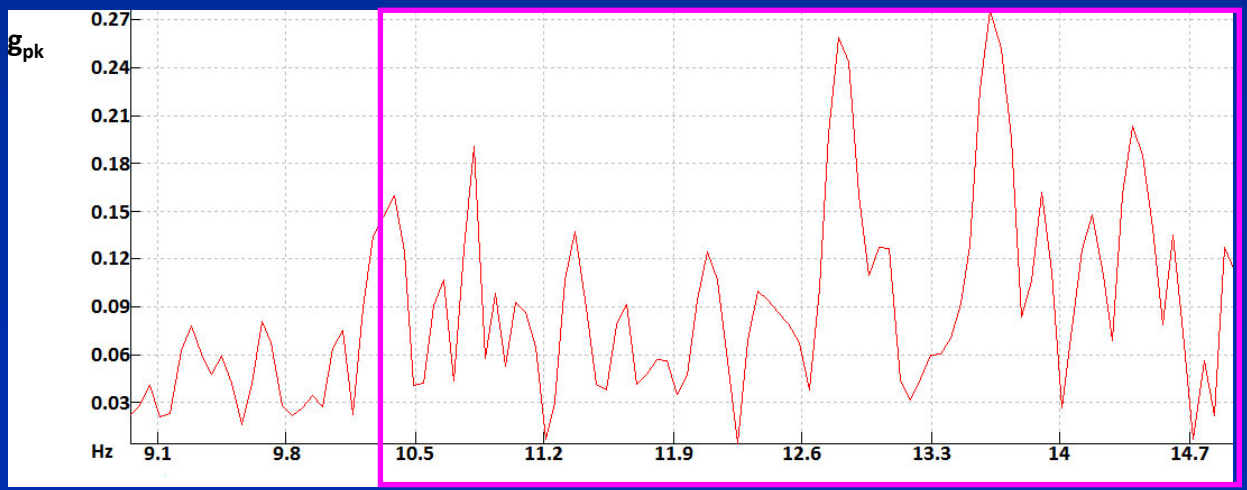




Photo courtesy: Axcess International, Inc.

# Vibration profile - 2003 Honda Civic



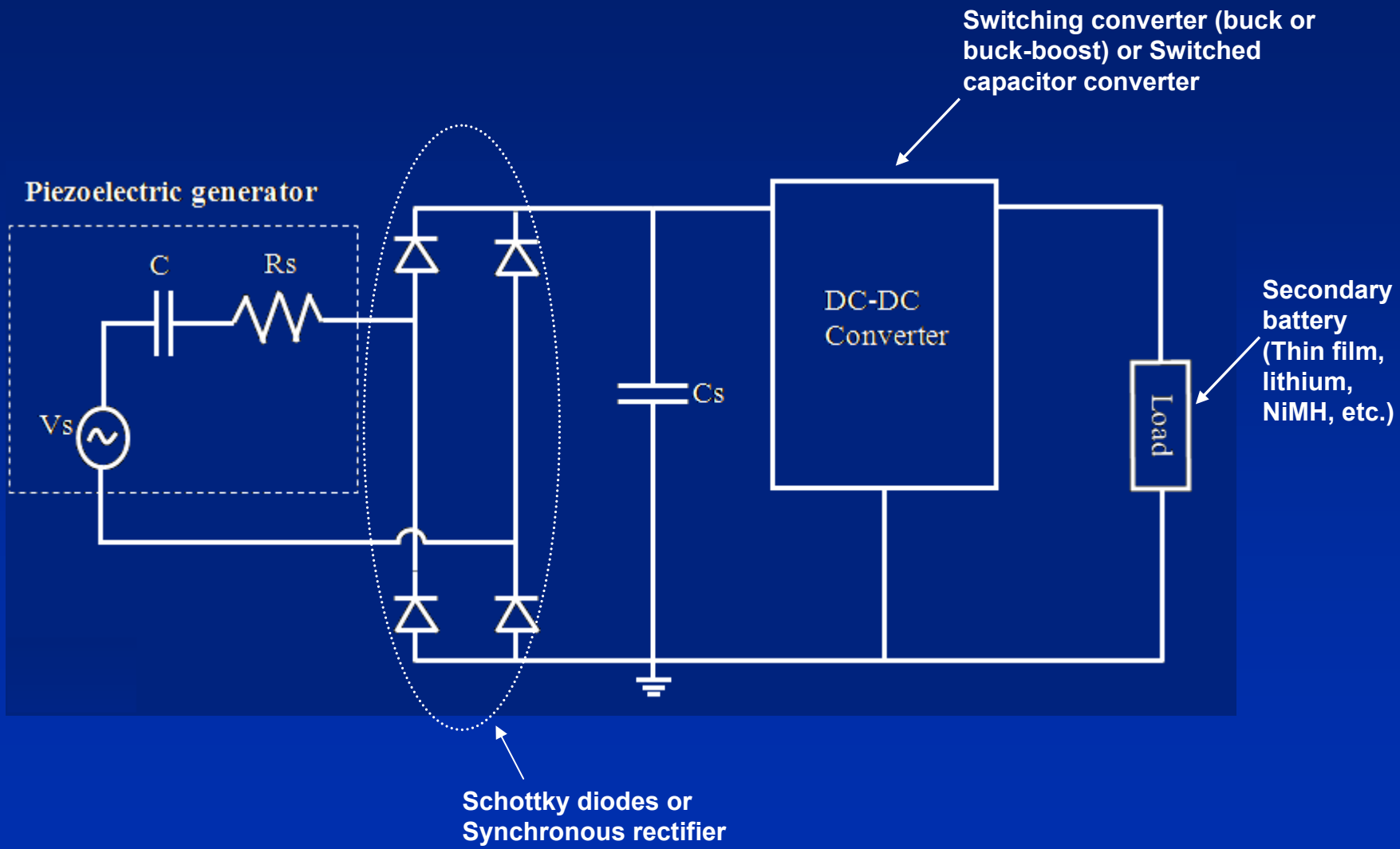




$f_1$ $f_2$

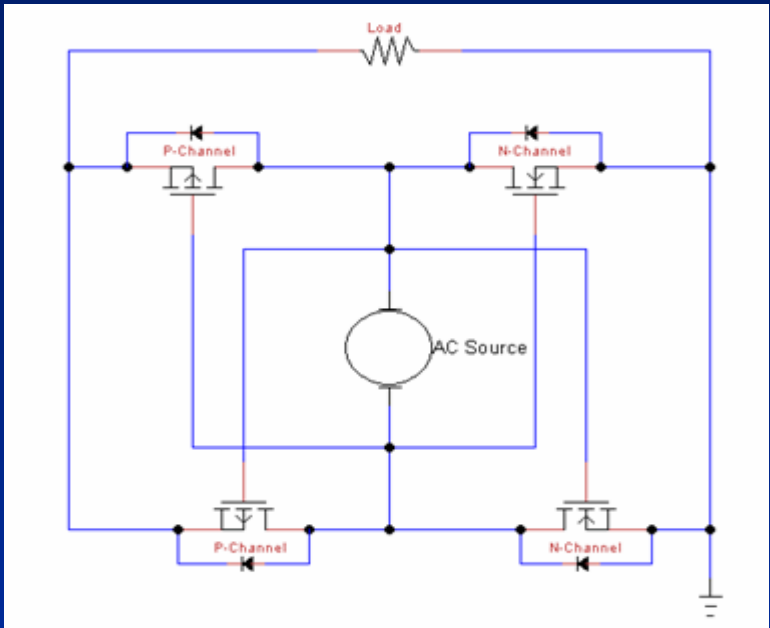
$f_1 \approx 10$ Hz

$f_2 \approx 15$ Hz

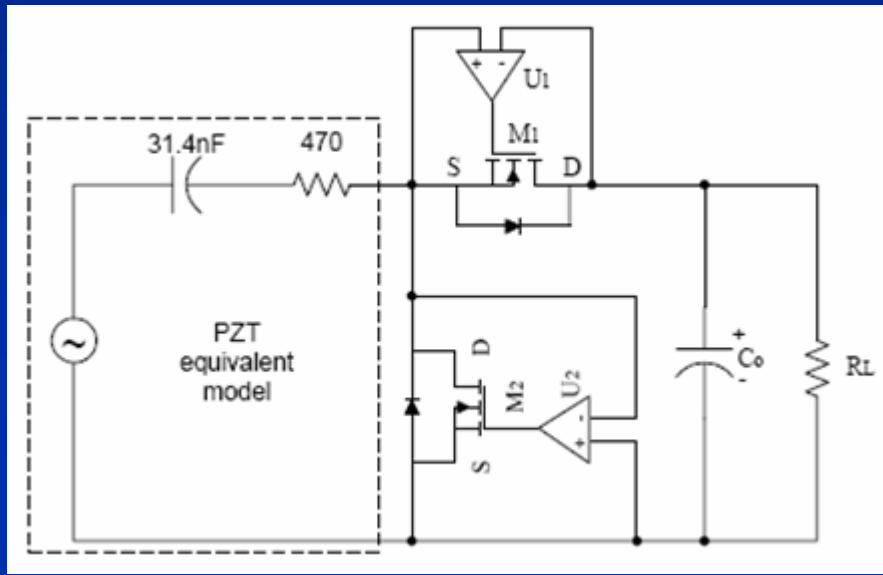
# EH Circuit for Piezo Converters



# AC/DC Conversion

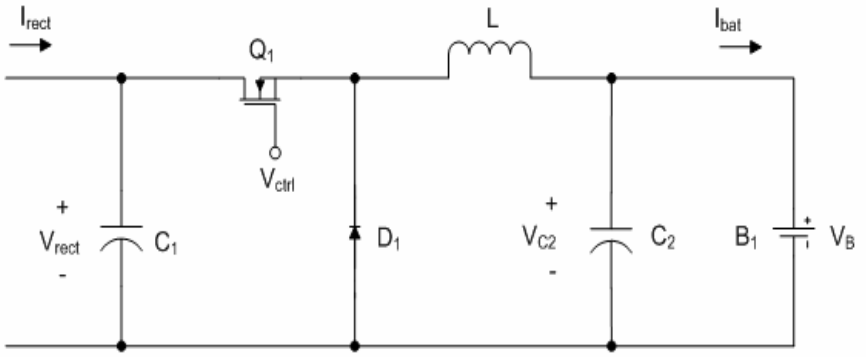



**Bridge rectifier w/ n-channel and p-channel MOSFETs**

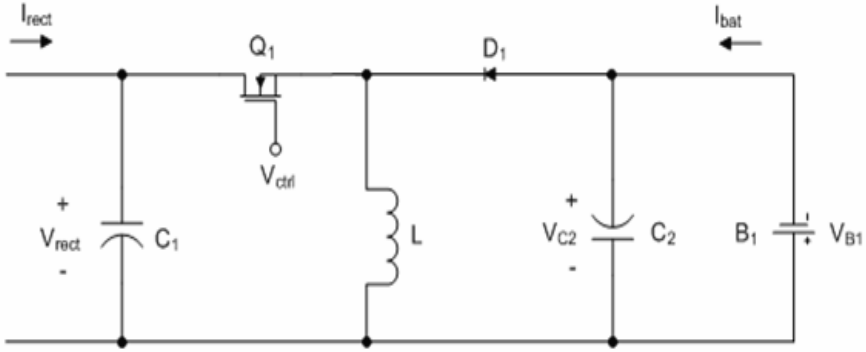



**Diode pair rectifier w/ comparators**

# DC-DC Converter Topologies




DC-DC buck converter with battery load (discontinuous conduction mode).

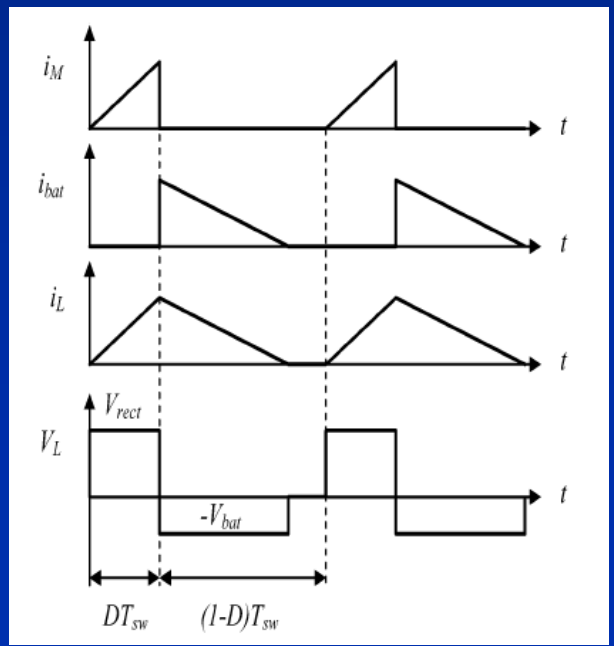



DC-DC buck-boost converter with battery load (discontinuous conduction mode).

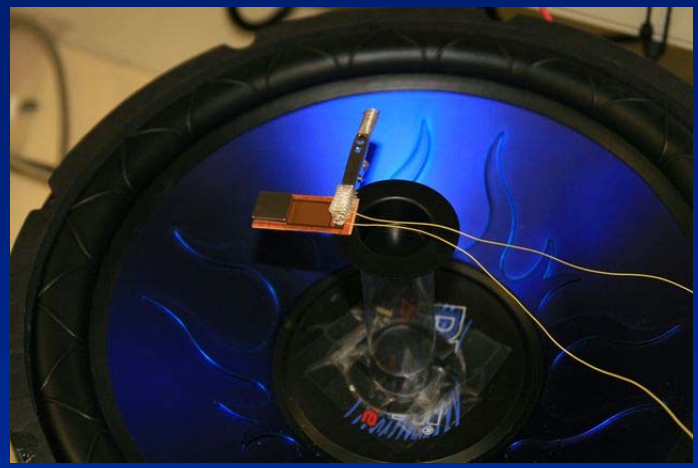
Constraint: $V_{rect} < \frac{1-D}{D} V_{bat}$.

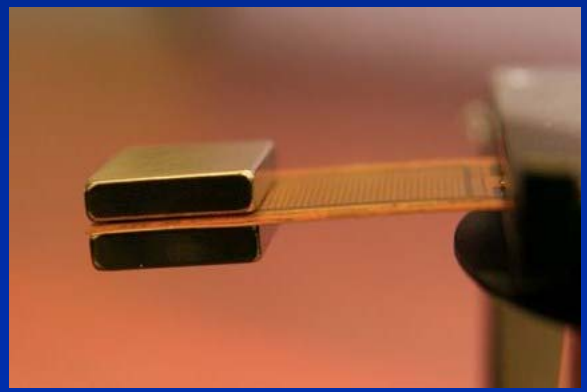
Use feedback and feedforward techniques to tune $V_{ctrl}$ to achieve impedance matching

Constraint: $V_{rect} >> V_{bat}$



# Experimental Set-up





Speaker/amplifier set-up


Acceleration = 0.1 - 5g @ 15 Hz - 30 kHz.

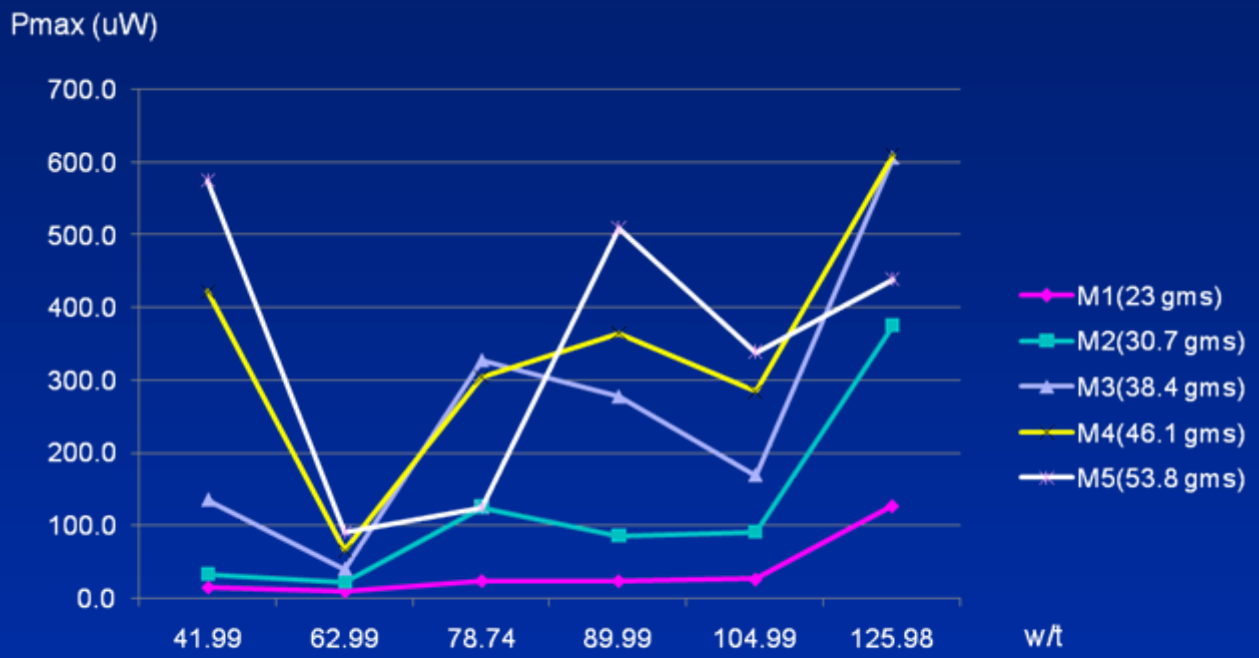
Smart Material Inc., M2814P2 PZT-5A patch
Patch size: 36 x 16 x 0.3 $mm^3$
Al (alloy 1100) cantilever beam
Neodymium-Iron-Boron proof (tip) mass

# MFC Cantilever tests

- Experiments conducted @ 0.25 $g_{pk}$ excitation with one 2814 P2 MFC patch
  - Power ($P_{max}$) vs. Beam thickness ($t$)
  - Voltage ($V_{oc}$) vs. Tip mass ($m$)
  - $P_{max}$ vs. $m$

- Observations
  - Higher $V_{oc}$ as $m$ is increased
  - Lower $t$ => lower resonant frequency ($f_r$)
    - However, at low $t$ (<= 0.2 mm) beam bends with high $m$ (>= 38 gm)
  - Optimum thickness ($t_{opt}$) = 0.381 mm (0.015”)

# $P_{max}$ vs. $t$ @ different $m$



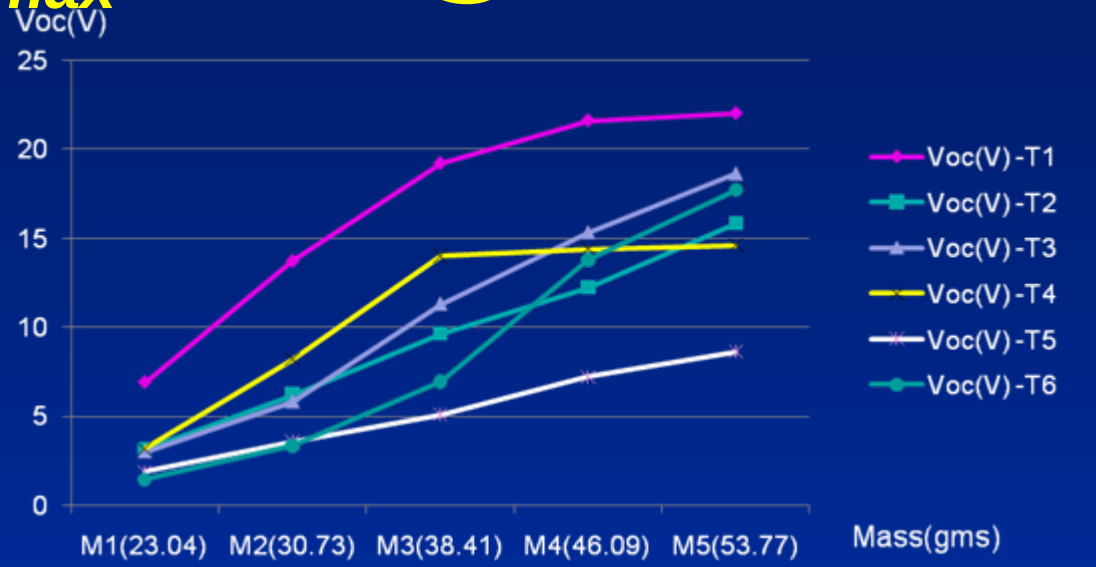

| | | | | | | |
|---|---|---|---|---|---|---|
| 154 | 97 | 95 | 127* | 111* | 98* | M1 |
| 119 | 70 | 74 | 103* | 89* | 80* | M2 |
| 100 | 55 | 60 | 83* | 70* | 61* | M3 |
| 86 | 46 | 44 | 66* | 54* | 48* | M4 |
| 74 | 41 | 36 | 54* | 43* | 37* | M5 |

**w = 16 mm (fixed)**
**$t_1$ = 0.127 mm => w/$t_1$ = 125.98**
**$t_2$ = 0.152 mm => w/$t_2$ = 104.99**
**$t_3$ = 0.178 mm => w/$t_3$ = 89.99**
**$t_4$ = 0.203 mm => w/$t_4$ = 78.74**
**$t_5$ = 0.254 mm => w/$t_5$ = 62.99**
**$t_6$ = 0.381 mm => w/$t_6$ = 41.99**

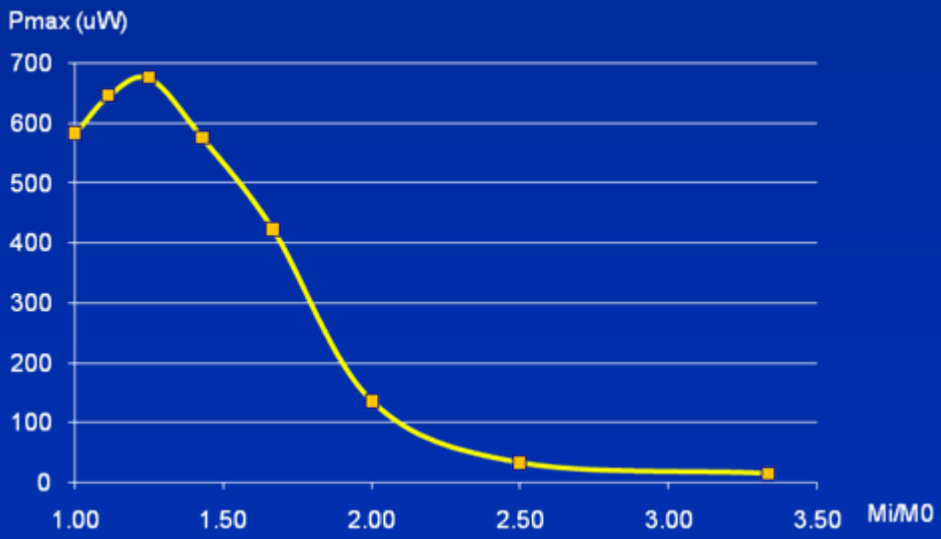
**Resonant frequencies at different thicknesses and mass**

*** Beam bent due to high tip mass (must avoid these thicknesses)**

# $V_{oc}$, $P_{max}$ vs. $m$ @ different $t$




$t_1$ = 0.127 mm
$t_2$ = 0.1524 mm
$t_3$ = 0.1778 mm
$t_4$ = 0.2032 mm
$t_5$ = 0.254 mm
$t_6$ = 0.381 mm



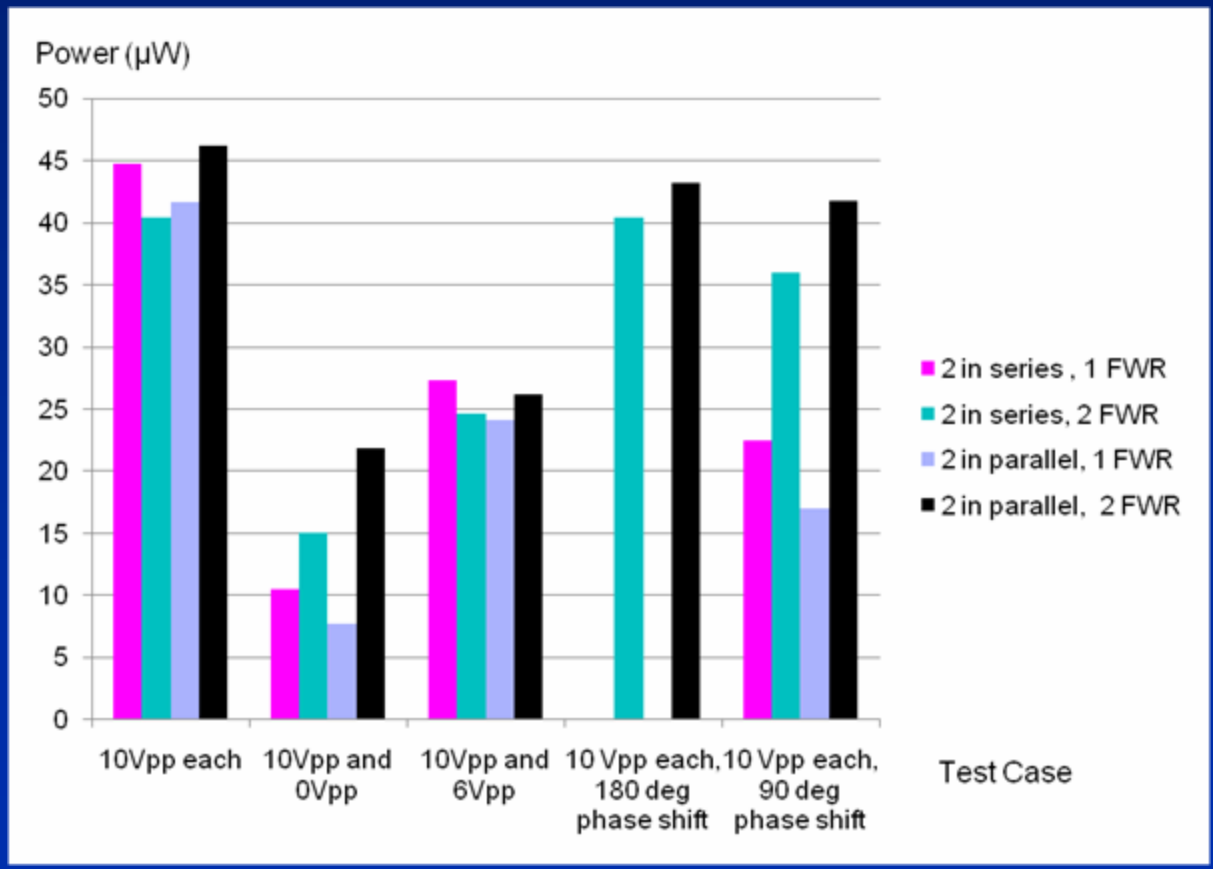

| Mi (gms) | Mi/M0 |
|---|---|
| 76.8 | 1.00 |
| 69.13 | 1.11 |
| 61.45 | 1.25 |
| 53.77 | 1.43 |
| 46.09 | 1.67 |
| 38.41 | 2.00 |
| 30.76 | 2.50 |
| 23.04 | 3.33 |

T6(mm) = 0.381

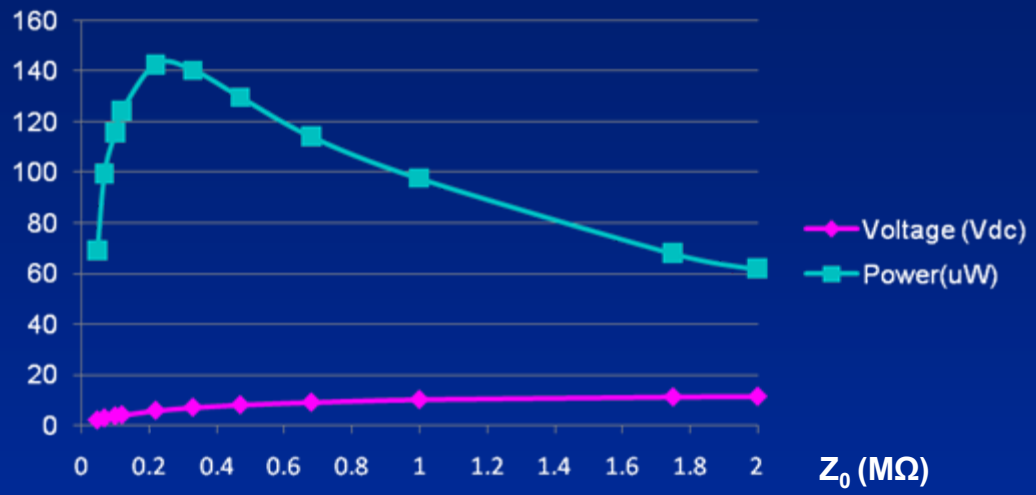
M0 = 76.81 gms for fR=45Hz

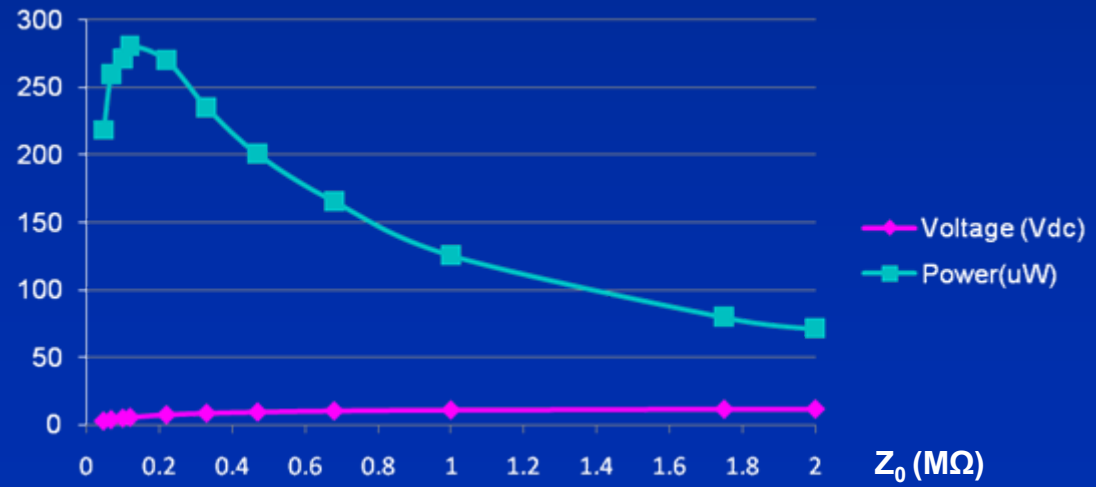
# Serial vs Parallel configurations
# 2 MFC2814P2 patches

$f_R$=40Hz, Acceleration = 0.07gPeak



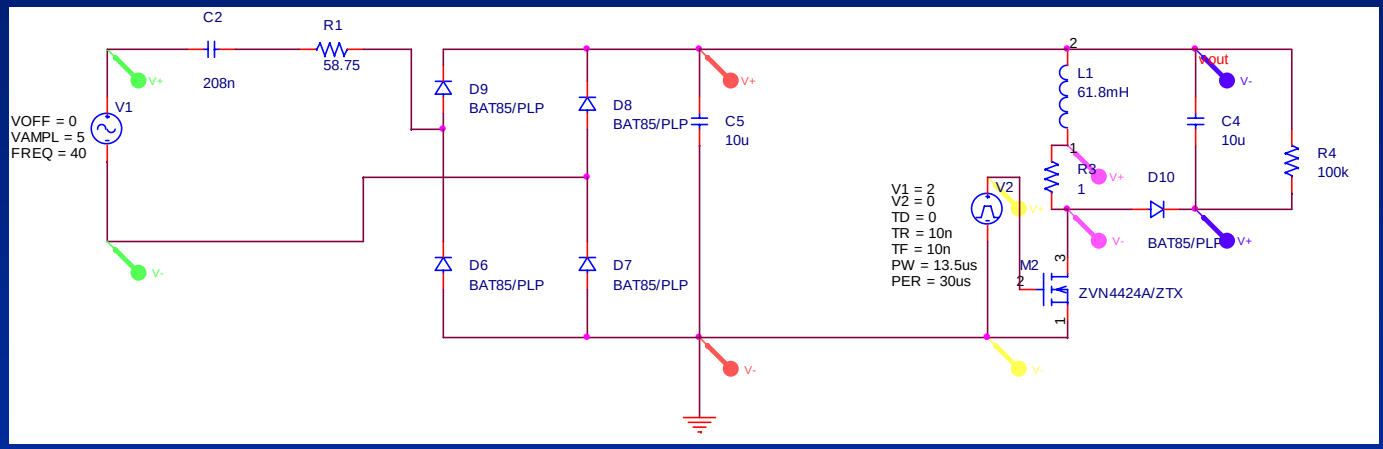
# Experimental Results - Single transducer and 2 in parallel

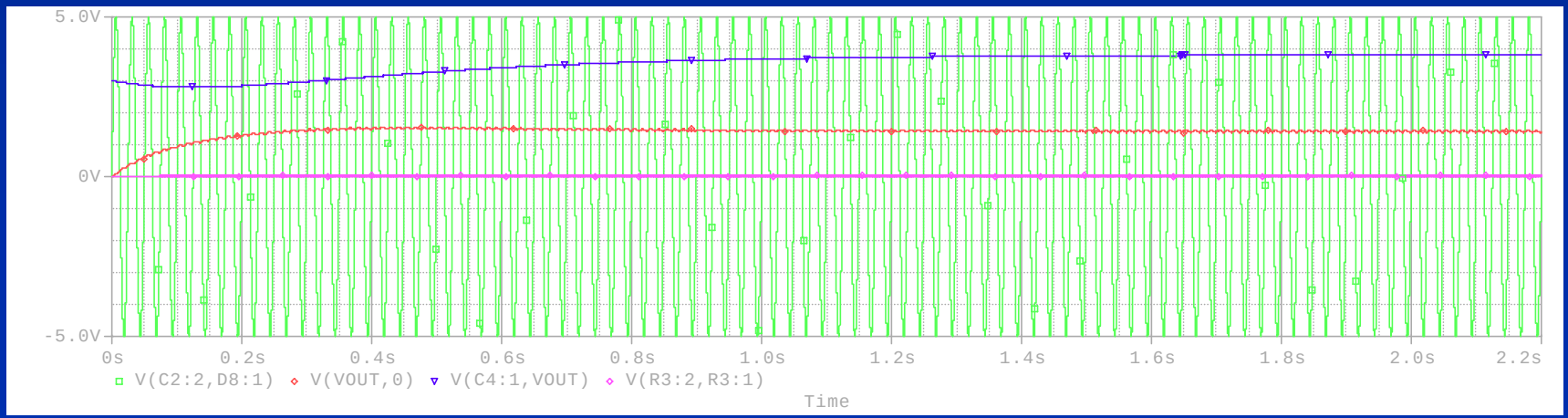


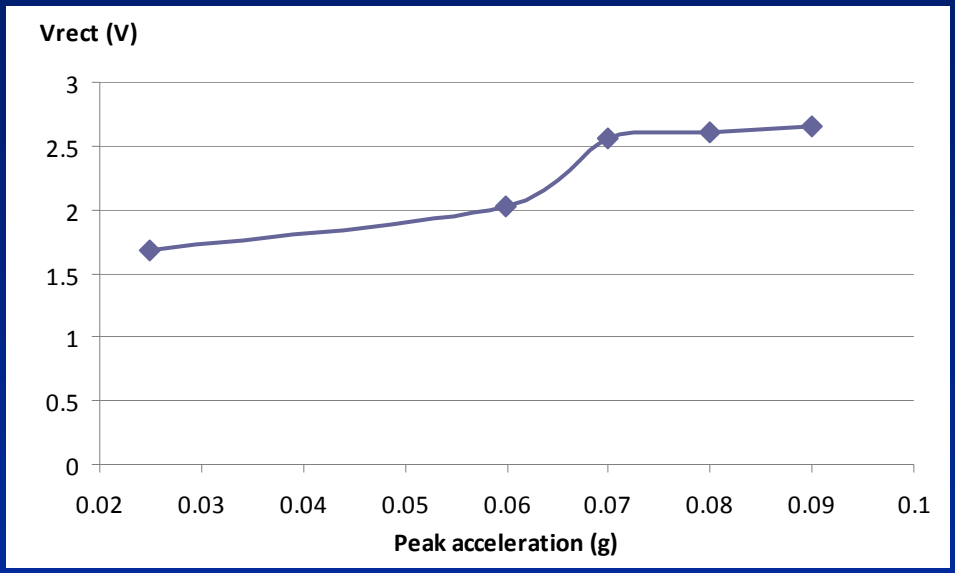
# DC-DC Conv. Simulation Results
# 8 transducers in parallel

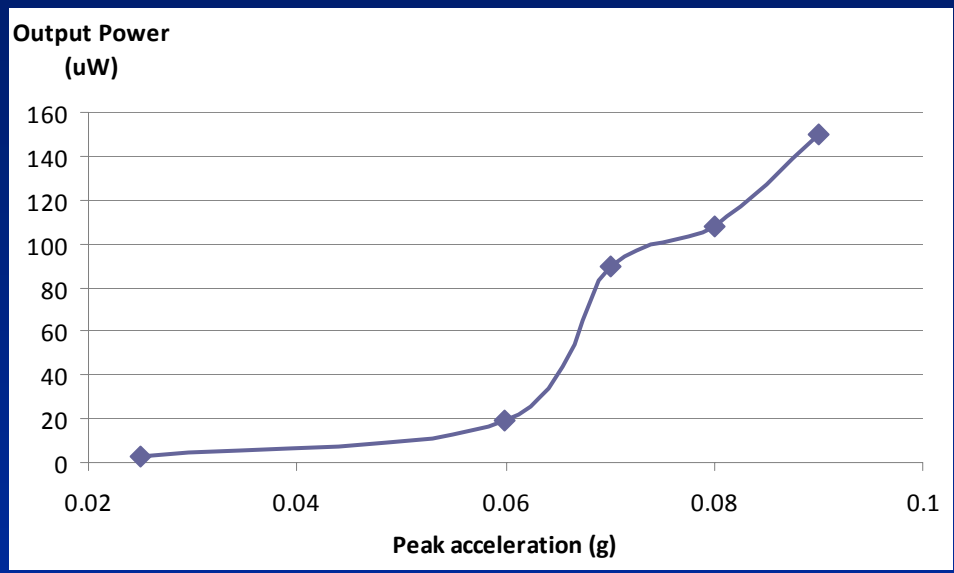
## Charged capacitor with 100k load

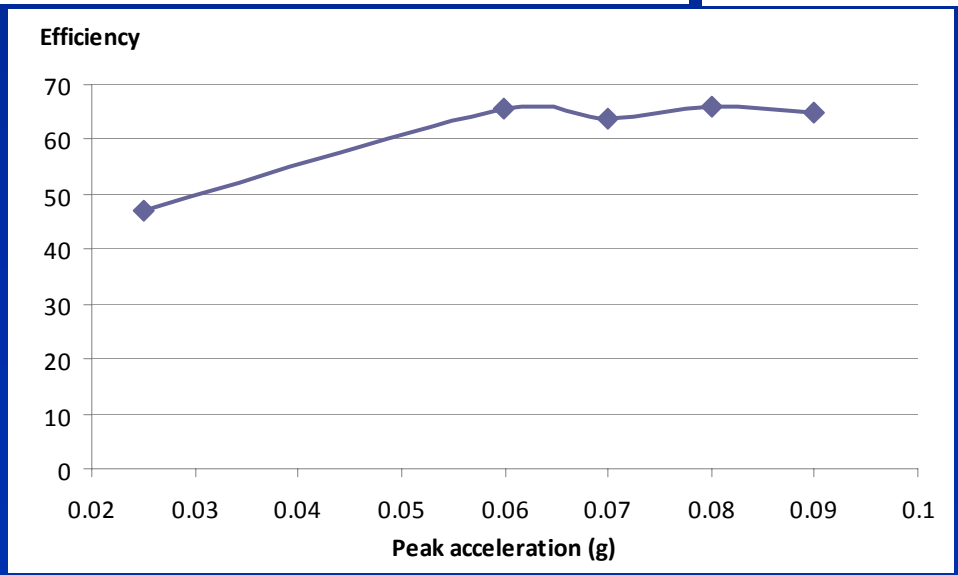


# DC-DC Converter Experimental Results
# 2 MFC2814P2 patches in parallel

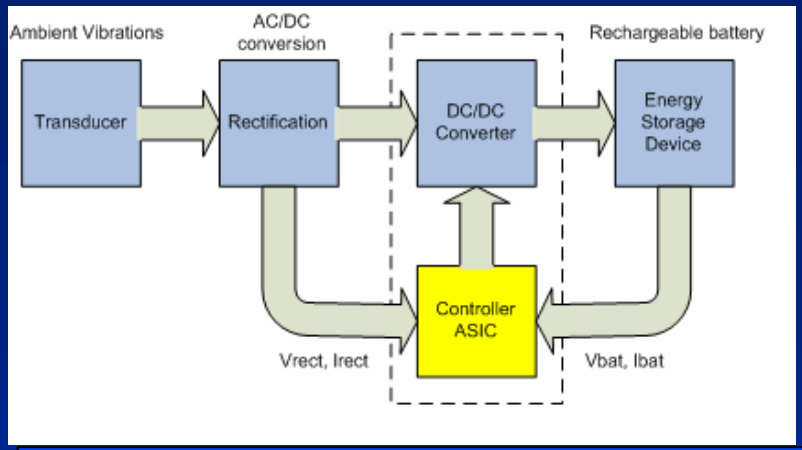


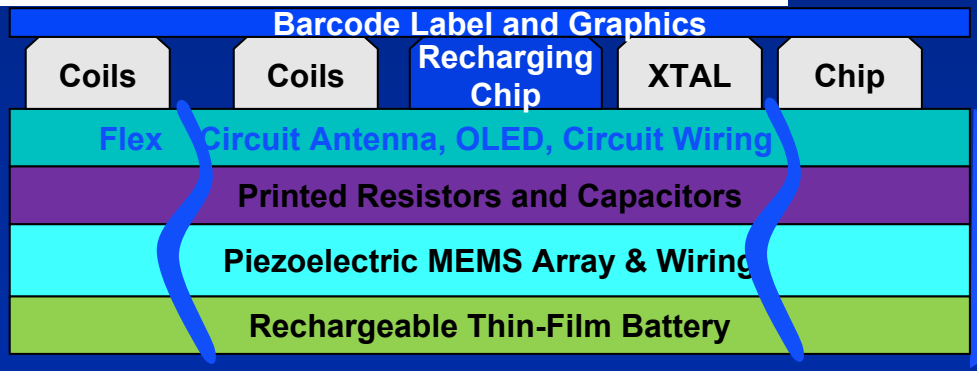




**Efficiency > 80% @ excitation > 0.5 $g_{pk}$**

# Future work - Integrated EH Sensor




Power management to tune $R_{in}$ of DC/DC converter to $R_{out}$ of transducer (impedance matching).




Overall MEMS piezoelectric EH sensor architecture

Roll-to-roll manufacturing

Texas Piezoelectric

UTD

# Conclusion

- Design of EH circuits for WSN nodes is very important  due to limited life of battery
- EH from vibrations can replenish idle energy consumption and extend battery life
- Off-the-shelf converters do not meet the specifications and efficient electronics are essential
- Further optimization and implementation on a chip would lead to better efficiency


*3rd Austin Conference on Integrated Systems & Circuits 2008*

*An Invited Talk*

# Receivers Design:

## CASE STUDIES

**Hesam Amir-Aslanzadeh**

**Dr. Edgar Sánchez-Sinencio**

**Email: Hesam@ece.tamu.edu**

**Analog and Mixed Signal Center (AMSC), Texas A&M University**

**http://amsc.tamu.edu, May 8th 2008**

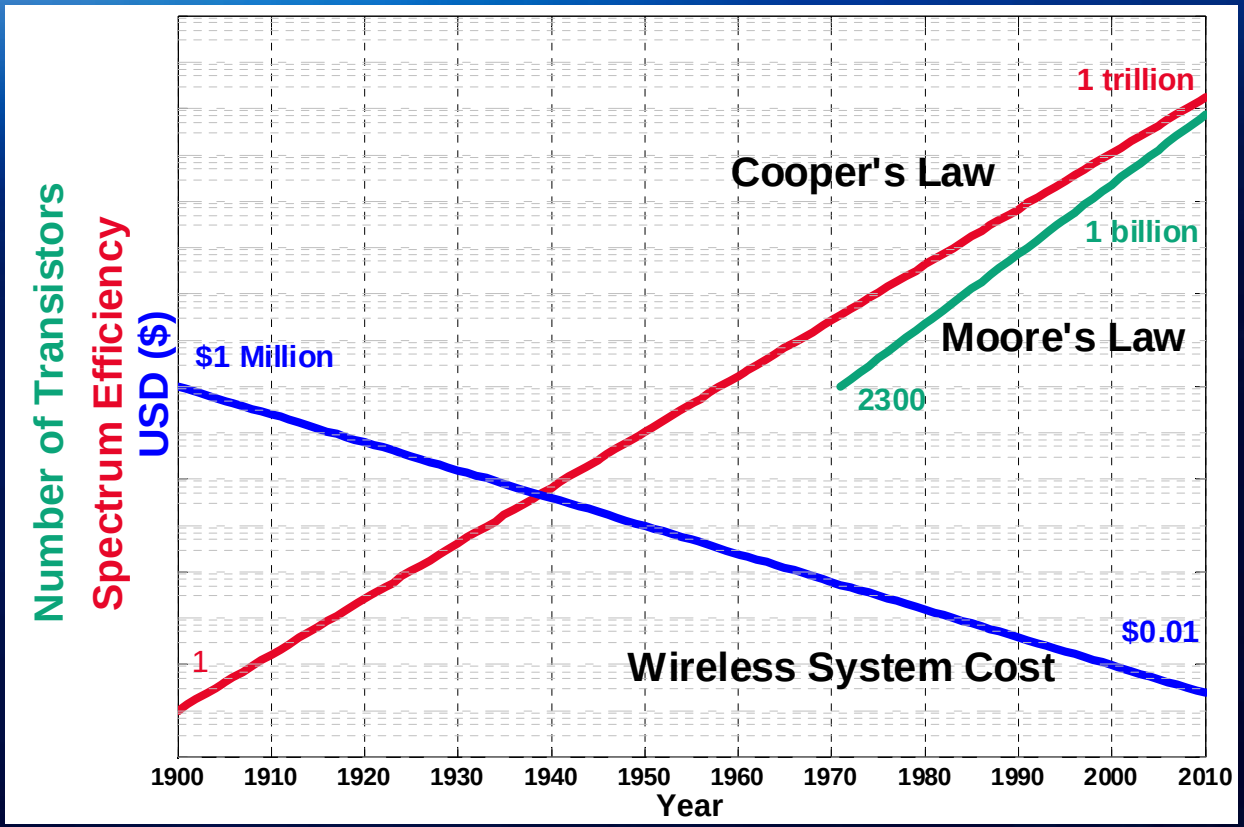
# Purpose:

- Discussing Receiver Design Decisions
  - Architectures
  - Technology
- Future Trends
  - Applications
  - Technology
  - Standards

# Outline

- Introduction: Wireless Revolution?
- Architecture Selection
- Case Studies:
  - Radios Designed in AMSC
- Recent Trends
- Emerging Technologies
- Conclusion

# Wireless Revolution?



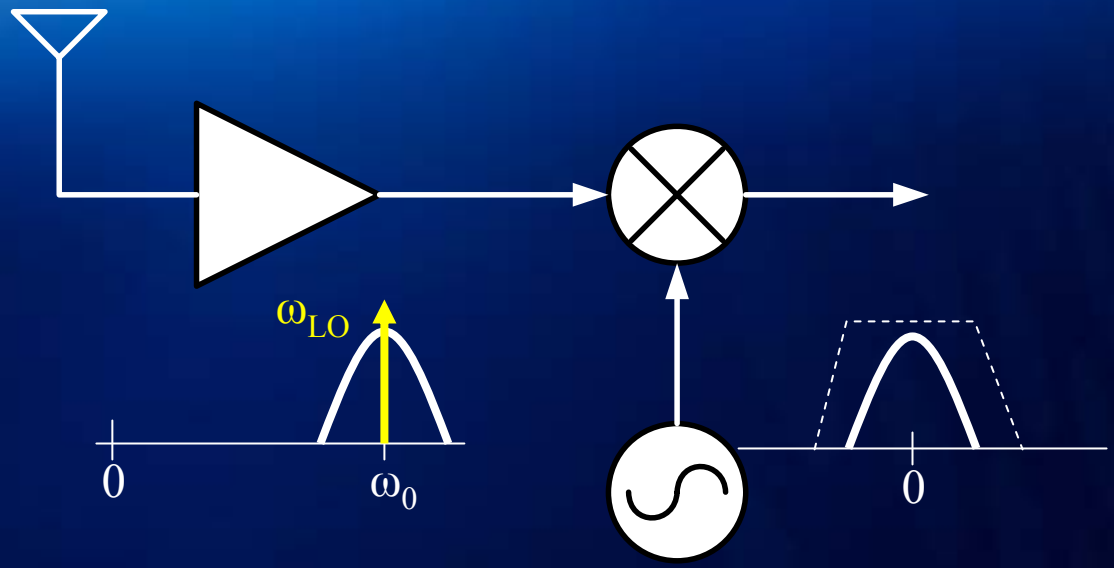

- *Moore's Law*: number of transistors double every 2 years
- Cooper's Law: Spectrum efficiency doubles every 2 ½ years
- Wireless systems cost per delivery halves almost every 5 years

Source: *Intel*; *Martin Cooper (ArrayComm)*

# Wireless Standards

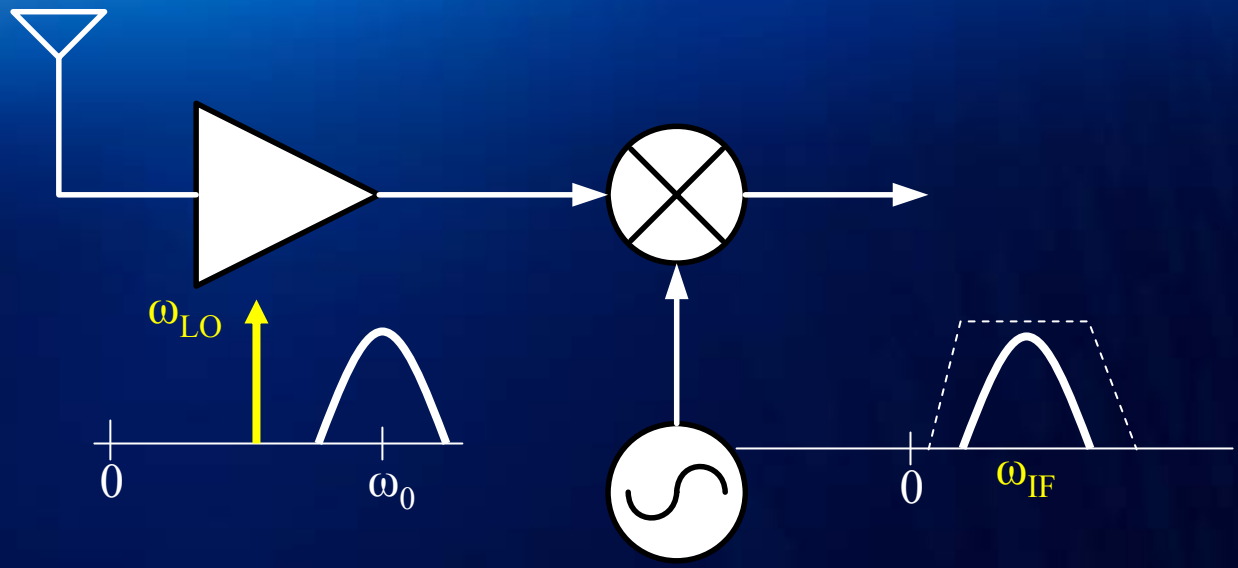
| | Data Rate | Range | Cost |
|---|---|---|---|
| WiMax | 15 Mb | 5 km | $8 |
| 3G | 14 Mb | 10 km | $6 |
| WiFi | 54 Mb | 50-100 m | $4 |
| Bluetooth | 700 kb | 10m | $1 |
| ZigBee | 250 kb | 30m | $4 |
| UWB | ~400Mb | 5-10m | $5 |
| RFID | 1-200kb | 0.01-10m | $0.04 |

# Direct Conversion

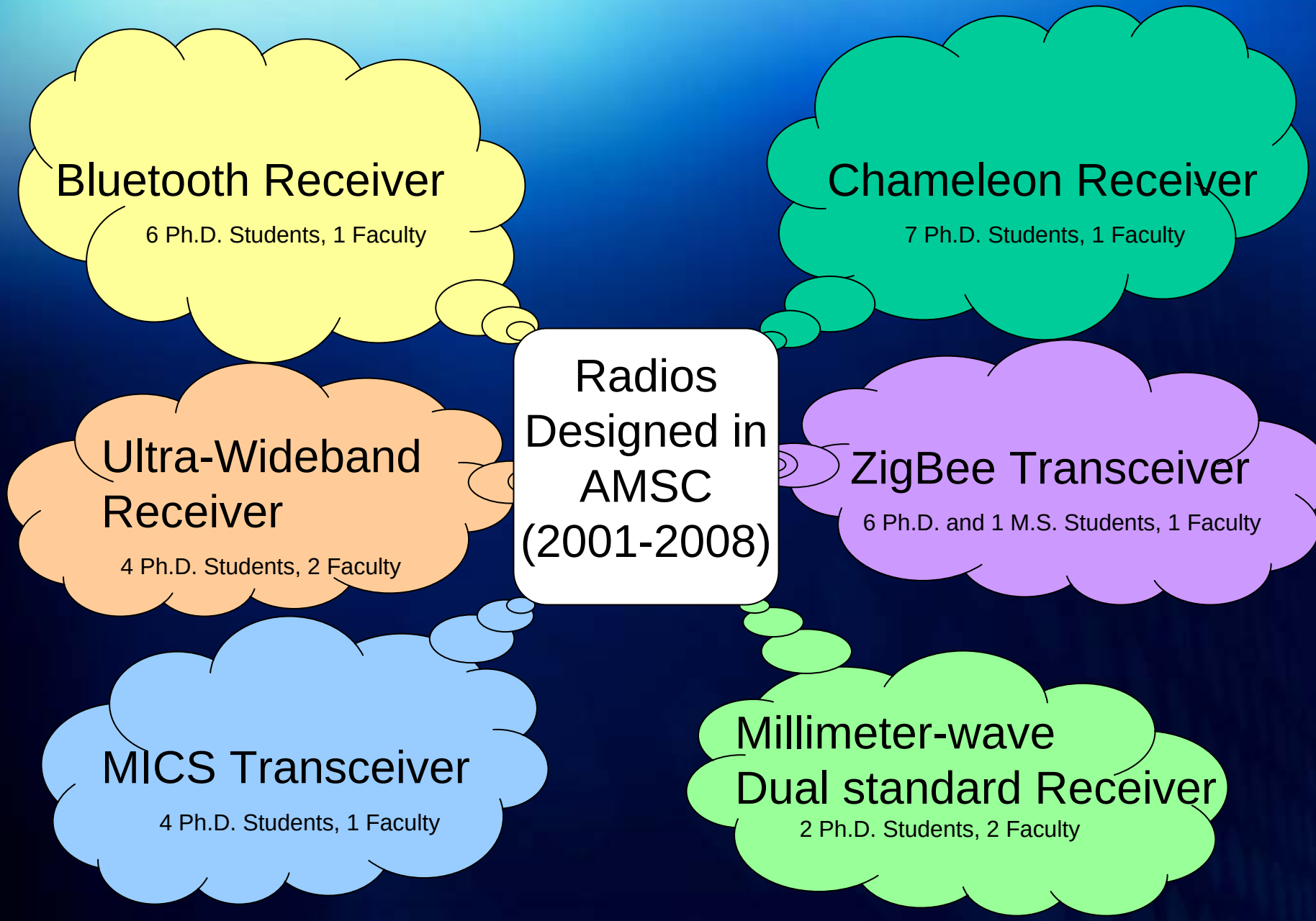



- High level integration.
- No image rejection required.
- Less components, possible low power consumption
- DC offset.
- Flicker Noise

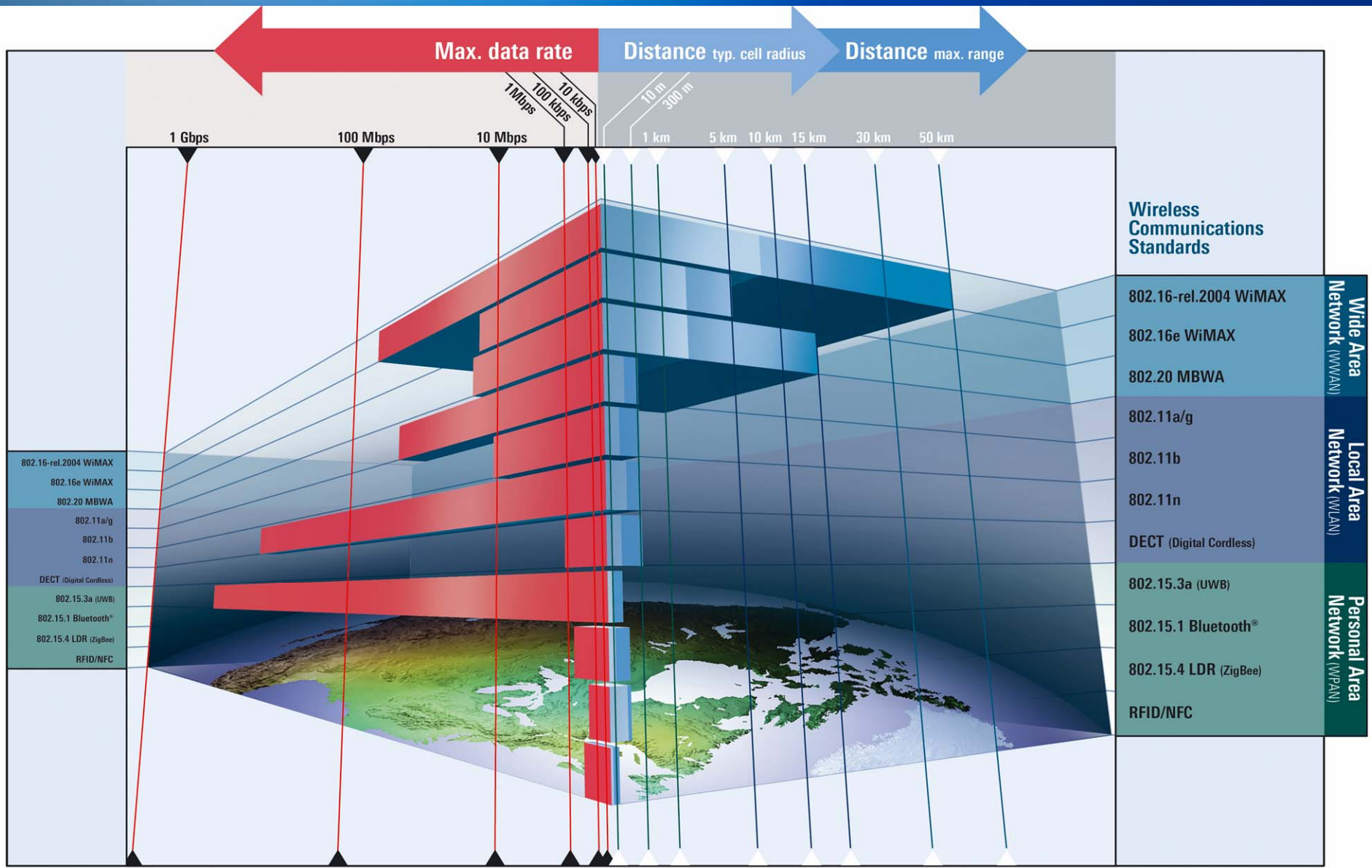
# Low IF Receiver




- High level integration and possible low power design
- Flicker noise less significant in signal band
- DC offset can be easily removed
- Image rejection
- Folded-back interference


Radios Designed in AMSC (2001-2008)
Bluetooth Receiver
6 Ph.D. Students, 1 Faculty
Chameleon Receiver
7 Ph.D. Students, 1 Faculty
Ultra-Wideband Receiver
4 Ph.D. Students, 2 Faculty
ZigBee Transceiver
6 Ph.D. and 1 M.S. Students, 1 Faculty
MICS Transceiver
4 Ph.D. Students, 1 Faculty
Millimeter-wave Dual standard Receiver
2 Ph.D. Students, 2 Faculty

# Data rate/Range



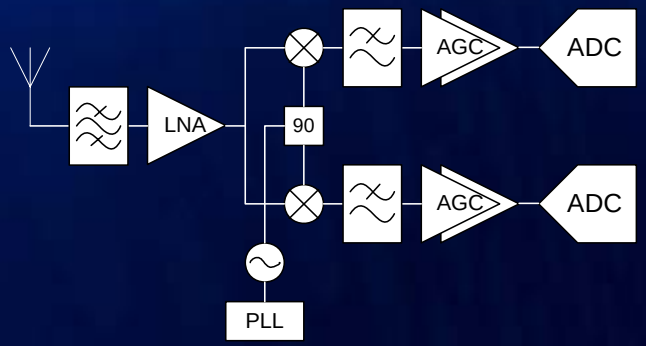
# Bluetooth

Applications


# Bluetooth Architectures

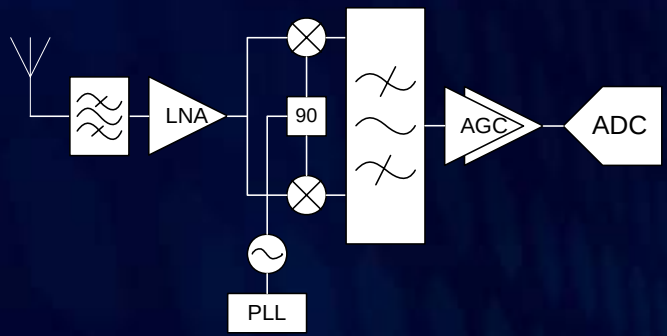
## Direct-Conversion Receiver

- DC offset and flicker noise problem: 99% of signal power is within DC to 430kHz.
- A fast settling AGC may be required for GFSK demodulation.

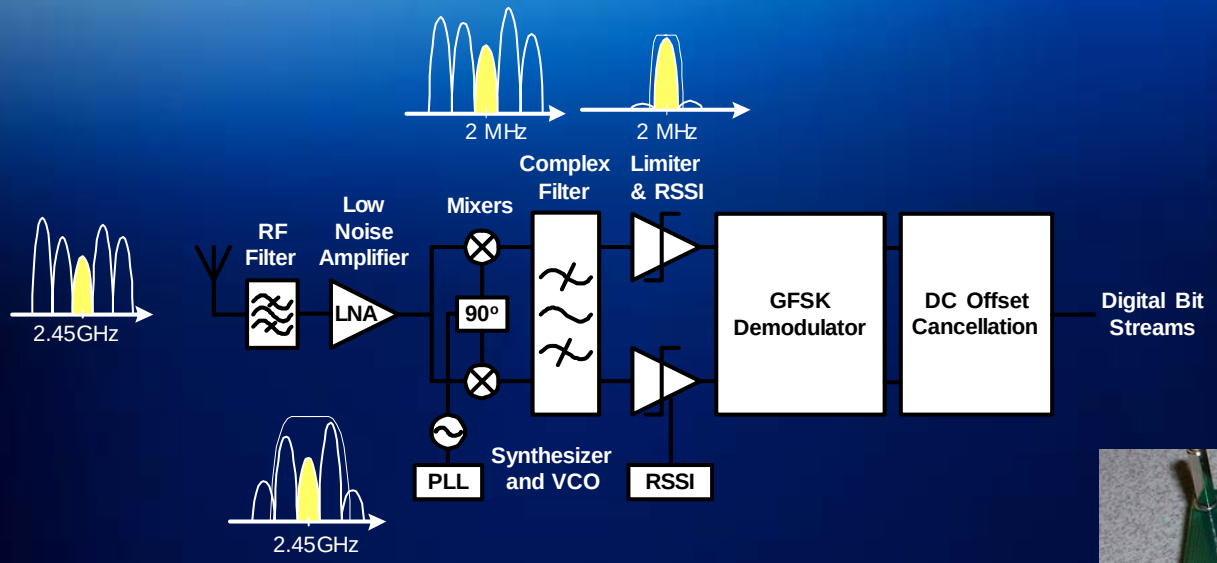


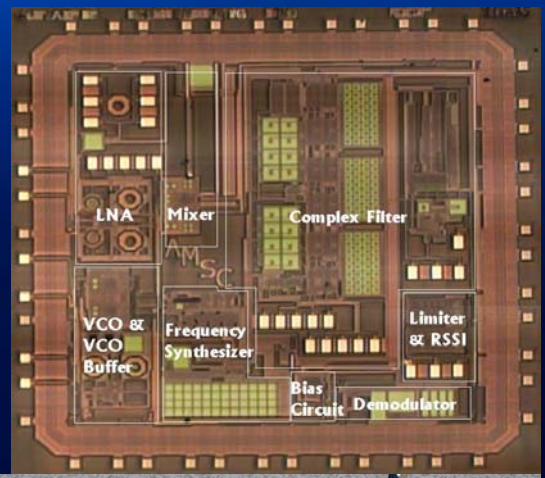

## Low-IF Receiver

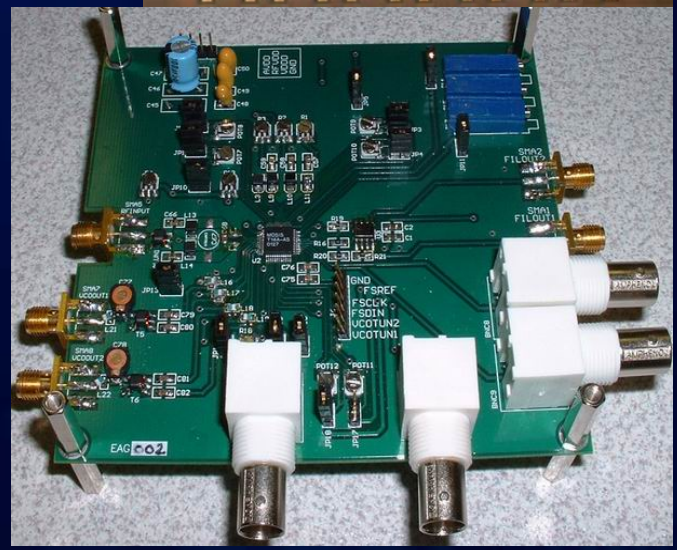
- Greatly alleviated DC offset and Flicker noise problem.
- Relaxed image rejection requirement (~33 dB).



# AMSC Bluetooth*



- ISM Band
- GFSK Signal
- Low-IF Quadrature
- Analog demodulator
  - No ADC, No AGC

* W. Sheng, B. Xia, A. Emira, C. Xin, A. Valero-López, S. Moon, E. Sánchez-Sinencio, "**A 3-V, 0.35um CMOS Bluetooth Receiver IC**" *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 1, Jan. 2003

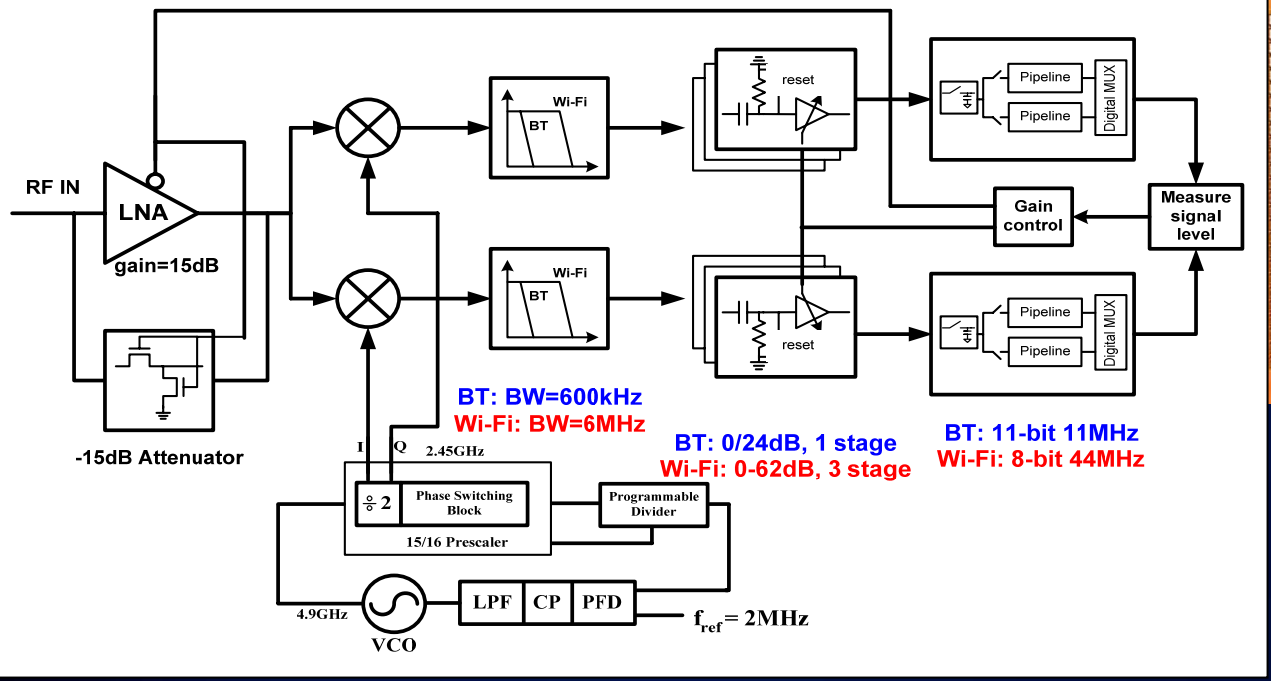
# Chameleon (Bluetooth/WiFi)

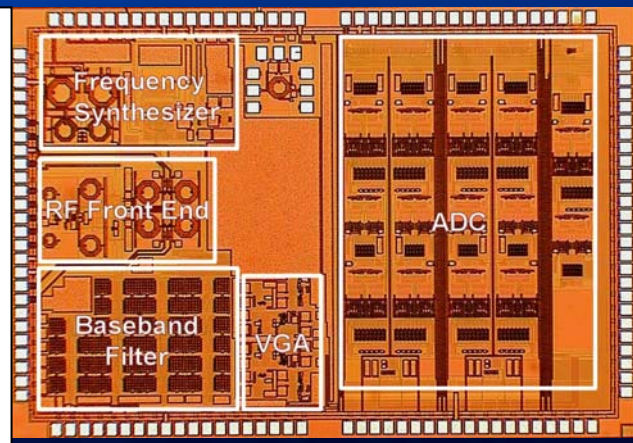
Applications

# Standard comparison

| | Bluetooth | Wi-Fi |
|---|---|---|
| RF Frequency | 2.4GHz | 2.4GHz |
| Sensitivity | -70dBm | -80dBm |
| Maximum Signal | -20dBm | -4dBm |
| Modulation | GFSK | CCK |
| Data rate | 1Mb/s | 1, 2, 5.5, 11Mb/s |
| Channel Bandwidth | 1MHz | 22MHz |

# Chameleon* (Wifi /Bluetooth)




- Direct conversion allows for maximum block sharing
- Shared RF front-end and programmable baseband components
- Programmable channel selection filter with constant linearity
- AC coupled VGA with constant output offset
- On-chip time-interleaved pipeline ADC

* A. A. Emira, A. Valedes-Garcia, B. Xia, A. N. Mohieldin, A. Y. Valero-López, S. T. Moon, C. Xin, E. Sánchez-Sinencio, "**Chameleon: A Dual-Mode 802.11b/Bluetooth Receiver System Design**" *IEEE Journal of Solid-State Circuits*, Vol. 53, No. 5, May 2006

# Ultra Wideband

Communication

# Ultra-Wideband Communication

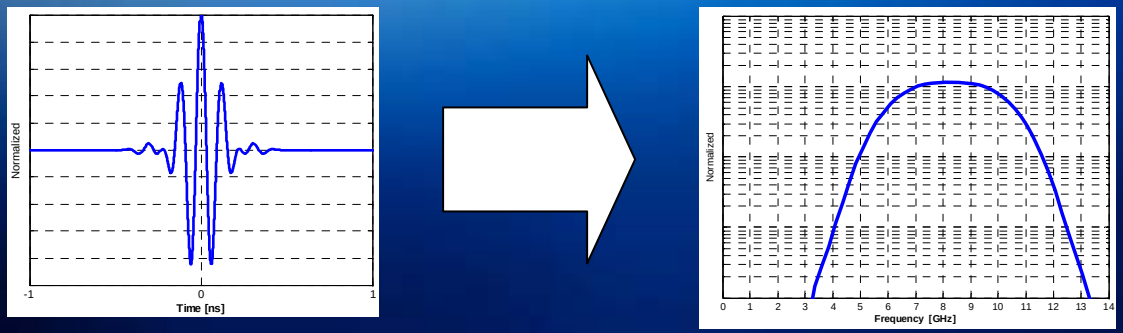
- UWB Applications
  - Certified wireless USB
    - **Hub and dongle adapter kits**
  - Embedded laptop solutions
  - Real Time Location System
- Late take-off in 2007
  - 40,000 units shipped in 2007
  - 400,000,000[1] predicted by 2013
  - Tremendous potential in handsets
  - Possibility of integration w/ Bluetooth


*Wireless USB (Courtesy of Belkin)*


*RTLS System (Courtesy of MultiSpectral Solutions)*

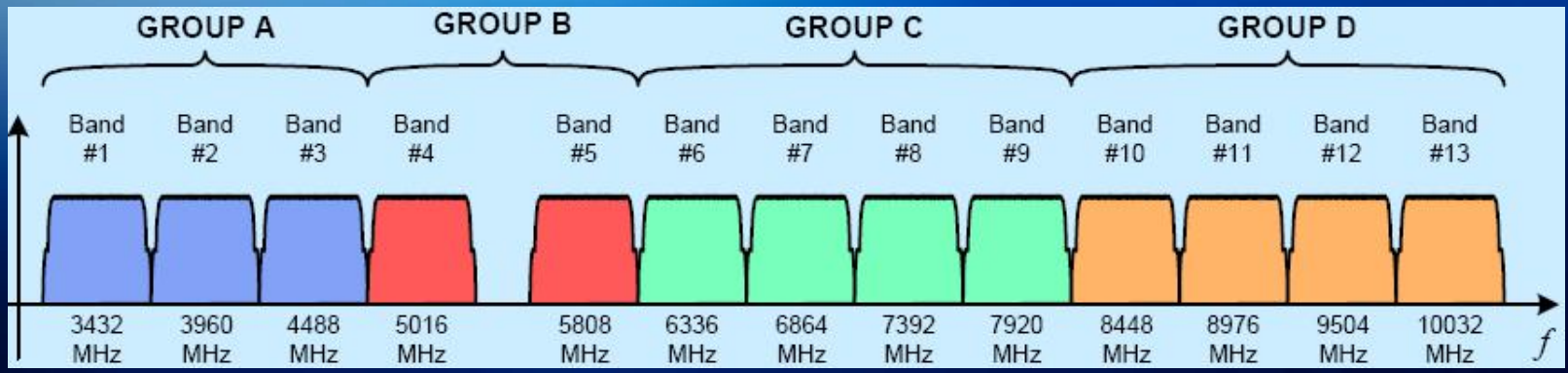
**[1] ABI Research prediction**

# Pulse-based UWB




- Short burst of electromagnetic energy
  - Efficient battery use
  - Multi-path fading immunity
  - Secure
  - High Crest factor (PAR)
  - Not immune to ISI
- Applications
  - Radar/Imaging (1-100M Pulse/S)
  - Precision Asset localization
  - RFID
  - Communication (1-2G Pulse/S)

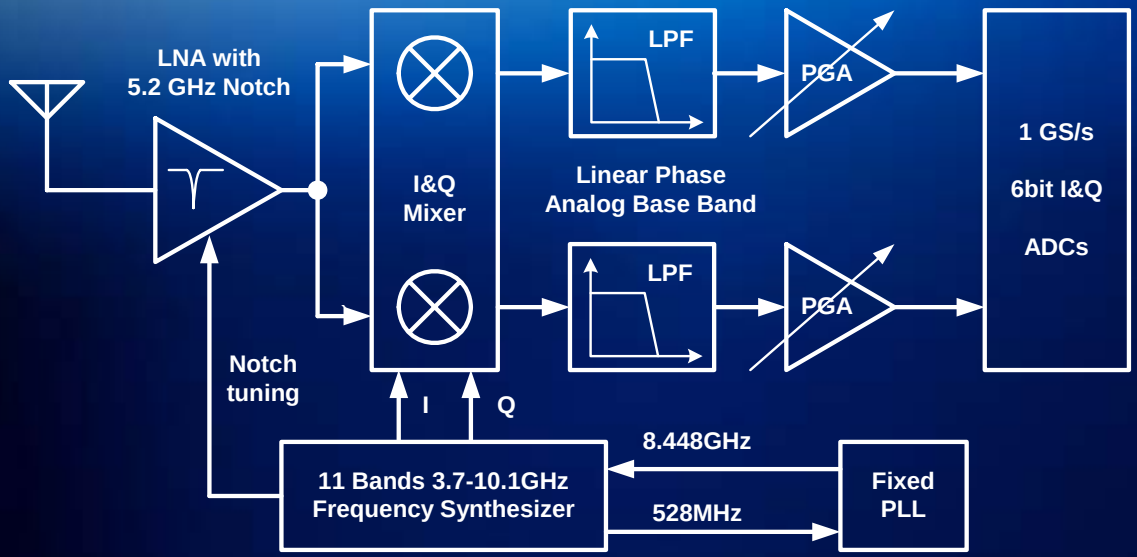
# MB-OFDM UWB

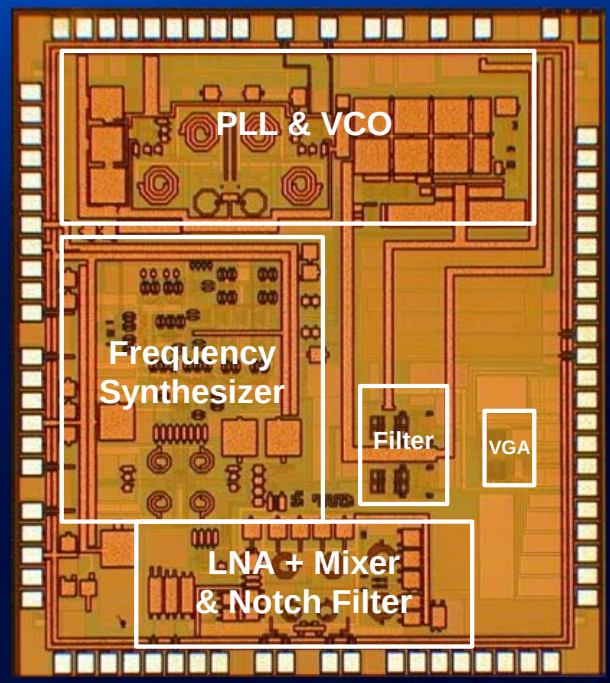



- 7500 MHz divided into 14 bands of 528 MHz
- Only first Band Group is mandatory
- All-band receiver is challenging
  - Range of frequencies to be generated spans several gigahertz
  - Switch time between different bands within band group should be less than 9.5ns

* C. Mishra, A. Valedes-Garcia, F. Bahmani, Anuj Batra, E. Sánchez-Sinencio, J. Silva-Martinez,"**Frequency Planning and Synthesizer Architectures for Multiband OFDM UWB Radios**" *IEEE Transactions on Microwave Theory and Techniques*, Vol. 53, No. 12, December 2005

# AMSC UWB*




- Direct Conversion Receiver
- Full implementation from LNA to ADC
- Includes on-chip rejection of interference in the 5.2GHz U-NII band (WLAN)
- On-Chip Synthesizer generates the 11 required carriers

* A. Valedes-Garcia, C. Mishra, F. Bahmani, J. Silva-Martinez, E. Sánchez-Sinencio, "**An 11-Band 3-10 GHz Receiver in SiGe BiCMOS for Multiband OFDM UWB Communications**" *IEEE Journal of Solid-State Circuits*, Vol. 42, No. 2, April 2007

# Highlight of Experimental Results

- First 3-10GHz MB-OFDM UWB receiver.
- Features first 3-10GHz 11 band fast switching frequency synthesizer.
- First UWB receiver beyond 5GHz demonstrated in package

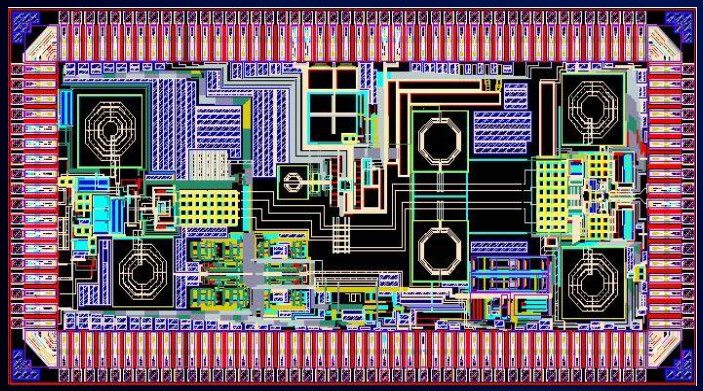
| | |
|---|---|
| Maximum conversion gain | 78-67 dB |
| Noise figure across bands | 5-10 dB |
| IIP3 for band group 1 (worst case) | -9 dBm |
| Baseband group delay variation | <0.6 nS |
| Active area | 5.6 $mm^2$ including pads |
| Current consumption | 114 mA |
| Supply voltage | 2.5 V |
| Package | QFN |
| Technology | IBM 6HP 0.25um SiGe |

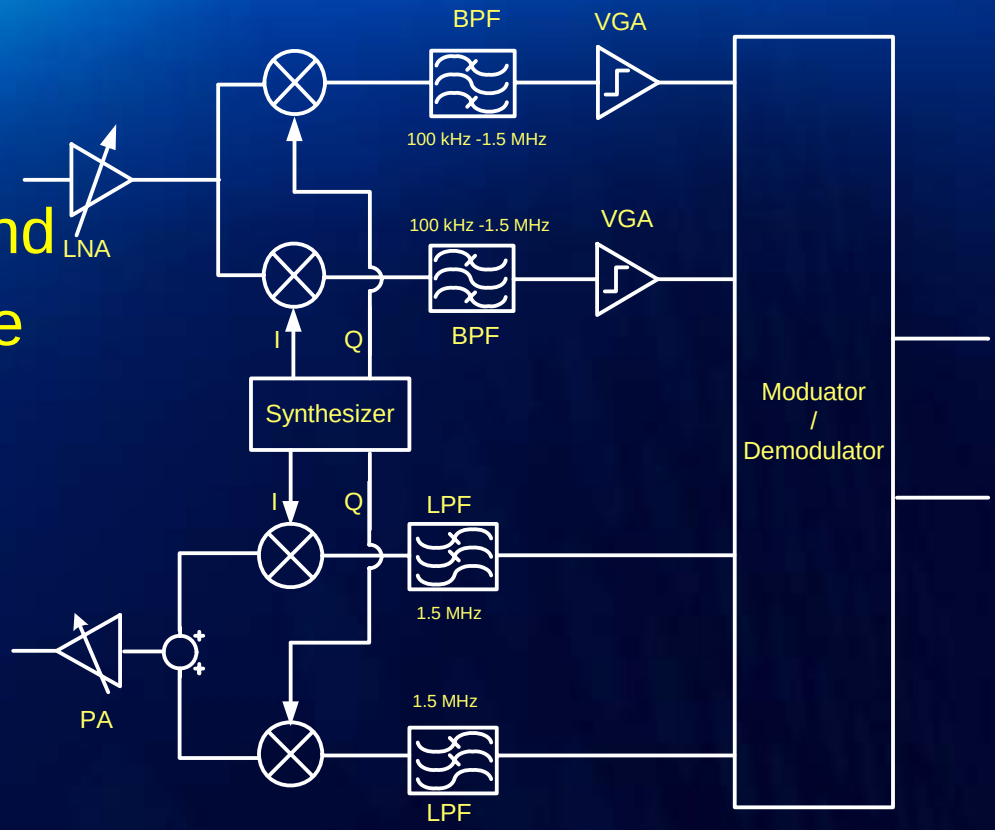
# ZigBee Applications



# AMSC ZigBee Transceiver*

- Very low-power standard
- Direct Conversion / ISM Band
- OQPSK Signal w/ sine-wave shaping
- Analog Mo/Dem
  - Coherent
  - Non-Coherent






- Integer-N Synthesizer
- Switching-Type PA
  - Constant-envelope signal

* ***Under fabrication***; Team Members: Faisal Hussien, Hesam A. Aslanzadah, Sang Wook Park, Didem Turker, Rangakrishnan Srinivasan, Felix Fernandez, Mohamed Mobarak, Gang Bu, Edgar Sánchez-Sinencio

# Recent Trends

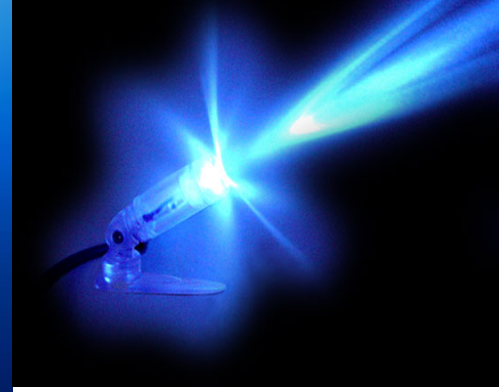
in **Wireless Technologies**

# Recent Trends

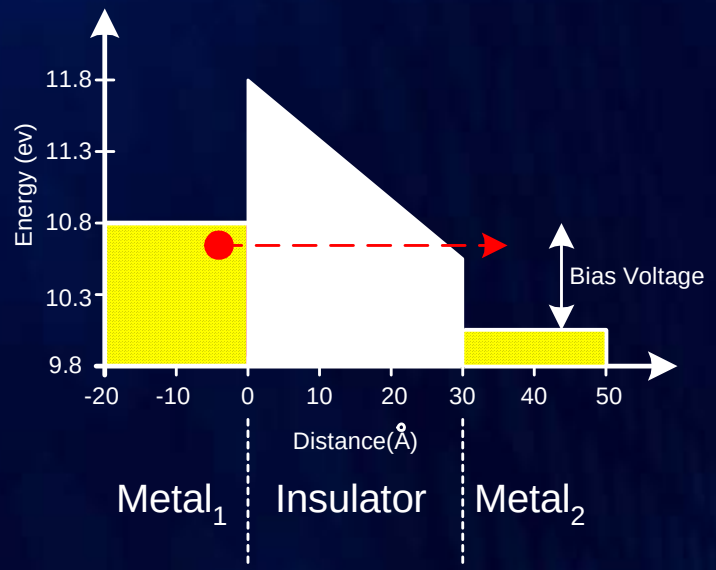
- Multi-Standard Transceivers
  - Multifunctional, Multi-band, Concurrent radios
- Adaptive Radios
  - Software-Defined Radio
- Baseband blocks
  - Reconfigurable
  - Programmable
  - Power-Adjustable
- High Integration
  - Antenna integration at millimeter-wave frequencies
- Wearable devices
  - Ultra low-power reliable RF/Analog
- MIMO
  - IEEE 802.11n, WiMax, …

# Emerging Technologies

- Concept: Quantum tunneling
- Low-Cost MIM technology
- *Phiar Inc.* models $f_T$ of 1.8 THz for MIIMIM transistors to be produced in 2008
- "Amorphous and compatible with a wide range of substrate materials"
  - Single chip CMOS 60-GHz transceiver possible w/ digital CMOS and integrated antenna + front-end in MIM



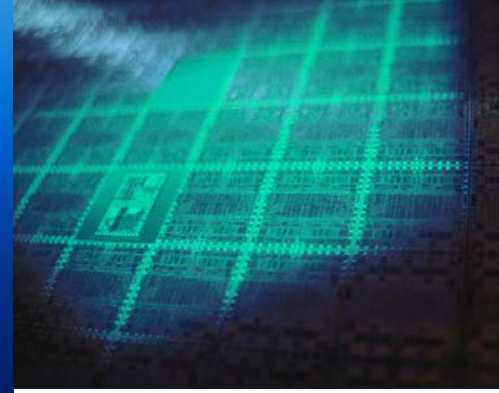
Phiar CORPORATION



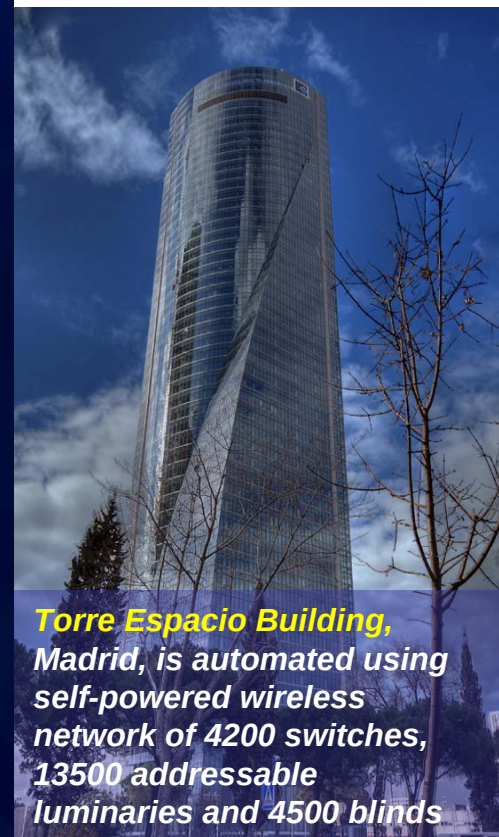

**Electron Tunneling used in a Diode**
***(Source: Phiar.com)***

# Emerging Technologies

- Concept: Green Wireless
- No Battery, No wire
- Building/Home/Industrial Automation
- Radio Module
  - Energy Scavenging: 50uW
  - Range: 300m (free field) / 30m(Building)
  - 868MHz (license free) / 315MHz (less crowded)
  - Data rate: 125kbps
- How?
  - Avoid over-crowded ISM band (2.4GHz)
  - ASK / 1% duty cycle
  - Multiple short telegrams (1ms) w/ checksum



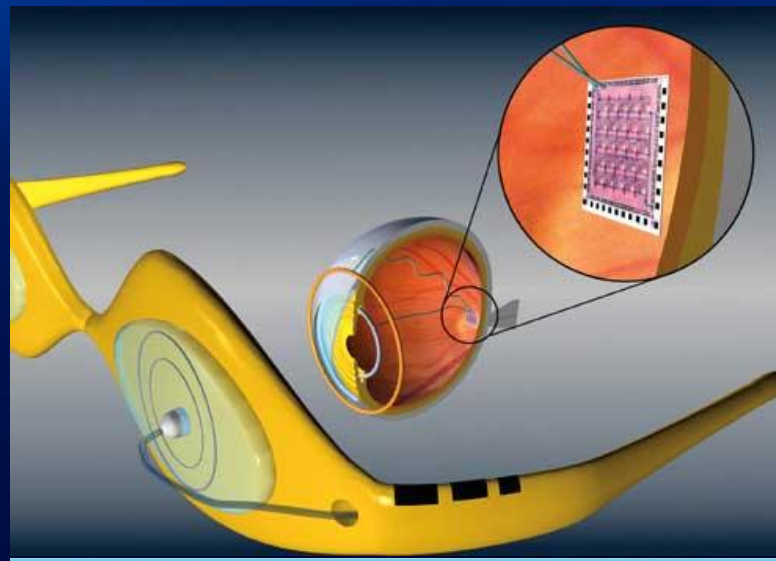
Green. Smart. Wireless.
enocean®

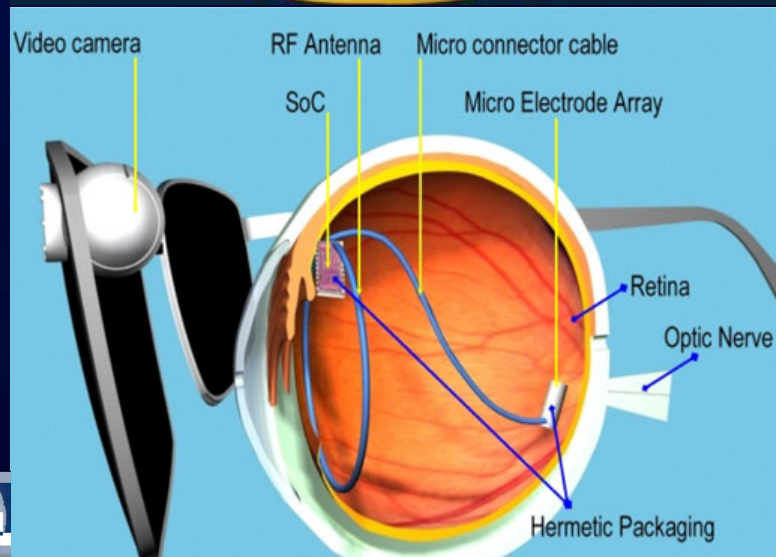


***Torre Espacio Building,*** ***Madrid, is automated using self-powered wireless network of 4200 switches, 13500 addressable luminaries and 4500 blinds***

# Emerging Technologies

- Concept: *Artificial Vision*
- Using
  - Video camera
  - Image processor + transmitter
  - Self-powered wireless receiver
    - Energy Scavenging
    - Receiving Processed Video Data
    - Ultra-low power
    - MICS unlicensed frequency (400 MHz)
- Second Sight
  - (Argus II) 16 Electrode Device
- Intelligent Medical Implants AG
  - 50 Electrode Device






Pictures Courtesy of ***Second Sight*** and ***Intelligent Medical Implants***

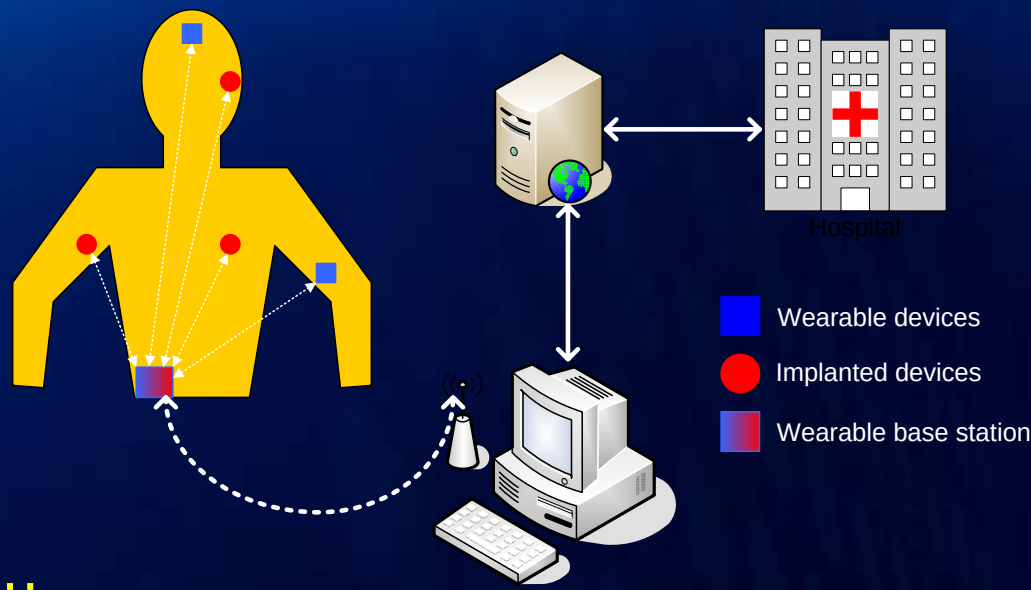
# Emerging Technologies

- Wireless HD (High Definition)
- Three contenders:
  - UWB (MBOA)
  - IEEE 802.11n
  - 60 GHz  license-free waveband

| | Available Spectrum [GHz] | Channel BW [MHz] | $P_{max}$ [dBm] | Data rate [Mbps] Typ./Max. |
|---|---|---|---|---|
| UWB | 1.5 (1 BG) | 520 | -4 | 200/480 |
| IEEE 802.11n | 0.67 | 40 | 22 | 74/248 |
| 60 GHz | 7 | 2500 | 39 | 4000/25000 |

# Medical Implant Communications Service*

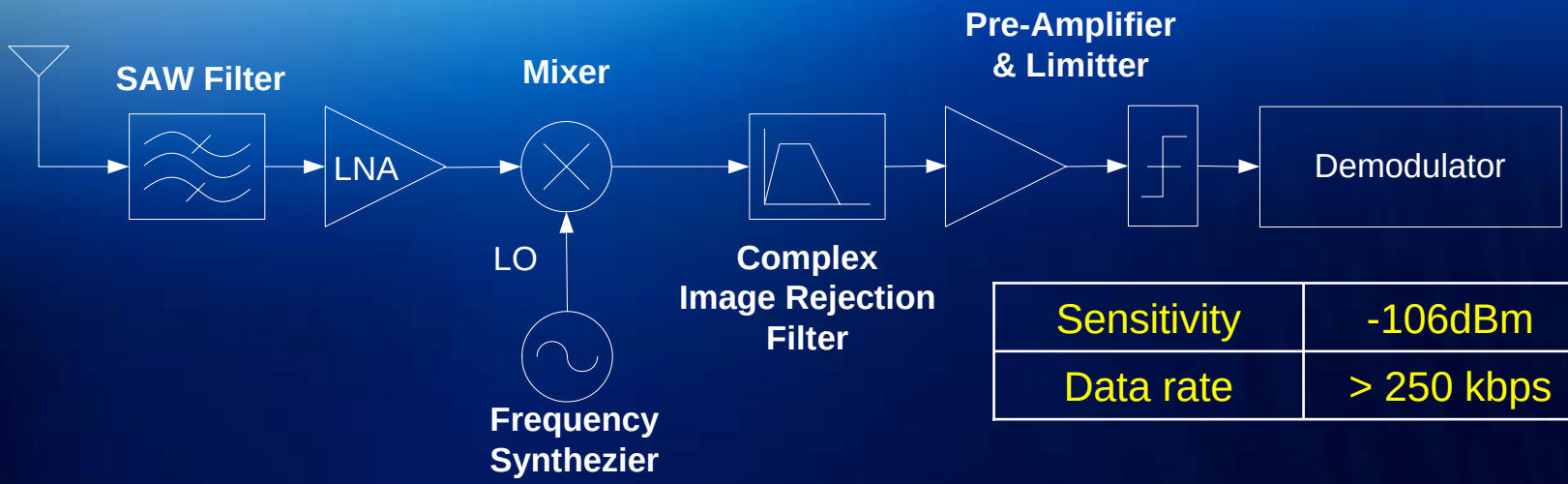
- Concept: Wearable Communication device
- $40B Market by 2011
- Implantable Medical Devices (IMD)
  - Heart diseases
  - Neurological disorders, …
- 402-405MHz band



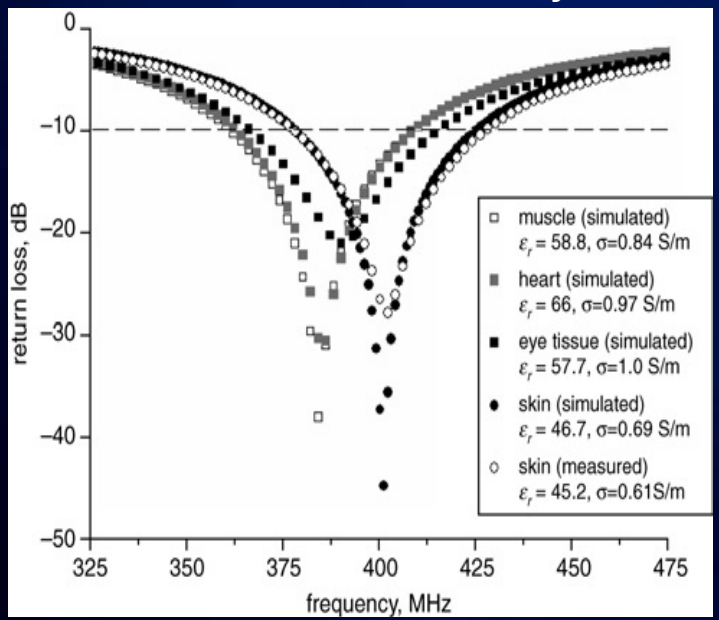

Possible scenario where patient conditions can be addressed remotely in real time using both implanted and wearable devices

* *Under Tape-out;* **Team: Félix O. Fernández-Rodríguez, Mohamed S. Mobarak, Mohammed M. Abdul-Latif, Jincheng Li, Kwisung Yoo, Edgar Sánchez-Sinencio**

# Architecture:



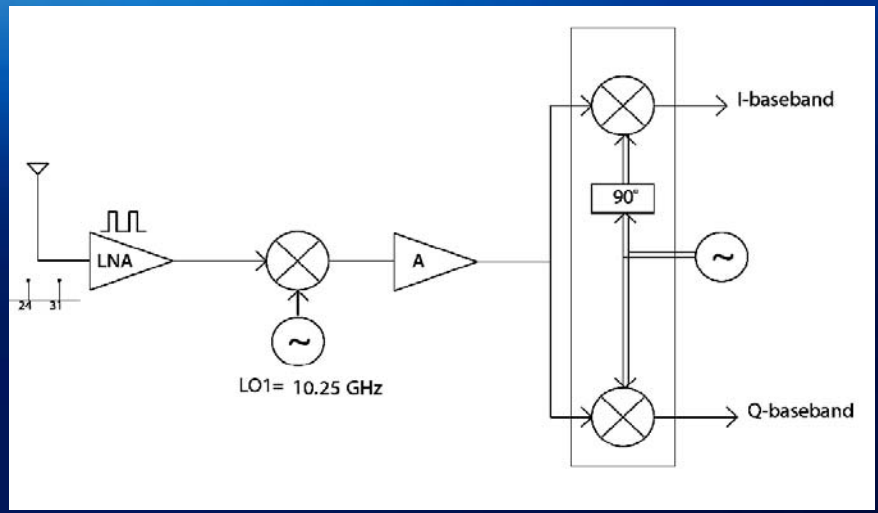

| | |
|---|---|
| Sensitivity | -106dBm |
| Data rate | > 250 kbps |




Measured and simulated return loss for stacked implantable planar inverted-F antenna implanted into different biological tissue

- Why 402-405 MHz?
  - Good radio propagation characteristic within human body (less return loss)
  - Suitable to meet MICS requirements (e.g. size, power, antenna performance and relaxed receiver design)

# AMSC MM-wave Receiver*




- Project Goals
  - Design/Implementation of a dual band receiver for the ISM(24GHz) and LDMS(31GHz) bands
  - The receiver should comply with IEEE802.16 standard
- MM-wave Dual Band receiver
  - The RF front-end is reused
  - Sub-harmonic mixing to reduce LO frequency
  - Band selection is preformed at IF

** Under Design; Team:* **Mohamed El-Nozahi, Ahmed Amer, Kamran Entesari and Edgar Sanchez-Sinencio**

# Conclusion

- Wireless applications in all areas of our lives
  - Medical, Environmental, Communication, House Automation, Security, …
- Different architectures for varying applications

Cartoons courtesy of ***The Economist (by Bell Mellor)***

# Thank You

Q&A

# Feed-forward Interference Suppression for Broadband Systems

Xin Wang

CERC, Dept. of ECE
Univ. of Texas at Austin
Austin, TX 78712
Tel : 949-735-5988
Fax : 512-471-8967
e-mail: xinw@cerc.utexas.edu

Ranjit Gharpurey

CERC, Dept. of ECE
Univ. of Texas at Austin
Austin, TX 78712
Tel : 512-232-7940
Fax : 512-471-8967
e-mail: ranjitg@cerc.utexas.edu

**Abstract - A RF front end IC design with integrated interference mitigation techniques that does not employ off-chip filters is desirable for reasons of cost as well as flexibility. Two different feed-forward cancellation approaches, one using phase aligned injection locked oscillator (ILO) embedded in a phase locked loop (PLL) and the other using a translational auxiliary path whose local oscillator (LO) signal is retrieved from the incoming interference signal, are presented in this paper and trade-offs between the two are discussed. Silicon results are presented for the ILO approach while prototype data are shown for the second method. Both structures can be applied to address the strong narrow band interference challenge in broadband systems.**

## I. Introduction

Interference suppression has attracted significant research interest recently as a result of the ever increasing usage of available spectrum due to the growing number of wireless communication standards.

For broadband systems such as WiMedia, also known as multi-band orthogonal frequency division multiplex (MB-OFDM) version of UWB, the wide unlicensed spectrum between 3.1GHz and 10.6GHz is used and therefore interference problem becomes especially challenging. Since no narrow band RF filter can be applied, even though it is possible for the system to hop to another 528MHz wide sub-band to avoid overlapping with a strong interferer, linearity is critical especially for the down-conversion mixer input stage. The high linearity requirement can lead to excessive power dissipation without the use of interference mitigation techniques.

A tunable band-stop response is proposed in [1] but is limited to frequency modulation (FM) systems. A fixed notch filter for suppressing WLAN interferers in a UWB front-end is reported in [2]. However this approach effectively makes certain UWB bands unusable. Spatial multiplexing [3][4] requires multiple receivers and antennas. Feed-forward cancellation with auxiliary down- and up-conversion paths [5][6][7] can be employed for narrowband desired signal and requires careful gain and phase alignment. An auxiliary path with feedback is used in [8] and is effective in rejecting specific interferers with known frequencies.

It is highly desirable if a single receiver without multiple antennas/inputs can reject strong modulated interferers at RF front end while passing broadband desired signals with dynamic tuning capability to the interferer frequency. Two approaches that address this problem are presented below. To our knowledge these architectures are new approaches to the problem of active interference detection and suppression.

## II. Proposed Solutions

### *A. Translational Auxiliary Path with Interference Frequency Estimation*

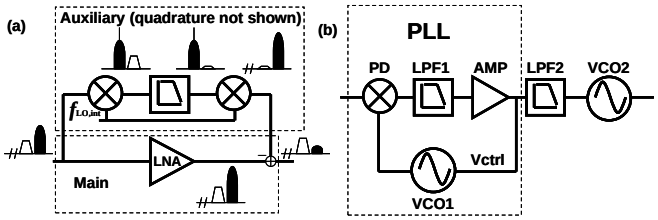



Fig. 1: (a) Feed-forward cancellation and (b) PLL-based estimation of interferer frequency

A feed-forward approach with interference frequency estimation has been proposed as shown in Fig. 1 [9]. The architecture of the receiver with the auxiliary path is shown in Fig. 1a. The main path consists of an LNA. The auxiliary path consists of I-Q down-conversion mixers, LPF's, and I-Q up-conversion mixers. The energy incident on the receiver is assumed to consist of a desired signal and an interferer, which may be modulated. The main path employs direct down-conversion, where the LO of the main path translates the desired signal to baseband. The LO used in the auxiliary path is assumed to be coincident with the center frequency of the external interferer.

The interferer is translated to baseband in the auxiliary path and is selected by the LPF. If the signal is at a different carrier frequency compared to the interferer, the LPF will reject the signal. The output of the auxiliary path is combined with the main path. By ensuring that the gain of the auxiliary path has the same magnitude and opposite phase compared to that of the LNA, the interferer can be canceled at the output of the LNA. The use of an LPF in the auxiliary path instead of an HPF allows for isolation of the interferer without impacting the signal as in [8]. However unlike [8], feedforward is employed, which makes the structure unconditionally stable.

A PLL is used to estimate the center frequency of the interferer (Fig. 1b). A mixer is employed as the phase detector (PD) since the reference input to the PLL is at a high frequency. The interferer and the desired signal, which is

assumed to be significantly smaller, are applied to the reference input of the PLL, which tracks the phase and frequency of the much larger interferer. If the interferer is frequency- or phase-modulated, the control line of the VCO will vary with time. The output of VCO1 will also be modulated and cannot be directly applied to the down- and up-converters in the auxiliary path. The control line of VCO1 (Vctrl) is averaged using a narrow-band low-pass filter (LPF2), whose output is used to tune a second identical, matched VCO (VCO2). In effect, the combination of the PLL and LPF2 operates as a frequency counter whose output is used to set the frequency of VCO2. In fact, if a sufficiently fast counter is available, it can be equally well used here for frequency detection. The output of VCO2, i.e. $f_{LO,int}$, is utilized in the auxiliary path (Fig. 1a). The technique has also been demonstrated with AM and DSBSC interferers as discussed in section III.

### *B. Phase Aligned Injection Locked Oscillator Approach*

A dynamically adaptable notch filter is realized with an injection-locked oscillator embedded within a phase locked loop (PLL) to provide self-tracking capability [10]. The auxiliary path can self-adapt to the interferer frequency with automatic phase alignment. The output of the auxiliary path can be linearly combined with the main signal path to achieve cancellation of the interferer with minimal impact on the desired signals, as shown in Fig. 2. A two-stage LNA is used in the front end, where the output from the first stage (LNA1) is fed into the injection port of the ILO whose negative resistance strength and center frequency ($f_c$) are both programmable. The frequency $f_c$ can be programmed using coarse and fine settings, with digitally controlled capacitors and analog varactors, respectively. The output of the ILO and LNA1 are also fed into a custom phase detector (PD). The transfer function of the PD is designed to have zero output voltage at zero degree input phase offset. As in a classical PLL, the PD output drives an analog charge pump (CP) and second-order loop filter (LF) and generates an analog tuning voltage that is applied to the oscillator's varactor tuning port.

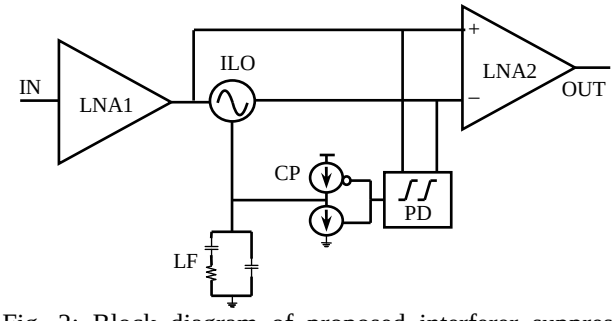



Fig. 2: Block diagram of proposed interferer suppression technique

The second stage of the LNA is a differential buffer LNA2. When the phases of the interferers from LNA1 and oscillator are aligned and have equal amplitudes, they are accurately canceled at the output of the second stage LNA2, since the amplifier is differential. Amplitude control is necessary at the input of LNA2 to ensure that the amplitudes at the differential inputs of LNA2 are equal along with the signal phases, which are automatically aligned by the PLL action.

The oscillator is initially operated in a low-Q non-oscillating mode, by employing a sufficiently low bias-current, which ensures that the losses in the tank are greater than the energy supplied by the negative resistance presented by the active devices. In this mode the oscillator is essentially a tuned buffer utilizing a shunt LC tank. The LC buffer amplifies the interferer with a zero phase shift when its center frequency equals that of the interferer, at which point the tank presents pure resistive impedance. This observation is used to tune the center frequency of the tank to be equal to that of the interferer (to the first order), by embedding the buffer within a PLL which compares the phase of the RF interferer applied to the input of the LC buffer to that appearing at its output, and minimizes this difference by tuning the center frequency of the tank.

Once this tuning is achieved, the bias of the oscillator circuit block is increased incrementally, until it becomes unstable and enters oscillation. The strength of negative resistance shunting the LC tank in this mode can be tuned by adjusting the bias current, which also controls the amplitude of the interferer. Since the PLL sets the tank center frequency to be equal or very close to the interferer frequency, the oscillator injection locks to the interferer, even if the negative resistance strength of the oscillator is programmed to a high value, without the risk of self oscillation at the oscillator's natural frequency. If the oscillator enters self-oscillation mode where it is not injection-locked to the interferer, there will be at least two separate strong tones, the interferer and the self oscillation output, and the phase detector will be effectively disabled with an average output of zero.

## III. Response to Different Modulation Types

It is useful to examine the response of both systems to interference with different types of modulation.

### *A. Translational Auxiliary Path Case*

Interference frequency estimation is the key for this approach. Different modulations on the interferer result in different behaviors of the PLL.

If an un-modulated CW interferer is applied to the PLL, VCO1 will lock to the tone and provide a constant control voltage, as long as the tone is within the capture range of the loop. If the interferer is frequency-modulated (FM), the PLL will track the FM as long as the modulation is within the capture range of the PLL. The average of the resultant VCO control voltage, if applied to an identical VCO, can be used to clock the auxiliary path. The impact of the amplitude-modulated (AM) interference envelope modulation is on the gain of the phase detector, which will vary in response to the instantaneous AM strength. If the PLL is locked to the center frequency of the AM interferer, the control line will still be at a DC level.

The most challenging modulation schemes are those where the carrier is suppressed, e.g. BPSK, QPSK and QAM. It is instructive to first examine the case of a double-side band suppressed carrier (DSB-SC) interferer of the form $\cos(\omega_m t)\cos(\omega_{int} t)$ with periodic zero crossings, which will cause the oscillator control voltage, Vctrl, to experience an

instantaneous step, and then eventually settle to a value identical to that before the phase step was applied, since the frequency is unchanged. In the steady state, the control voltage of the PLL can be divided into the tracking and locked regions periodically, as shown in Fig. 3. The settled part of the control signal in Fig. 3 represents the information regarding the center frequency of the DSB-SC interferer. The transient behavior of the control voltage will be mostly averaged out by LPF2 shown in Fig. 1, resulting in a much smoother LO signal from VCO2 to feed the auxiliary path.

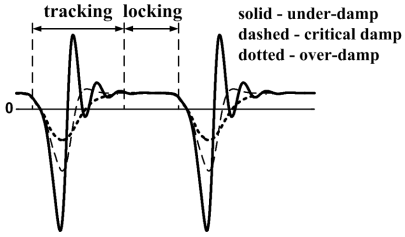


Fig. 3: PLL control signal for the DSB-SC interferer

More detailed discussion on PLL behaviors for different modulation types can be found in [9] and thus are not repeated here.

### *B. Phase Aligned ILO Case*

The ILO approach is able to address phase and frequency modulated interferers besides single tone as long as the modulation bandwidth is within that of the PLL loop filter. This is mainly due to the automatic phase aligning feature of the approach.

For amplitude modulated case, some envelope detection with proper scaling is necessary for the amplitude control of the auxiliary path. The scaling is especially important for the most challenging case of DSB-SC interferer, to ensure that the auxiliary path oscillator enter the non-oscillating mode when the interference amplitude is low such that no self oscillation will happen.

## IV. Prototyping/Silicon Results

### *A. Translational Auxiliary Path Case*

A prototype implementation of the feed-forward interference cancellation with the PLL-based frequency estimate is shown in Fig. 4. The main signal path in the front-end consists of an amplifier and a phase shifter. The auxiliary path consists of a high-frequency VGA, passive I-Q down-converter, low-pass filters with 5MHz corners, passive I-Q up-converter, followed by a high-frequency amplifier AMP2. The baseband section in the auxiliary path consists of filters only. The amplifiers used in the prototype exhibit a low-frequency cut-off of 100kHz, and therefore they could not be used at baseband. The auxiliary path is similar to that employed in [7], except that HPF's were used instead of LPF's in that architecture. AMP3 is a high-frequency amplifier that emulates the input stage of the receiver mixers. PLL consists of a passive mixer as a phase detector. The loop filter consists of an OP-AMP based first-order low-pass filter (LPF1). The output of the OP-AMP drives VCO1 in the PLL path. The corner frequency of the LPF2 was 16kHz and its output was applied to an identical VCO (VCO2) that was trimmed to ensure nearly identical frequency vs. voltage characteristic.

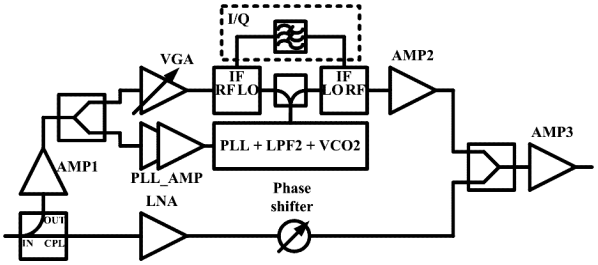


Fig. 4: Block diagram of the prototype system

Four representative measurements depicting cancellation for different types of interferers are shown utilizing VCO2 to provide the LO for the auxiliary path. The desired signal at 884MHz is 30dB smaller than the interferer at 874MHz in these measurements. For CW tone case, the interferer is attenuated by 18.2 dB. The FM interference of 0.4MHz modulation bandwidth obtains an attenuation of 18.5dB. Similarly, a 0.4MHz wide AM interferer is attenuated by about 19dB. A DSB-SC interferer that consists of two phase-locked tones at 873.8MHz and 874.2MHz was also employed. With the auxiliary path applied, an attenuation of 15dB was achieved. Within the band of interest, where the desired signal may be present, the noise in the two cases is almost identical. The noise power increases for frequencies within the passband of the auxiliary path LPF, which corresponds to the interferer band.

To measure the P1dB of the system, a DSB-SC signal consisting of tones at 873.8MHz and 874.2MHz is applied as the interferer. For the main path alone, the 1dB gain compression of the desired signal at 884MHz was improved from -34.7dBm to -25dBm by 9.7dB. The linearity is limited by the final amplifier AMP3. The above improvement in linearity is achieved without significant measurable impact on the noise floor.

### *B. Phase Aligned ILO Case*

The architecture was designed and implemented in UMC's 0.18μm RFCMOS process. The design has a die area of $2mm^2$ and the auxiliary path draws about 10mA current off a 1.8V supply and 2~3mA off a 3.3V supply. Due to the speed and Q limitation, we designed the system around 1.5GHz to prove the concept. The same principle can be applied at higher frequencies, using a faster technology, such as 0.13μm CMOS.

We swept input power level of the interferer for four different levels and recorded suppression achieved with the best digital tuning setting for ILO of each frequency point within the range between 1.35GHz and 1.56GHz. For input power level between -20dBm and -25dBm, most frequency points achieved better than 15dB of interferer suppression. For -30dBm level, most data points lie between 10 and 20dB. For -15dBm level, suppression ranges between 5 and 10dB. At this power level, LNA1 entered compression, which caused degradation in the achievable cancellation.

Compression performance with and without cancellation

was determined in another measurement using an interferer at an offset of 120MHz from the signal. The 1dB compression point with cancellation was observed at an output of -7.9dBm. Without the cancellation active, the interferer at the output increased to -2.1dBm, causing a gain compression of 2dB.

For modulated interferers, we employed a standard GSM pattern supplied with Agilent N5182A vector signal generator as the interferer and observed similar suppression effect of over 20dB, as shown in Fig. 5. In a similar setup, an FM interferer with 100KHz modulation bandwidth also achieved similar level of suppression.

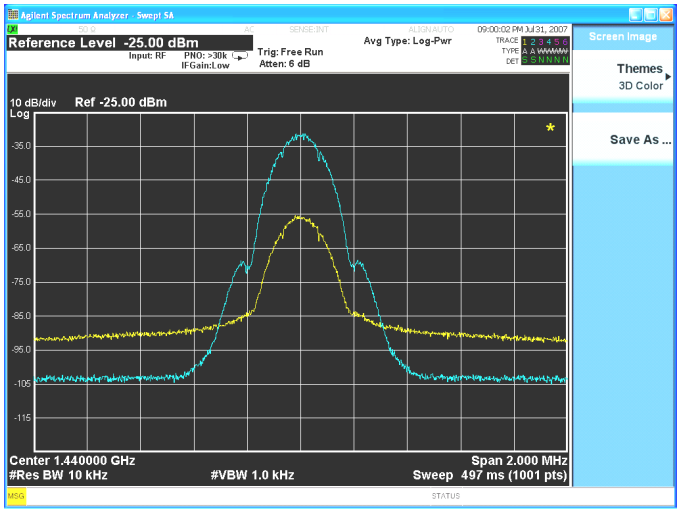



Fig. 5: GSM interferer suppression plot shows better than 20dB cancellation without degrading desired signal (not shown).

A simple broadband match using an off chip balun with and without a 200 Ω external resistor was employed. Similar gain performance was obtained between the two while the NF improved without the resistor. A NF ranging between 3.9 and 4.5 was measured without the auxiliary path in a noise figure meter. This includes an off chip broadband balun that had approximately 1dB insertion loss. the NF get degraded slightly by less than 0.5dB as long as the desired signal is sufficiently far from the oscillation tone, which for this specific design is beyond 200MHz.

## V. Summary and Conclusions

Both techniques have been demonstrated to efficiently suppress interference for broadband desired signal systems, a major advantage over [5-7] without assuming a known interferer LO signal as did in [8].

While fundamentally implemented under different principles, the two approaches employ similar hardware blocks such as the PLL's and oscillators.

The ILO approach requires fewer additional circuit blocks while the translational path approach potentially offer a more robust solution for more complicated interferer types. For example the ILO approach may need to employ advanced signal scaling for the AM loop (not implemented in our work) to guarantee the cancellation. Mitigation of spurious tones is equally critical for both approaches.

Both approaches would require phase noise of the oscillator to be of the order of that required in the main path down-converter, as the reciprocal mixing product of the interferer and phase noise will appear along with the interferer. Lastly, similar to what was discussed in [7], to handle multiple interference signals separated by a frequency offset beyond the PLL loop bandwidth, parallel structures may become necessary for both approaches.

## References


[1] E. Baghdady, "New developments in FM reception and their application to the realization of a system of power-division multiplexing," *IEE Trans. Commun. Syst.*, pp. 147-161, Sep. 1959

[2] G. Cusmai, M. Brandolini, P. Rossi, F. Svelto, "A 0.18-um CMOS selective receiver front-end for UWB applications," *Solid-State Circuits, IEEE Journal of*, Vol. 41, No. 8, pp. 1764 – 1771, Aug. 2006

[3] J. Paramesh, R. Bishop, K. Soumyanath, D.J. Allstot, "A four-antenna receiver in 90-nm CMOS for beamforming and spatial diversity," *Solid-State Circuits, IEEE Journal of*, Vol. 40, No. 12, pp. 2515 – 2524, Dec. 2005

[4] D. Neumann, M.W. Hoffman, S. Balkir, "Robust front-end design for ultra wideband systems," *Circuits and Systems, ISCAS 2006, Proceedings, 2006 IEEE International Symposium on*, pp. 4, May 2006

[5] R. Gharpurey, and S. Ayazian, "Feedforward interference cancellation in narrow-band receivers," *Design, Applications, Integration and Software, 2006 IEEE Dallas/CAS Workshop on*, pp. 67 – 70, Oct. 2006

[6] H. Darabi, "A blocker filtering technique for wireless receivers", *2007 IEEE International Solid-State Circuits Conference, Proceedings*, pp 84-85, Feb. 2007.

[7] S. Ayazian and R. Gharpurey, "Feedforward Interference cancellation in radio receiver front-ends," *IEEE Transactions on Circuits and Systems II*, Vol. 54, pp. 902-906, Oct. 2007

[8] A. Safarian, A. Shameli, A. Rofougaran, M. Rofougaran, F.D. Flaviis, "Integrated blocker filtering RF front ends," *2007 IEEE Radio Frequency Integrated Circuits Symposium, Proceedings*, pp 13-16, Jun. 2007.

[9] C.H. Sun, X. Wang, S. Ayazian, and R. Gharpurey, "Interference cancellation in receivers with interference frequency estimation," *IEEE Transactions on Circuits and Systems II*, in press.

[10] X. Wang and R. Gharpurey, "Interference cancellation in broadband wireless systems utilizing phase aligned injection-locked oscillators," *IEEE Transactions on Circuits and Systems II*, May 2008, in press.

# A linear transconductor using series-connected CMOS Quad

Venkatesh Acharya*, Dr. Bhaskar Banerjee* and Dr. T.R.Viswanathan†, *IEEE Fellow*
*School of Electrical and Computer Engineering
University of Texas at Dallas, Richardson, Texas 75083
Telephone : (972) 883-6459, Fax : (972) 883-2710
Email : acharya@student.utdallas.edu,bhaskar.banerjee@utdallas.edu
†School of Electrical Engineering
The University of Texas at Austin, Austin Texas 78712
Telephone : (512) 232-3389
Email : tviswanathan@ece.utexas.edu

***Abstract*— The well-known CMOS Quad generates currents that contain both odd and even functions of its differential input voltage [1]. Here we propose to increase the input voltage range of the quad by connecting its two skewed pairs in series. We also propose a modification to the circuit where the even component current generated in the pairs is selectively fed back to itself. This selective even feedback improves the linearity of transfer characteristics of the series-connected quad.**

## I. Introduction

Linear transconductors are essential building blocks for the design of integrated active filters used in high-speed communication and hard drive systems. The symmetric differential pair is the most popular transconductance element. The nonlinearity in its $v-i$ transfer characteristics must be reduced for precision applications. The quadratic output-current of a CMOS Quad is used to perform this linearization [1]. We have shown[1] how a simple circuit-modification can linearize the Quad without introducing additional gain or appreciable delay in the feedback path thereby achieving high-frequency response. Unlike in a differential-pair linearized by a Quad, this circuit does not have square-law common-mode current in the linearized output.

## II. Linearized series connected Quad

A quad consists of two skewed differential pairs. It forms a transconductance element, which is more linear than a symmetrical differential pair. Its input range can be increased by connecting the two skewed pairs in series. The basic structure of the series connected quad is as shown in Fig 1. All the properties of original quad are preserved here. When a differential input voltage $v_{in}$ is applied across this circuit, it is shared equally across the two skewed pairs. Note that the pairs are transposed like in a normal quad. In effect, we can increase the input voltage before shutting off any of the devices in the two pairs.

PMOS input pairs are used in all simulations as in most of the modern CMOS processes we can connect the bulk of the PMOS devices to the source. This avoids the distortion in the circuit due to back gate bias. This limits the maximum frequency at which this circuit can operate.

[1]Authors can be contacted via email for the copy of the paper.

### A. Circuit description

A series connected Quad consists of two skewed differential-pairs ($M_1, M_2$) and ($M_3, M_4$) with a skew-ratio of $(1:n)$ between the small and scaled device as shown in Fig. 1. Let their transconductance parameters be $k$ and $nk$ as shown. Here $k$ is $[(1/2)C_{ox}\mu(W/L)]$ and the symbols $C_{ox}, \mu$ and $(W/L)$ have their usual meaning of gate-oxide-capacitance per unit area, carrier mobility and aspect-ratio respectively. Both pairs are biased with constant tail current $(n+1)I$ which will be shared among the devices in the ratio same as their aspect ratio. When differential voltage $v_{in}$ is applied across the circuit, it is equally shared across the two skewed pairs. The skewed-pairs in the Quad generate currents that contain both odd and even functions of the differential input-voltage $v_{in}/2$. [A current $i = f(v)$ is odd if $f(v) = -f(-v)$ and even when $f(v) = f(-v)$]. By subtracting the drain-currents of $M_4$ and $M_2$ we can isolate the odd component and by adding the currents of $M_1$ and $M_3$, we get a purely even-function. If we assume a simple square-law model for the FET then even current is proportional to $v_{in}^2$.

The even current generated in the series-connected quad can be selectively fed back to the circuit with two cascode devices. Fig. 2 shows the scheme in which the even currents are fed back to the circuit using identical n-channel cascode devices, $M_5$ and $M_6$. The square-law-current with the appropriate polarity needed to linearize the Quad is obtained by summing the drain-currents of the two smaller devices $M_1$ and $M_3$. Cascode devices provide low output admittance in the feedback path. They also provide the essential level shift. Cascode devices also minimize Miller effect and thus maintain the desired higher frequency response. The cascode-transistors feed equal currents $I_B - (i_1 + i_3)/2$ to the nodes Q and R. The balanced drain-currents in the wider devices $M_4$ and $M_2$ provide the linearized output. Fully differential voltage-outputs can be obtained using resistive or active loads at the drains of $M_4$ and $M_2$. The load will be a capacitor when the Quad is

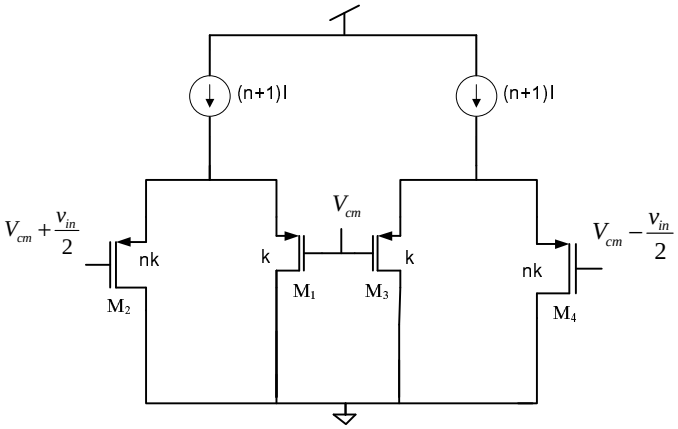



Fig. 1. Series connected quad.

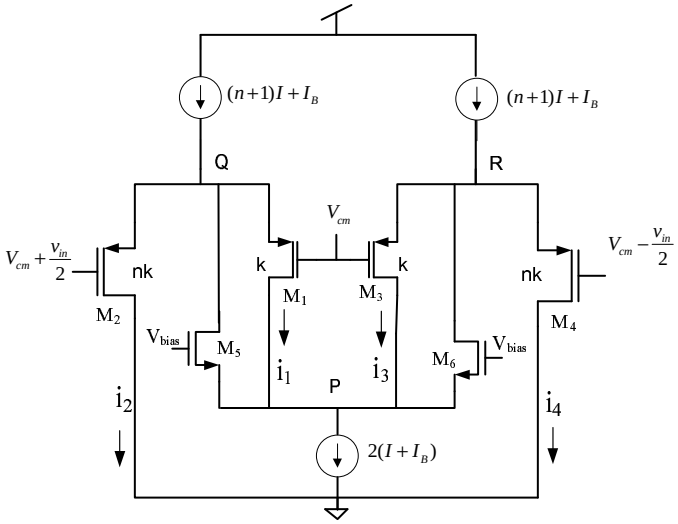



Fig. 2. Series connected Quad with the feedback of even component.

used in $g_m - C$ integrators.

When the signal-currents in $M_1$ and $M_3$ add at the node P, the odd-components cancel and the sum becomes purely even and this divides equally at the sources of $M_5$ and $M_6$. Their drain-currents add directly to the bias-currents of the Quads at the nodes Q and R. Note that there is no inversion or additional-gain in the path. These currents feeding each of the nodes Q and R divide between the small and big devices. In the quiescent state, a fraction $\frac{1}{(n+1)}$ flows in the small devices and the rest, namely the fraction $[n/(n+1)]$, flows in the larger devices. It is easy to see that the feedback for the currents in the smaller devices ($M_1$, $M_3$), is positive but the feedback factor $1/(n+1)$ is less than unity for all positive values of $n$. It is 1/2 for $n = 1$ and it decreases for higher values of $n$. Thus the circuit is stable. This selective-feedback of the even-component amplifies the magnitude of the quadratic-current generated by a factor $[(n+1)/n]$ and superposes it on the tail currents. Thus, it forces the incremental even-component to go to zero in the bigger devices.

Applying KVL to the circuit of Fig. 1, we get

$$\sqrt{\frac{i_1}{k}} - \sqrt{\frac{i_2}{nk}} = \frac{v_{in}}{2}, \quad \text{or}$$
$$\frac{kv_{in}^2}{4} = i_1 + (\frac{i_2}{n}) - 2\sqrt{\frac{i_1 i_2}{n}} \tag{1}$$

$$\sqrt{\frac{i_4}{nk}} - \sqrt{\frac{i_3}{k}} = \frac{v_{in}}{2}, \quad \text{or}$$
$$\frac{kv_{in}^2}{4} = i_3 + (\frac{i_4}{n}) - 2\sqrt{\frac{i_3 i_4}{n}} \tag{2}$$

Let $I$ and $(nI)$ represent the quiescent d-c currents in the small and big transistors respectively. The quiescent current though the cascode devices $M_5$ and $M_6$ is $I_B$. Representing the even and odd signal-currents by $i_e$ and $i_o$ respectively, we can come up with large signal drain currents of the devices $M_{1-4}$ as below :

$$i_1 = I + i_e + i_o, \quad i_2 = nI - i_o,$$
$$i_3 = I + i_e + i_o, \quad i_4 = nI + i_o. \tag{3}$$

Solving equations (1), (2) and (3) we get the large-signal closed-form results for $i_e$ and $i_o$ as

$$i_e = \frac{kv_{in}^2}{4}(\frac{n-1}{n+1}) \tag{4}$$

$$i_o = (\frac{n}{n+1})v_{in}\sqrt{k}\sqrt{I - \frac{kv_{in}^2}{4(n+1)^2}} \tag{5}$$

If we were to subtract $i_2$ from $i_4$ to form a current $i_{out}$ using an additional P-channel current mirror(not shown in Fig. 1), we would get

$$i_{out} = 2(\frac{n}{n+1})v_{in}\sqrt{k}\sqrt{I - \frac{kv_{in}^2}{4(n+1)^2}} \tag{6}$$

Above analysis is not strictly applicable as 0.18 $\mu$m TSMC models do not have good square-law characteristics. The idea here is to get an approximate predictions of the circuit using simple square-law model. Large-signal simulations are essential to investigate the performance of the circuit. Further, it is assumed that the common mode voltage of the input is precisely equal to $V_{cm}$ applied at the gate of devices $M_1$ and $M_3$. Any deviation of the input common mode from $V_{cm}$ effectively reduce the effective window of the circuit.

One advantage of this circuit is that the fully differential output current will not have any square-law common-mode component. This means that common-mode rejection requirement of the following stage will be substantially less. If single ended output current taken out, then common mode rejection ratio required of the subtracter which converts differential output to single ended is also less.

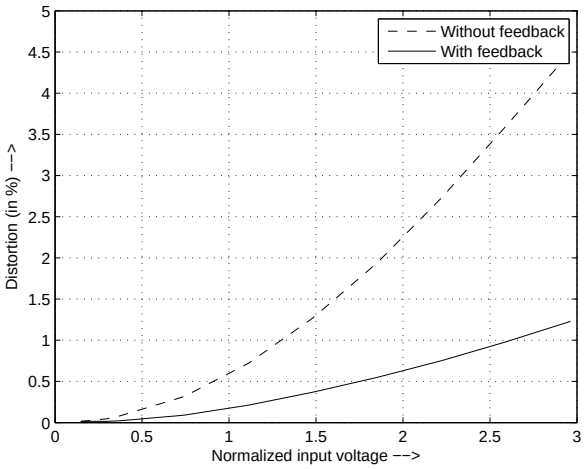



Fig. 3. Effect of selective even feedback in Series Connected Quad (n = 3).

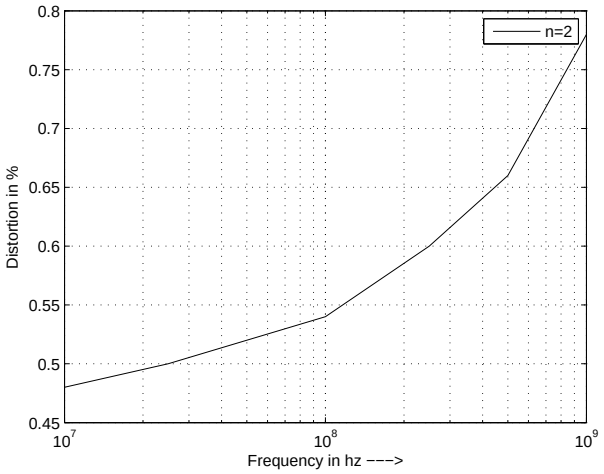



Fig. 4. Total Harmonic distortion versus frequency for $v_{in}/V_{on}$ = 2 and $n = 3$.

### *B. Simulation Results*

The process chosen for the simulations is TSMC $0.18\mu$m and the corresponding BSIM3 (V3.2) models are used. The input voltage $v_{in}$ (normalized with respect to $V_{on}$) is varied over the complete window of the quad. The % error in linearity of the Quad with feedback (obtained by d.c. analysis) for $n = 3$. Figure 3 shows the effect of selective even feedback on distortion. Figure 4 gives the results of large-signal analysis over the frequency range of 10 MHz to 1 GHz. The THD of the Quad remains well below 0.45% up to 10 MHz and increases to 0.78% between 100 MHz and 1GHz.

## III. Linearized series connected quad as a resistor

Making a differential transconductor into a floating resistor is well-known [3], [4]. If we implement a degeneration resistor with a series connected quad with selective even feedback, as shown in Fig 5 we can linearize its transconductance and increase the input voltage range. Simulation results show that for a differential p-p input of 0.8V and frequency 1 kHz, the distortion of less than 1% is achieved. Simulation results obtained from large-signal analysis of the proposed circuit using 0.18$\mu$m TSMC BSIM3 models for the transistors show that for a differential p-p sinusoidal input voltage of 1V, the total harmonic distortion below 0.45% can be achieved at low- frequencies and the distortion remains sub 0.8% up to a frequency of 1GHz.

## IV. Conclusion

The series connected CMOS Quad can be linearized by selective feedback of the even current. Simplified square law characteristics of the FET is used to obtain closed-form solutions. The circuit is stable and gives a low distortion over wide frequency range. This series connected quad with even current fed back can be used as resistor to degenerate simple differential pair. This application is particularly very useful for fabrication in low-voltage digital processes where good quality resistors are always an issue.

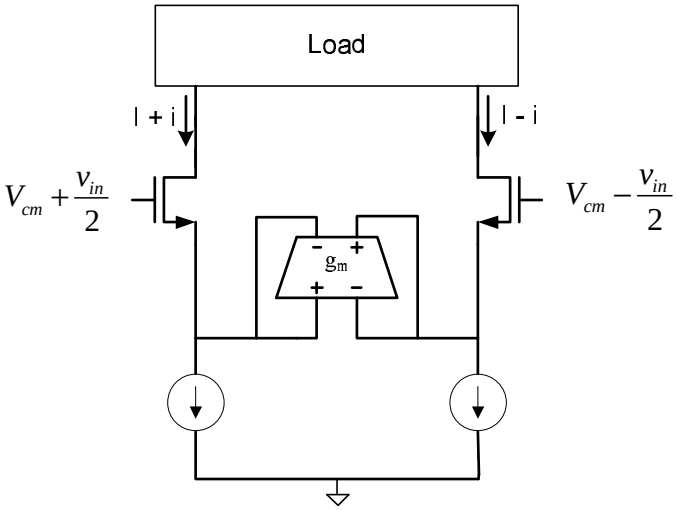



Fig. 5. Degeneration of diff-pair using series connected quad.

## Acknowledgment

The authors gratefully acknowledge the discussions and help of T.L.Viswanathan. We also thank Ashok Nedungadi for useful comments. We also wish to thank Intersil Inc., and Silicon Laboratories Inc. for their financial support.

## References

[1] A. Nedungadi and T.R.Viswanathan, *Design of Linear CMOS Transconductance Elements* IEEE Transactions On Circuits And Systems, Vol. CAS-31, NO. 10, October, 1984. pp 891-894.

[2] V. Acharya and T.R.Viswanathan, *A Linearized CMOS Quad*, unpublished.

[3] S. Tantry, Y. Hiraku, T. Oura, T. Yoneyama and H. Asai, *A Low Voltage Floating Circuit Having Positive and Negative Resistance Values*, Asia-Pacific Conference of Circuits and Systems 2002.

[4] Nagaraj, *New CMOS Floating voltage controlled resistor*, Electronic Letters. Volume 22, issue 12, p. 667-668.

# Series connected CMOS Quad

Venkatesh Acharya
Dr. Bhaskar Banerjee
University of Texas at Dallas

Prof. T R Viswanathan
University of Texas at Austin

# Outline

- Background
- Asymmetrical Pairs , Quad and its use in linearizing diff-pair
- Selective even feedback
- Series Connected Quad (SCQ) to increase the input voltage
- Simulation Results
- Conclusions

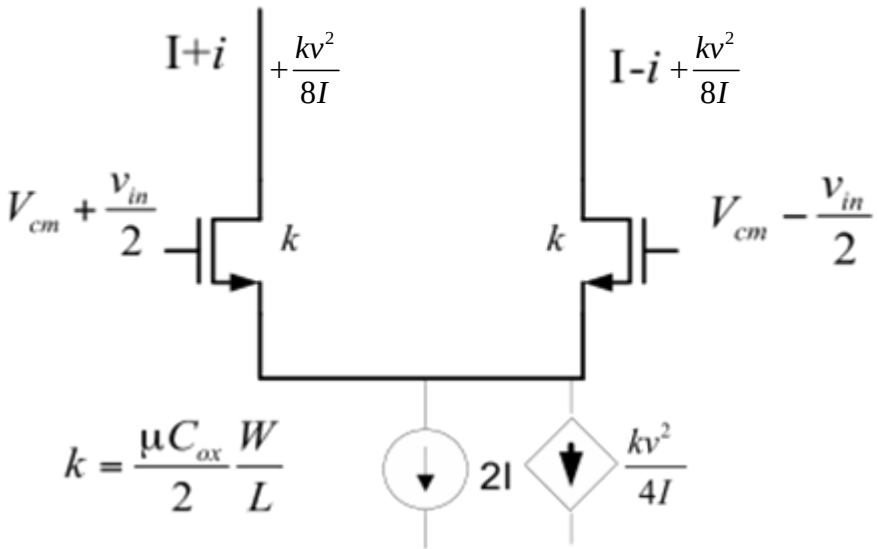
# Differential pair

- A basic building block
- Symmetry causes i = f(v) to be an odd function

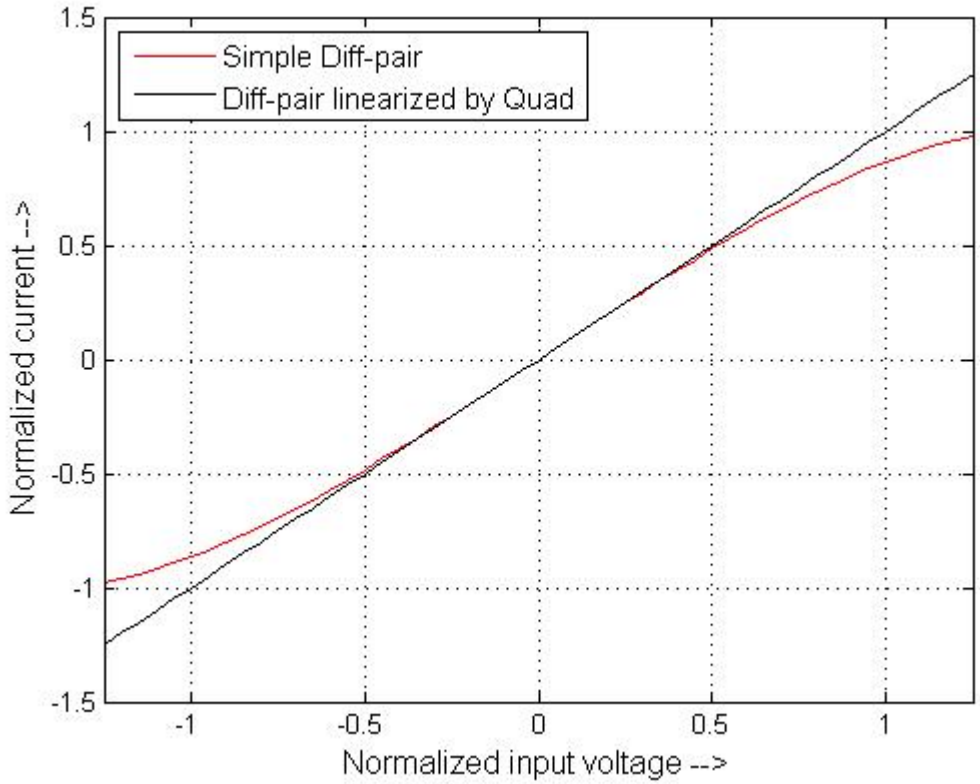
$$i = v\sqrt{kI}\sqrt{1-\frac{kv^2}{4I}}$$

$$i = v\sqrt{kI}\sqrt{1-\frac{kv^2}{4I}+\frac{kv^2}{4I}}$$

$$i = g_m v$$



# DC Characteristics of Diff-pair

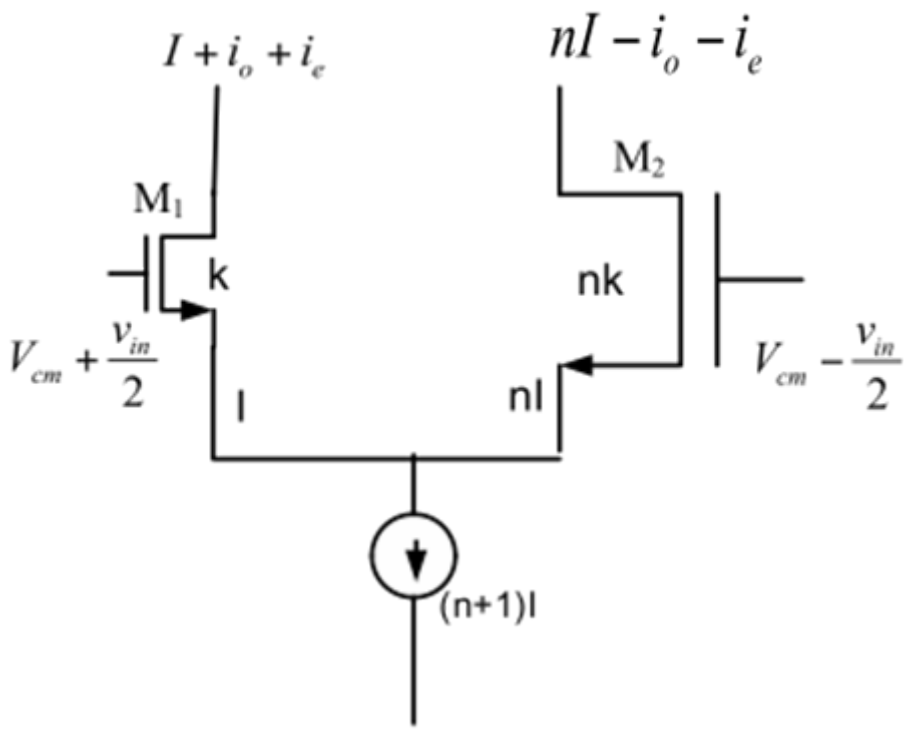


# Asymmetrical Pair

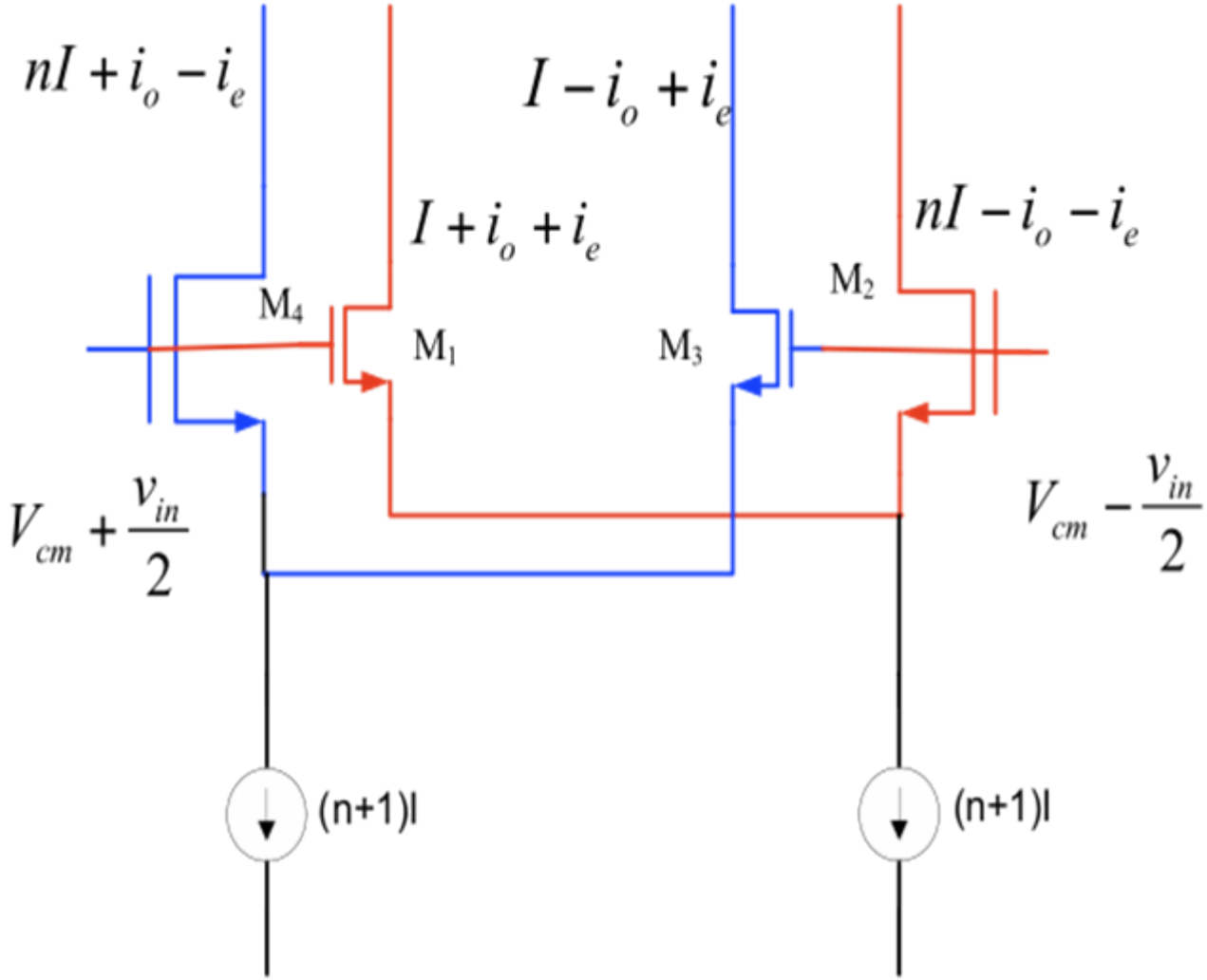
- Asymmetrical pair generates
- $i = f_{odd}(v) + f_{even}(v)$

- A second pair driven by –v gives
- $i' = -f_{odd}(v) + f_{even}(v)$

- Isolate the odd and even components
- $i + i' = 2 f_{even}(v)$
- $i - i' = 2 f_{odd}(v)$



# Two Asymmetrical Pairs- Quad



# Normalized Currents

- Device current i normalized to I, $y_i$=i/I
- Input voltage $v_{in}$ normalized to $V_{on}$= $\sqrt{(I/k)}$, $x=V_{in}/V_{on}$

$$y_1 = 1+\gamma x^2 + 2\alpha x\sqrt{1-\beta x^2}$$

$$y_2 = n-\gamma x^2 - 2\alpha x\sqrt{1-\beta x^2}$$

$$y_3 = 1+\gamma x^2 - 2\alpha x\sqrt{1-\beta x^2}$$

$$y_4 = n-\gamma x^2 + 2\alpha x\sqrt{1-\beta x^2}$$

$$\gamma = \frac{n(n-1)}{(n+1)^2} \qquad \alpha = \frac{n}{n+1} \qquad \beta = \frac{n}{(n+1)^2}$$

# Simple Quad

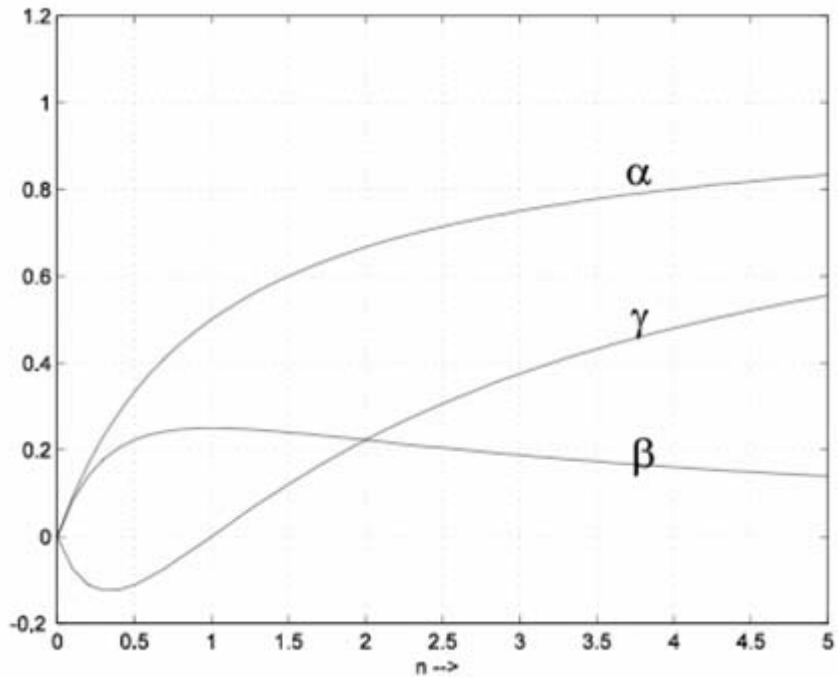
- $\alpha$ measures Tran-conductance
- $\beta$ measures non-linearity term under the root sign. As n becomes large, Quad is more linear.
- $\gamma$ measures the even current generated.

- For n=1,

  $\alpha = 0.5$,

  $\beta = 0.25$

  $\gamma = 0$

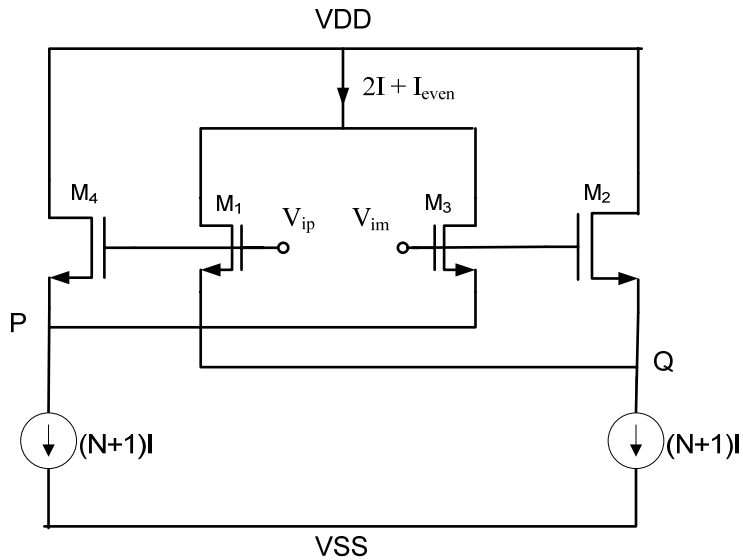


# Outline

- Introduction
- Asymmetrical Pairs , Quad and its use in linearizing diff-pair
- Selective even feedback
- Series Connected Quad (SCQ) to increase the input voltage
- Simulation Results
- Conclusions

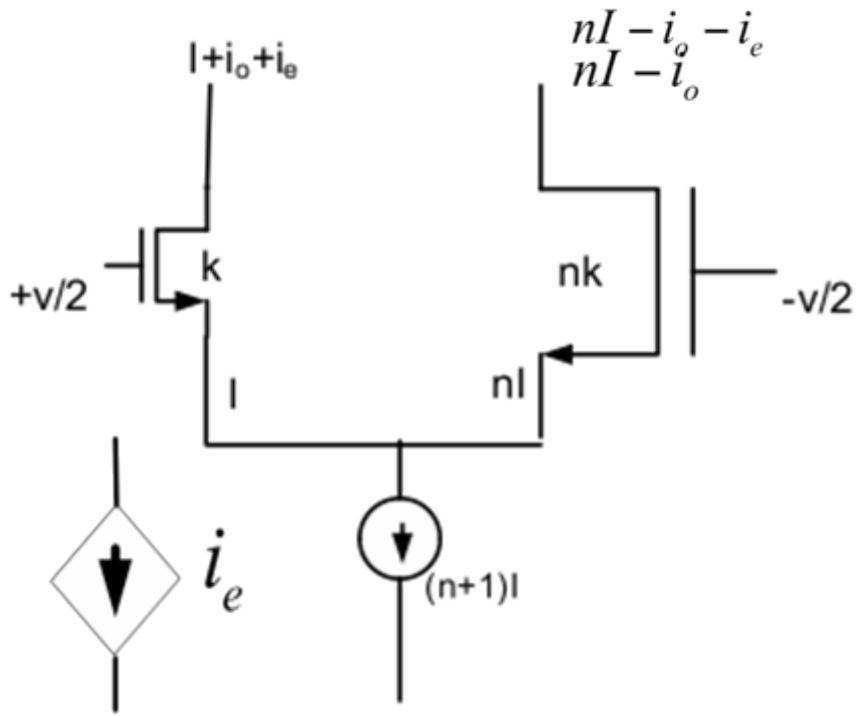
# Few questions to Ponder!

- Quad is more linear than a differential pair
- Diff. Pair can be linearized by a quad
- Can Quad linearize itself? If yes! How well?

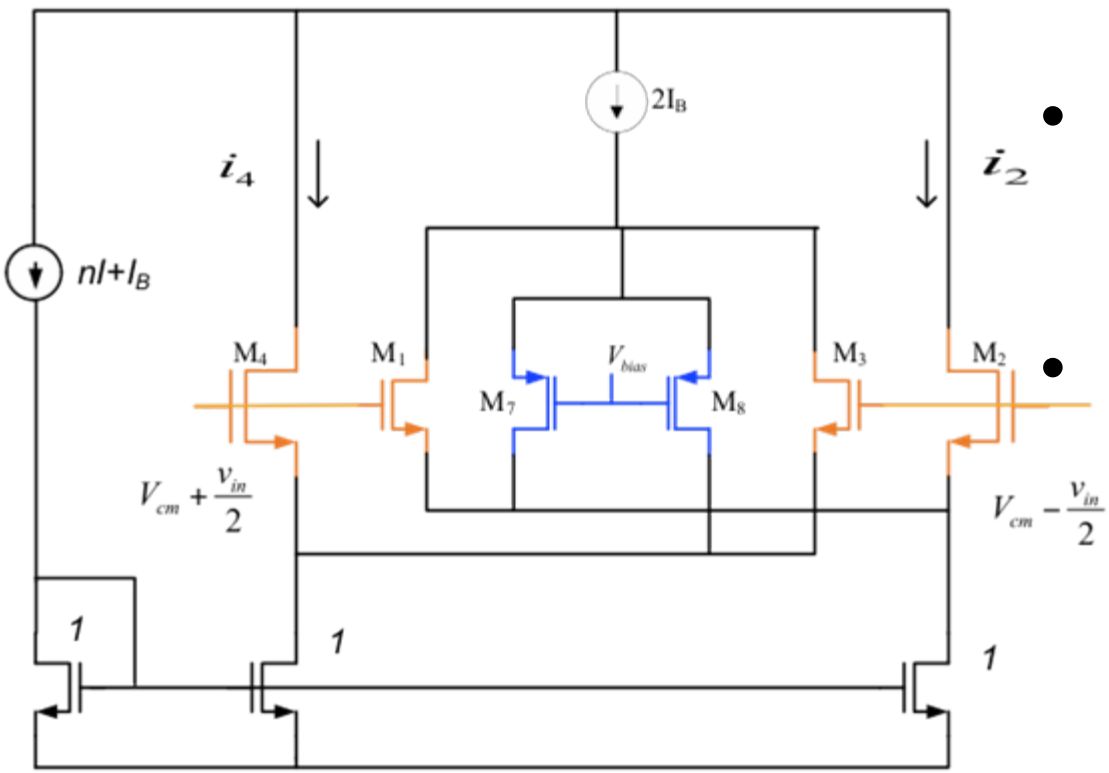


# Selective even feedback

- Add even current to tail current
- Bigger device doesn't have even component
- Very attractive in the differential world



# Modified Quad




- $M_1$ – $M_4$ form quad cell
- $M_7$ - $M_8$ isolate even current and feedback.
- Output currents $i_2$ and $i_4$ don't have even components

# Normalized Currents

- Device current i normalized to I, $y_j = i_j / I$
- Input voltage $v_{in}$ normalized to $V_{on} = \sqrt{(I/k)}$

$$y_1 = 1 + \gamma^* x^2 + 2\alpha x\sqrt{1 - \beta^* x^2}$$

$$y_2 = n - 2\alpha x\sqrt{1 - \beta^* x^2}$$

$$y_3 = 1 + \gamma^* x^2 - 2\alpha x\sqrt{1 - \beta^* x^2}$$

$$y_4 = n + 2\alpha x\sqrt{1 - \beta^* x^2}$$

$$\alpha = \frac{n}{n+1} \qquad \beta^* = \frac{1}{(n+1)^2} \qquad \gamma^* = \frac{(n-1)}{(n+1)}$$

# Effect of selective feedback of $i_{even}$

$$\alpha = \frac{n}{n+1} \qquad \beta = \frac{n}{(n+1)^2} \qquad \gamma = \frac{n(n-1)}{(n+1)^2}$$

$$\alpha = \frac{n}{n+1} \qquad \beta^* = \frac{1}{(n+1)^2} \qquad \gamma^* = \frac{(n-1)}{(n+1)}$$

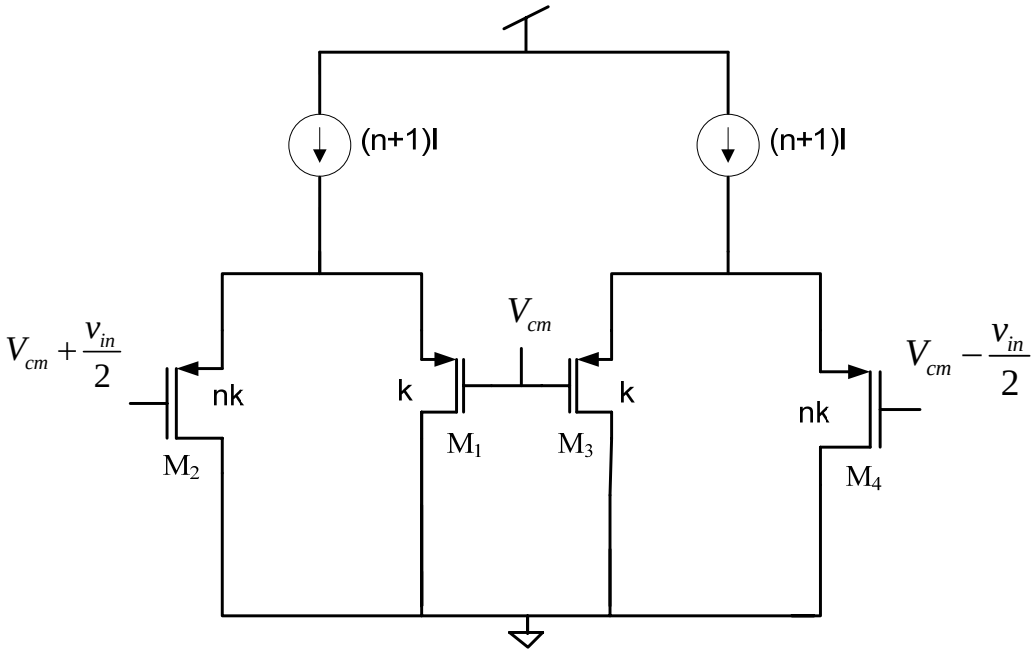
$$\gamma^* = \gamma \frac{n+1}{n} \qquad \beta^* = \frac{\beta}{n}$$

# Outline

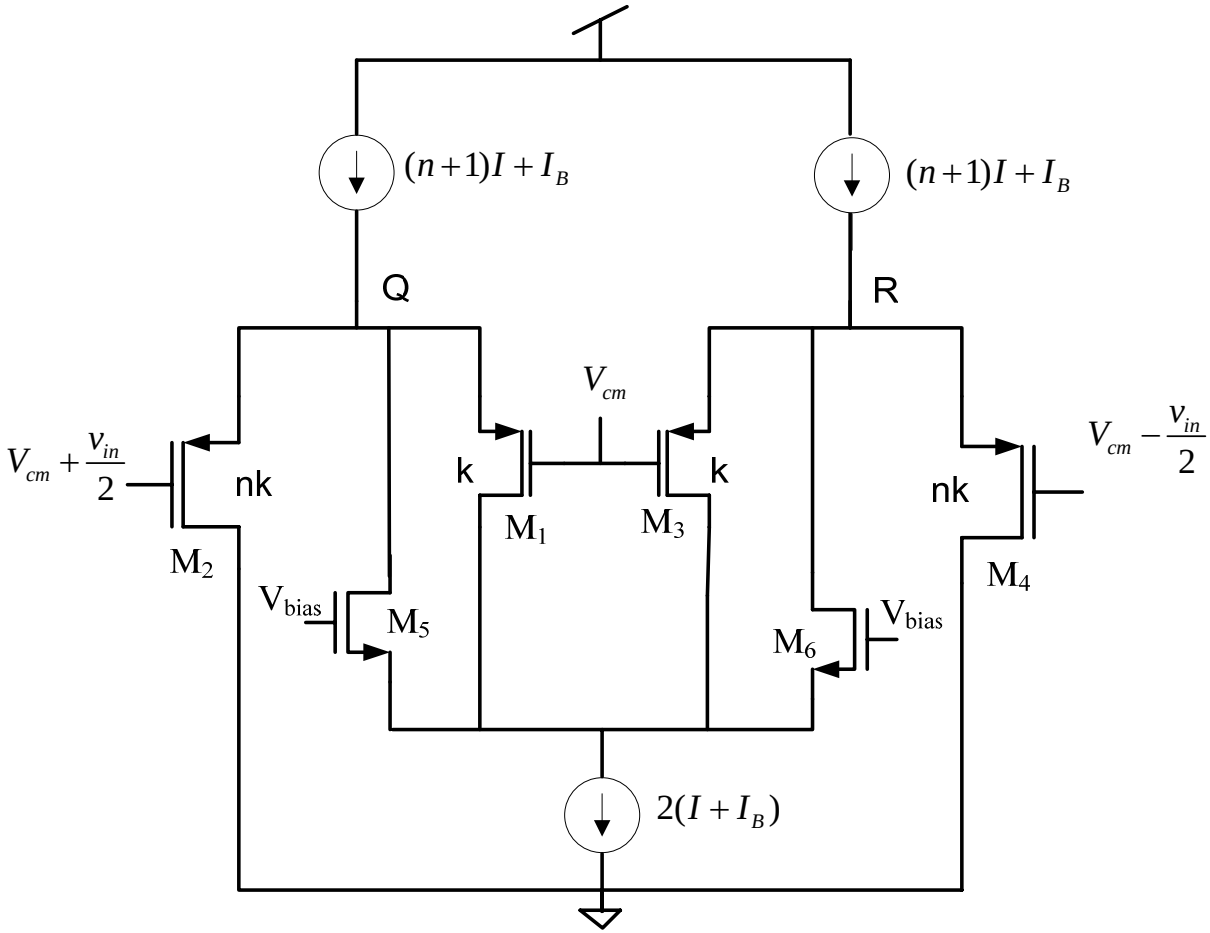
- Introduction
- Asymmetrical Pairs , Quad and its use in linearizing diff-pair
- Selective even feedback
- Series Connected Quad (SCQ) to increase the input voltage
- Simulation Results
- Conclusions

# Series Connected Quad

- Two asymmetrical pairs connected in series
- Input voltage will shared equally between pairs
- Window is doubled
- PMOS input stage to remove back gate bias



# Series connected quad with linearization



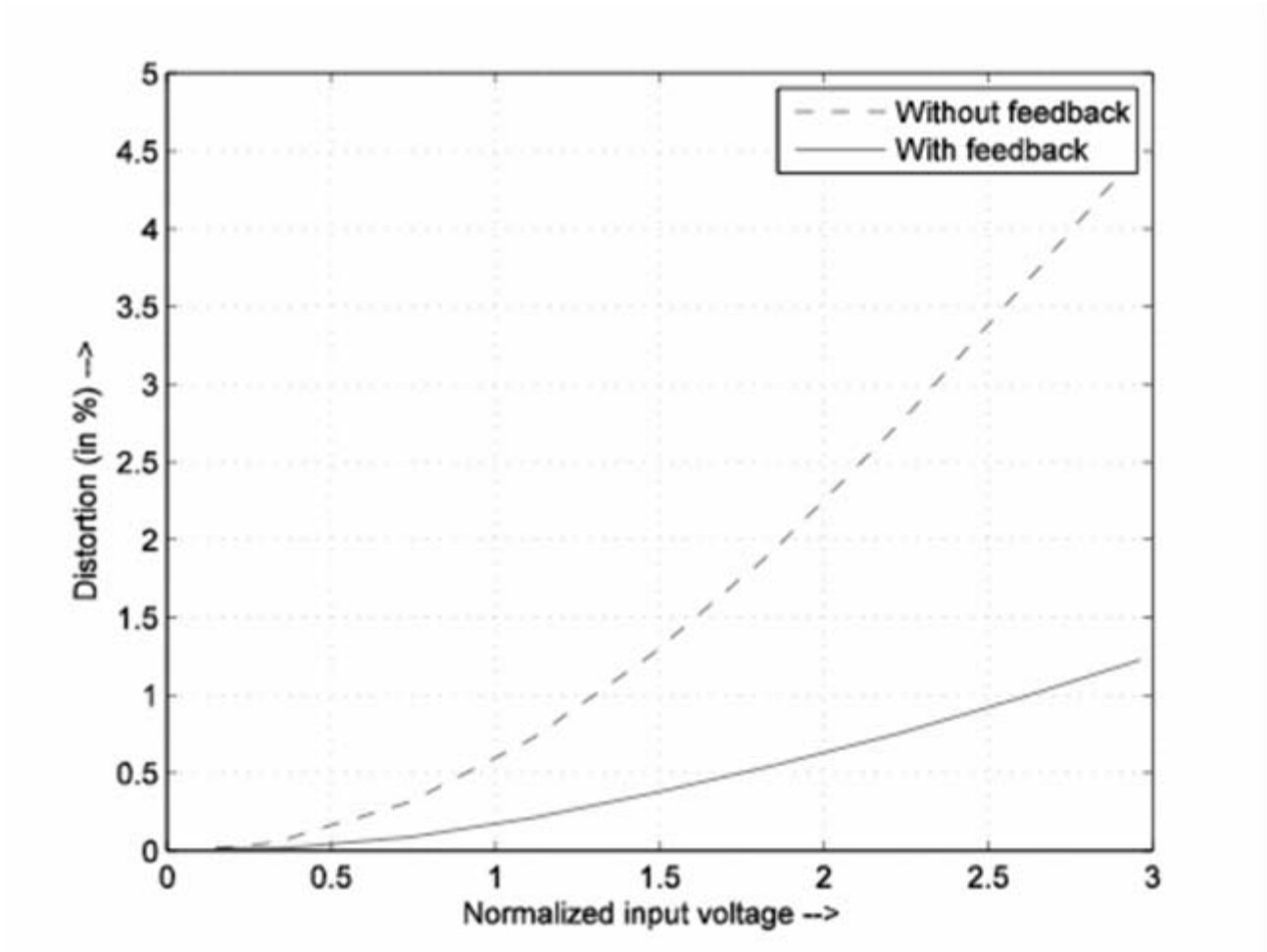
# Outline

- Introduction
- Asymmetrical Pairs , Quad and its use in linearizing diff-pair
- Selective even feedback
- Series Connected Quad (SCQ) to increase the input voltage
- Simulation Results
- Conclusions

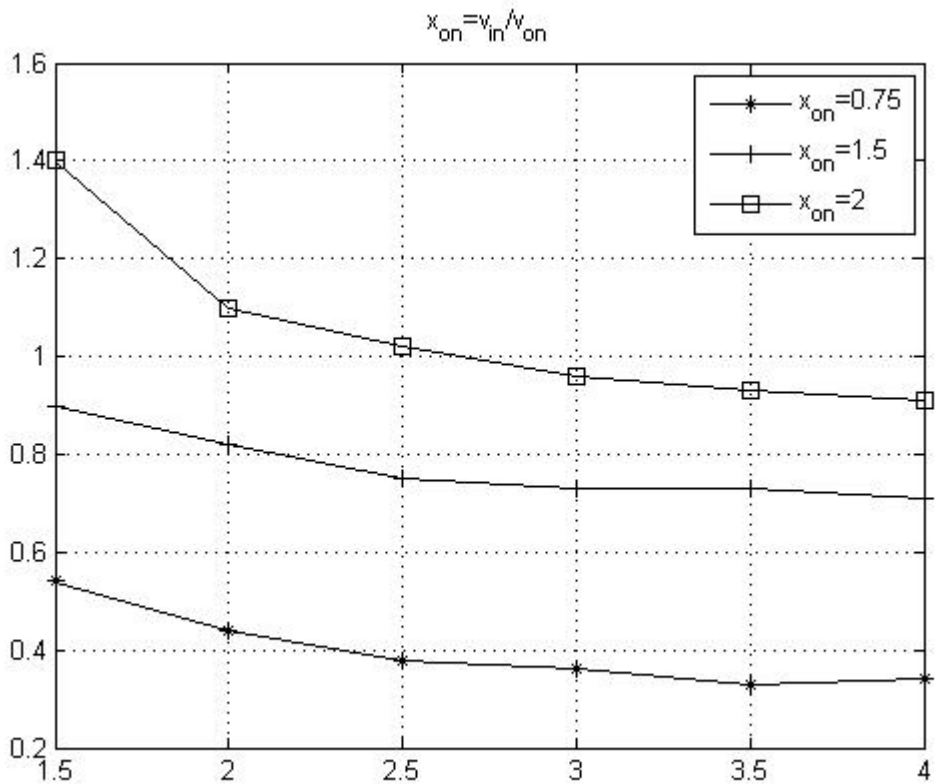
# Simulations

- All the simulations are carried out in 0.18u TSMC 1.8V Process.
- Transient simulations are carried out at 1KHz, unless specified.

# THD vs Normalized input voltage

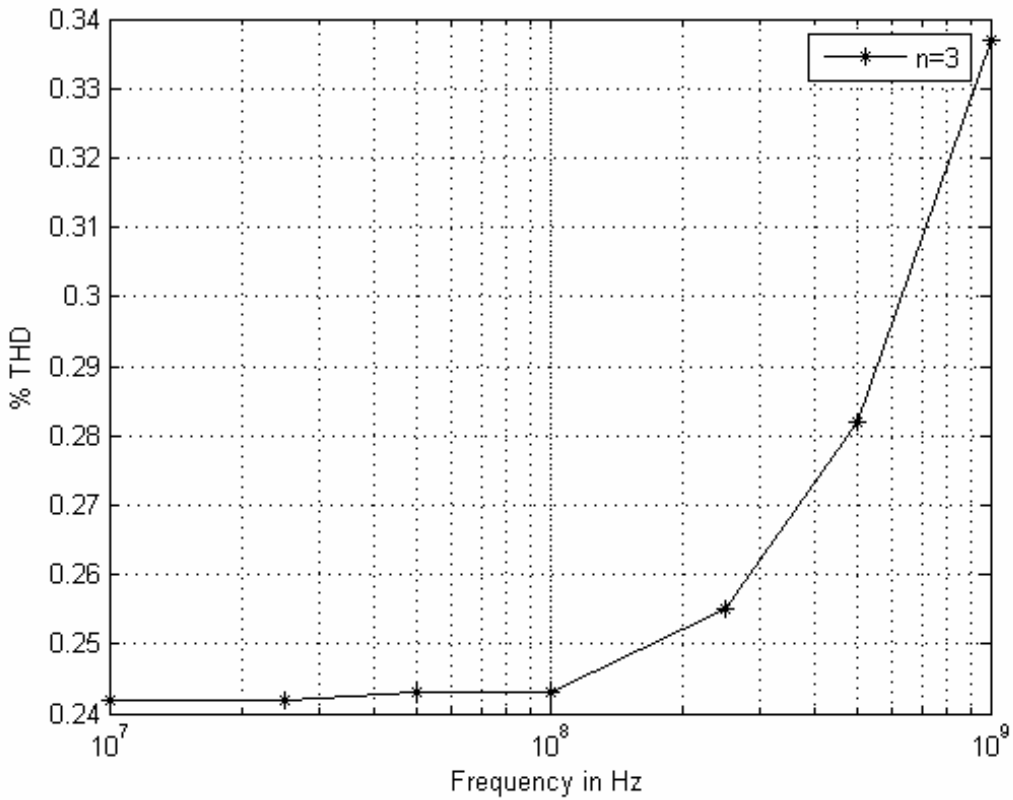


# Distortion as ‘n’ varies




As ‘n’ increases distortion remains constant.

# Distortion Vs Frequency



# Conclusions

- Simple modification in CMOS quad can remove common mode current at the output current. It also reduces the distortion almost one order.
- Series-connected quad increases the maximum input voltage can be applied to quad.
- A numerous applications like band-gap, oscillator, balanced modulator, signal folder can be realized because of even current generated in the CMOS Quad.

Questions??

# Indirect Compensation Technique for Low-Voltage CMOS Op-amps

Vishal Saxena
E.C.E. Dept., University of Texas at Austin
Austin, TX, USA
vsaxena@ece.utexas.edu

R. Jacob Baker
E.C.E. Dept., Boise State University
Boise, ID, USA
JBaker@boisestate.edu

***Abstract*—Two and three-stage indirect-compensated op-amps employing split-length composite devices are presented. By incorporating split-length devices the right-half plane zero which hampers op-amp performance can be eliminated. Chip test results indicate significant enhancements in op-amp speed while reducing power consumption and layout area. Moreover, these techniques can be used to compensate three-stage op-amps operating at low supply voltage ($V_{DD}$).**

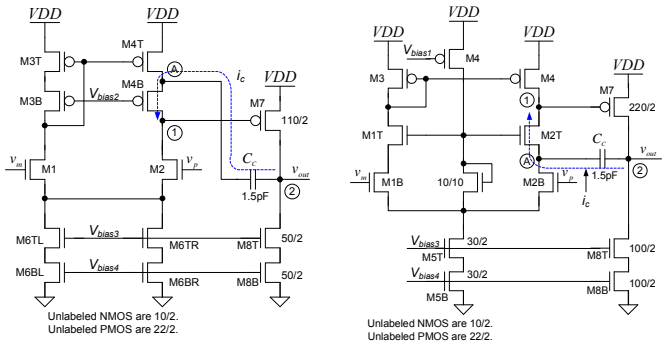
## I. Introduction

Two-stage op-amps have been the amplifier topologies of choice in analog system design due to their simple frequency compensation and relaxed stability criterions. The two-stage op-amps have traditionally been compensated using the Miller (or Direct) compensation technique [1][2]. Miller compensation achieves dominant pole compensation by pole splitting due to capacitance multiplication effect. However, the compensation capacitance ($C_c$) connected between the outputs of the first and second gain stages, leads to a right-half plane (RHP) zero. The RHP zero, located at $z_1=g_{m2}/C_C$ in the s-plane, pulls down the phase margin of the op-amp and requires a larger capacitance to compensate the op-amp. This in turn results in a reduced unity gain frequency of the op-amp given by $f_{un}=g_{m1}/2\pi C_c$ [1].

The RHP zero can be eliminated by blocking the feed-forward compensation current, while allowing the feedback component of the compensation current to attain pole splitting. This can be achieved by several methods including a zero nulling resistor ($R_Z$) or a voltage buffer in series with the compensation capacitor in the feedback path [1][4]. A common-gate stage can also be employed to block the feed-forward component of the compensation current while achieving pole-splitting [3]. Such techniques where the compensation current is indirectly fed-back are categorized as indirect compensation. This paper presents a brief description of indirect feedback compensation and presents the use of split-length devices for op-amp compensation while operating at low-$V_{DD}$.

## II. Indirect Feedback Compensation Of Op-Amps

The class of amplifier compensation in which the compensation current is fed back indirectly from the output to the internal high impedance node is defined as *Indirect Feedback Frequency Compensation* or simply, indirect compensation [1], [5]. Here, the compensation capacitor is connected to an internal low impedance node in the first stage, which allows indirect feedback of the compensation current from the output node to the internal high-impedance node i.e. the output of the first stage. The dominant pole location for the indirect compensated op-amp is same as in Miller compensation. However, instead of a RHP zero we now have a LHP zero located at $z_1=g_{mc}/(C_C+C_A)$, where $g_{mc}$ is the transconductance of the common-gate device and $C_A$ is the capacitance attached to the low-impedance node A. The non-dominant pole location is given by $p_2=-g_{m2}C_C/(C_1C_L)$. Also there exists a third parasitic pole arising due to the loading of the low impedance node-A [4].




(a) Cascoded current mirror load

(b) Cascoded Diff-pair

Figure 1. Indirect compensated two-stage op-amps using cascode common gate device. The compensation capacitor, $C_c$, in each of the op-amps is connected to the the low impedance node A [1][4].

We can discern that when using indirect compensation, the second pole, $p_2$, is pushed further away from the dominant pole, $p_1$, by a factor of approximately $C_C/C_1$. Hence, pole splitting can be achieved with a lower value of the compensation capacitor $C_C$ and/or with a lower value of $g_{m2}$.

This results in a significantly higher unity-gain frequency attainable by the op-amp. Also the LHP zero adds to the phase in the vicinity of the unity gain frequency, $f_{un}$, and improves the phase margin [1][2]. Figure 1 shows two-stage op-amp topologies where indirect compensation is achieved by using the "embedded' common-gate device in the cascode structure [4].

## III. Indirect Compensation using Split-Length Composite Transistors

Indirect-compensated two-stage op-amps can be designed by employing the internal low impedance nodes available in a cascode topology to feedback the compensation current [1]. However, with continual scaling of supply voltage ($V_{DD}$) cascoding may no longer be an option in the sub-100nm CMOS processes [6]. A suitable technique for low $V_{DD}$ design which employs a split-length composite transistor for indirect compensation, proposed in [1]&[5], is analyzed in this section.

Figure 2 illustrates splitting of an NMOS or a PMOS to create a low impedance node-A. For a composite NMOS, the lower device, M1B, operates either in cut-off or triode region but never in saturation. Since a triode device offers a low channel resistance and also that node-A is connected to the source of M1T, the node-A is a low impedance node. Similar argument holds for the PMOS composite device [1].

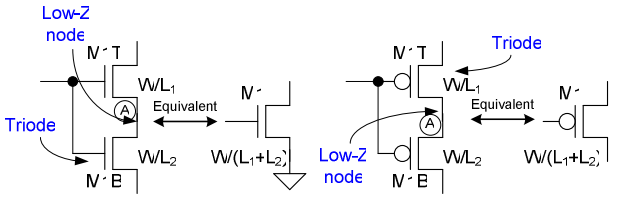



Figure 2. Illustration of the split-length composite NMOS and PMOS devices [1].

### A. *Split length current mirror load (SLCL)*

Figure 3 exhibits a two-stage op-amp with a split-length current mirror load (SLCL) topology. The compensation capacitor is connected to the internal low impedance node-A to achieve indirect compensation.

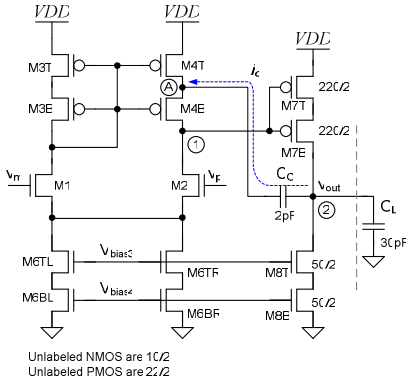



Figure 3. A two-stage op-amp with indirect feedback compensation using split-length load composite devices [1][5].

In order to simplify the small signal analysis of this op-amp topology, few assumptions have been made. The transconductance of each of the split PMOS devices is denoted as $g_{mp}$. The resistance, $R_A$, can be approximated to be equal to the channel resistance of the trioded PMOS, which is close to $1/g_{mp}$. Also, here if the current mirror load is designed with the same $g_m$ as the diff-pair, we have $g_{mp} = \sqrt{2}\,g_{m1}$. The simplified small-signal model for SLCL op-amp is shown in figure 4 [7].

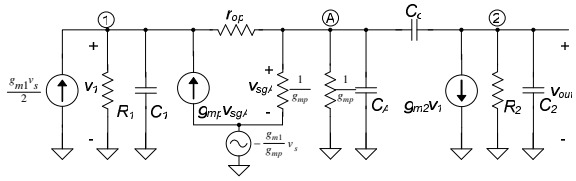



Figure 4. Small signal model for analysis of the two-stage op-amp employing split length load devices [7].

On applying nodal analysis on the small signal model shown in figure 4, we obtain a dc gain of $-g_{m1}R_1 g_{m2}R_2$ and a unity gain frequency equal to

$$f_{un} = \frac{g_{m1}}{2\pi(2C_C)} \tag{1}$$

The dominant pole is given as

$$p_1 \approx -\frac{1}{2g_{m2}R_2R_1C_C} \tag{2}$$

The LHP zero is located at

$$z_1 \approx -\frac{4g_{mp}}{3(C_C+C_A)} = -\frac{4\sqrt{2}g_{m1}}{3(C_C+C_A)} \approx \frac{8\sqrt{2}}{3}\omega_{un} \tag{3}$$

The non-dominant poles are approximated by

$$p_2 \approx -\frac{g_{m2}C_C}{2C_1C_L} \tag{4}$$

$$p_3 \approx -\left[2g_{mp}/C_2 \| C_C + 1/\left(R_1 \| r_{op}\right)C_1\right] \tag{5}$$

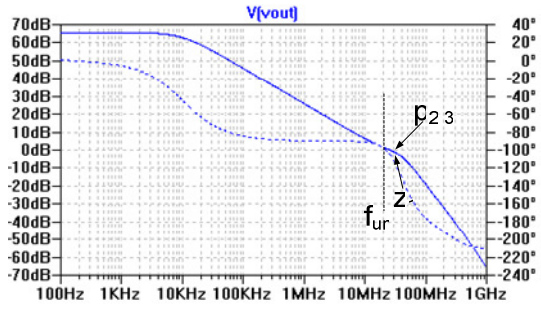



Figure 5. Simulated frequency response of the indirect compensated opamp with split-length current mirror load (SLCL). Here $f_{un}$=20MHz and PM=80°.

SPICE simulated frequency response for this op-amp is shown in figure 5. This op-amp exhibits a unity gain frequency of 20MHz, a phase margin of 75° and a transient settling of 60ns.

### B. *Split length differential pair (SLDP)*

Figure 6 shows the proposed two-stage op-amp topology where a split-length diff-pair (SLDP) is used for indirect compensation. This topology exhibits better power supply rejection ratio (PSRR) since the node used for compensation (node A) is isolated from the supply rails and lesser supply noise is leaked to the output.

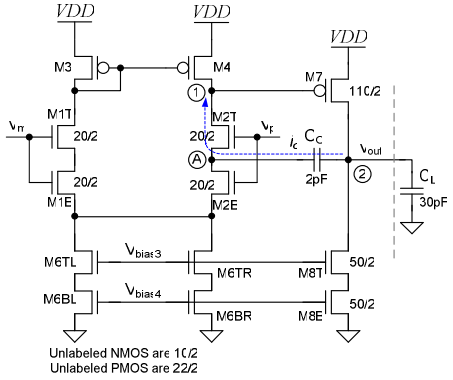



Figure 6. An indirect compensated two-stage op-amp employing split-length diff-pair.

Small signal analysis of this topology again yields the same non-dominant poles and zero locations as in the split-length current mirror load case. However, the unity gain frequency is now estimated by

$$f_{un} = \frac{2g_{m1}}{2\pi C_C} \tag{6}$$

Thus the LHP zero can now be expressed as

$$z_1 \approx -\frac{4g_{mn}}{3(C_C + C_A)} = -\frac{4\sqrt{2}g_{m1}}{3(C_C + C_A)} \approx \frac{2\sqrt{2}}{3}\omega_{un} \tag{7}$$

which implies that the LHP zero is located at a lower frequency than the unity gain frequency. This has the effect of flattening the gain magnitude response which may degrade the phase margin of the op-amp. The SPICE simulated frequency response for this op-amp is shown in figure 7. This op-amp exhibits a unity gain frequency of 35MHz, a phase margin of 62° and a transient settling of 75ns [7].

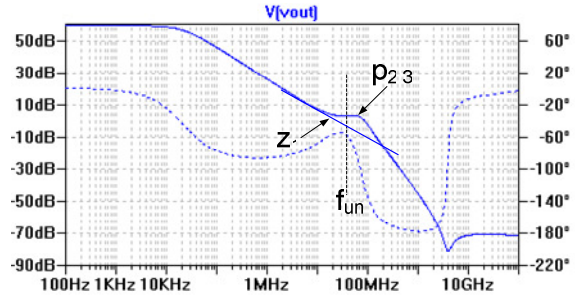



Figure 7. Simulated frequency response of the indirect compensated opamp with split-length diff-pair (SLDP). Here $f_{un}$=35MHz and PM=60°.

In the case of SLCL indirect compensation, we have the flexibility of varying $g_{mp}$ independent of $g_{m1}$ in order to control the location of the LHP zero and hence the phase margin of the op-amp. However, in the case of SLDP we do not have such convenience and it might be hard to obtain desirable phase margins with the SLDP topology. But the SLDP indirect compensation topology is of great utility when designing multi-stage indirect compensated op-amps described in [6].

## IV. INDIRECT COMPENSATION OF THREE STAGE OP-AMPS

The SLCL and SLDP indirect compensation techniques shown in the last section form the basis for low-voltage op-amp compensation. However, one may argue that the op-amp gain is sacrificed by avoiding cascoding. But, since cascoding may no longer be viable due to supply voltage ($V_{DD}$) scaling and relatively fixed threshold voltages ($V_{TH}$). Thus the paradigm of cascoding needs to be traded with cascading of low-voltage stages to design high-gain op-amps in nano-CMOS. Also since the intrinsic gain of the transistors ($g_m r_o$) has been dropping with continued scaling, use of at least three stages is inevitable for op-amp design in nano-CMOS.

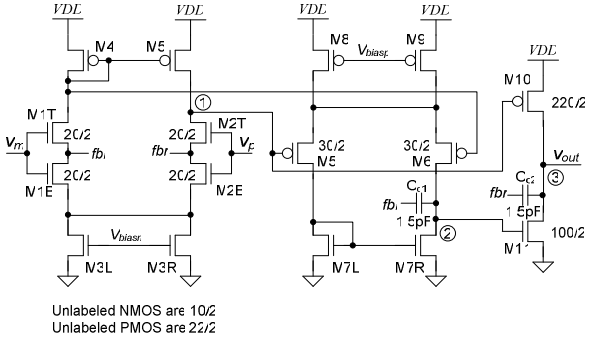



Figure 8. A low-$V_{DD}$ class-AB three-stage op-amp employing reversed nested indirect compensation (RNIC).

Figure 8 presents a three-stage op-amp operating at a supply voltage of 2.5V, designed by cascading three low-$V_{DD}$ gain stages. A PMOS diff-amp is used in the second stage to precisely set the bias level for the third common-source stage and also for providing higher CMRR. The third stage is biased in a class-AB fashion such that the gates of M10 and M11 move together and one of the devices is shut-off while driving the load. Note the way in which the compensation currents are indirectly fed-back to node-1 from nodes 2 and 3.

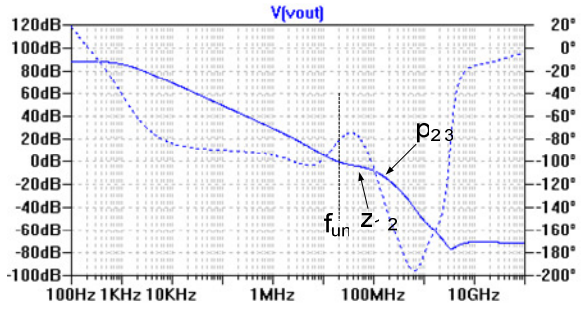



Figure 9. Simulated frequency response of the indirect compensated three-stage opamp (RNIC). Here $f_{un}$=20MHz and PM=76°.

This compensation scheme leads to two LHP zeros besides a dominant pole and two non-dominant poles. The two LHP zeros counter the two non-dominant poles and help improve the phase margin. The low impedance internal nodes fbl and fbr also lead to two parasitic poles at higher frequencies, which are close to the $f_T$ limited poles (or mirror poles) and can be ignored. Detailed analysis for this three-stage topology is provided in [6]. Thus incorporation of indirect-compensation in three-stage op-amps leads to lower power, simple and manufacturable topologies as shown in figure 8.

## V. CHIP TEST RESULTS AND PERFORMANCE COMPARISON

The test chip, designed using AMI's C5N (0.5µm) process, includes Miller compensated op-amps with and without the zero nulling resistor and the SLCL, SLDP & RNIC indirect compensated op-amp topologies (see figure 10).

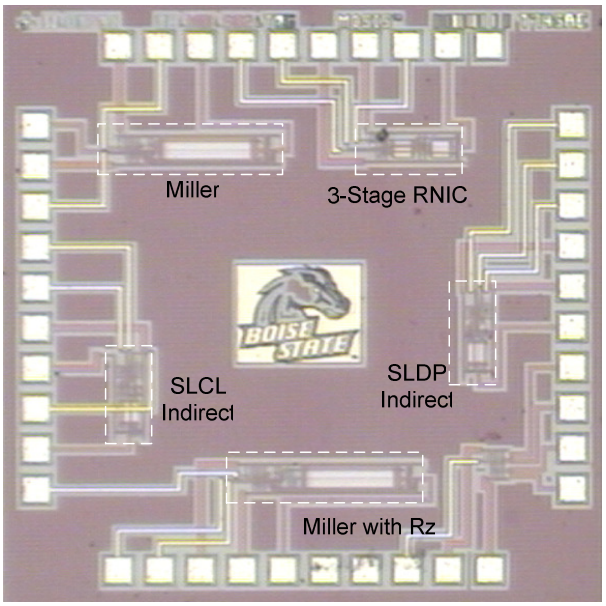



Figure 10. Microphotograph of the test chip showing the fabricated two and three stage op-amps.

A performance comparison of the op-amp topologies fabricated on the test chip is presented in Table 1. The chip test results exhibit that the indirect-compensated two-stage op-amps exhibit nearly ten times improvement in the gain bandwidth ($f_{un}$) and four times faster transient settling when compared to the Miller compensated op-amps. Also the indirect compensation results in 40% reduction in power and 50% reduction in the layout area of the two-stage op-amps.

Further, the proposed three-stage topology leads to around 26 dB higher gain with almost the same unity-gain frequency (as SLCL op-amp) by consuming only 20% more power while operating at 50% of the supply voltage and occupying the same layout area as the corresponding two-stage op-amps.

TABLE I. PERFORMANCE COMPARISON OF THE OPAMPS FOR CL=30PF.

| Op-amp Topology | $A_{DC}$ (dB) | $f_{un}$ (MHz) | $C_C$ (pF) | PM | $t_s$ (ns) | Power (mW) | Layout area ($mm^2$) |
|---|---|---|---|---|---|---|---|
| Miller | 57 | 2.5 | 10 | 74° | 270 | 1.2 | 0.031 |
| Miller with $R_Z$ | 57 | 2.7 | 10 | 85° | 250 | 1.2 | 0.034 |
| SLCL (this work) | 66 | 20 | 2 | 80° | 60 | 0.7 | 0.015 |
| SLDP (this work) | 60 | 35 | 2 | 60° | 75 | 0.7 | 0.015 |
| RNIC (this work) | 89 | 20 | 1.5, 1.5 | 76° | 60 | 1.4 | 0.017 |

## VI. CONCLUSION

Indirect feedback compensation technique applied to two-stage and three-stage op-amps using split-length transistors has been presented. The chip test results demonstrate that the indirect feedback compensation employing split-length devices leads significantly faster, lower power op-amps with smaller layout footprint when compared to the traditional Miller compensation. These indirect compensated topologies are suitable for op-amp design in nano-CMOS processes.


## ACKNOWLEDGMENT

The authors are grateful to the MOSIS educational program for supporting this project.


## REFERENCES


[1] R. J. Baker, *CMOS: Circuit Design, Layout and Simulation, 2nd ed.*, Wiley-IEEE, 2005.

[2] P.R. Gray, P. J. Hurst, S. H. Lewis, R. G. Meyer, "*Analysis and design of Analog Integrated Circuits," 4th ed.*, John Wiley & Sons, 2001.

[3] B. K. Ahuja, "An Improved Frequency Compensation Technique for CMOS Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 18, pp. 629-633, Dec. 1983.

[4] P. J. Hurst, S. H. Lewis, J. P. Keane, "Miller Compensation Using Current Buffers in Fully Differential CMOS Two-Stage Operational Amplifiers," *IEEE Tran. on Circuits and Systems I- Regular Papers*, vol. 51, no. 2, Feb. 2004.

[5] V. Saxena, R. J. Baker, "Indirect Feeback Compensation of CMOS Op-Amps," *proceedings of the IEEE/EDS WMED*, pp. 3-4, April, 2006.

[6] V.Saxena, "Indirect Feedback Compensation Techniques for Multi-Stage Operational Amplifiers," Masters Thesis, Boise State University, Oct 2007.

[7] V.Saxena, R.J. Baker, "Compensation of CMOS Op-amps using Split-Length Transistors," submitted to *IEEE International MWSCAS*, Aug 2008.