



S I L I C O N   L A B S

## Translating Innovation to Commercial Success

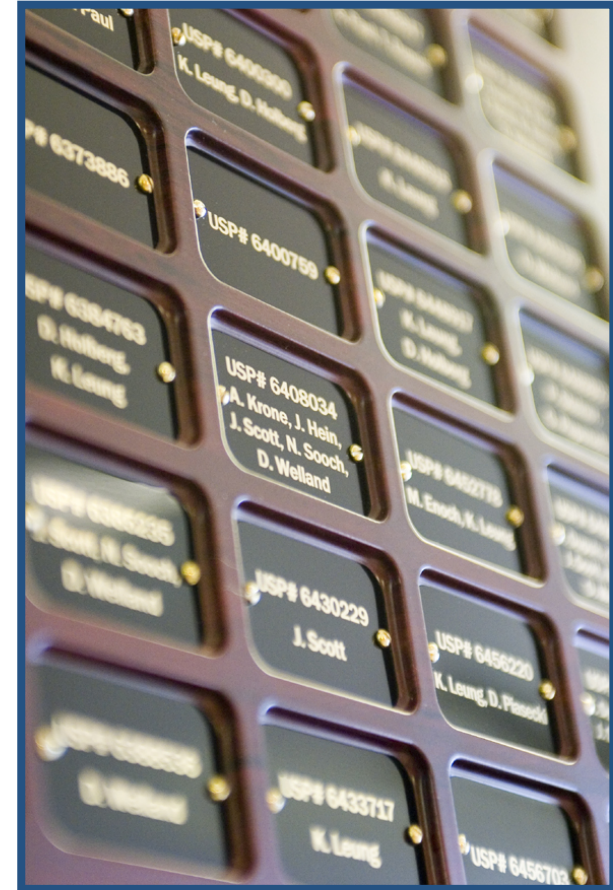
Necip Sayiner, PhD  
President and CEO  
ACISC Conference, 2008

# Agenda – Translating Innovation to Commercial Success

- ◆ Developing differentiation through innovation
- ◆ Leveraging Moore's law
- ◆ Defining commercial success
- ◆ Securing the right talent and encouraging collaboration
- ◆ Focusing on execution and creating a desire to win
- ◆ Keeping in mind the global nature of the market place
- ◆ The end result

# Differentiating through Innovation

- ◆ Must create fundamental, sustainable competitive advantage through innovation
- ◆ Must be aware of customer problems and be able to seek out and implement superior solutions
- ◆ Must have an understanding of the complete system to bring a system-oriented solution to the table
- ◆ Provide a combination of core competencies to break traditional barriers and create first of a kind innovations



# Unique Mixed-Signal Core Competency

- ◆ Combine mixed-signal expertise with digital-centric architectures to replace pure analog approaches
- ◆ Driving higher levels of integration without compromising performance
- ◆ Introducing disruptive products in established markets to rapidly gain share



**Si2400**

First Embedded Modem  
With Silicon DAA



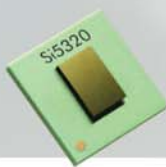
**Si4133**

First RF Synthesizer



**Si3210**

First Integrated  
CMOS SLIC



**Si5320**

Lowest Jitter  
Precision Clock IC



**C8051F350**

First 8051 MCU  
With 24-Bit ADC



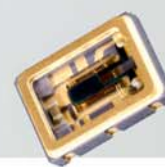
**Si4700**

First CMOS  
Digital FM Tuner



**Si2110**

First Single-Chip Front End  
For Satellite TV



**Si550**

First Quad Frequency  
XOs and VCXOs

# Innovation: DAA Example

**Silicon Labs'  
ISOmodem**



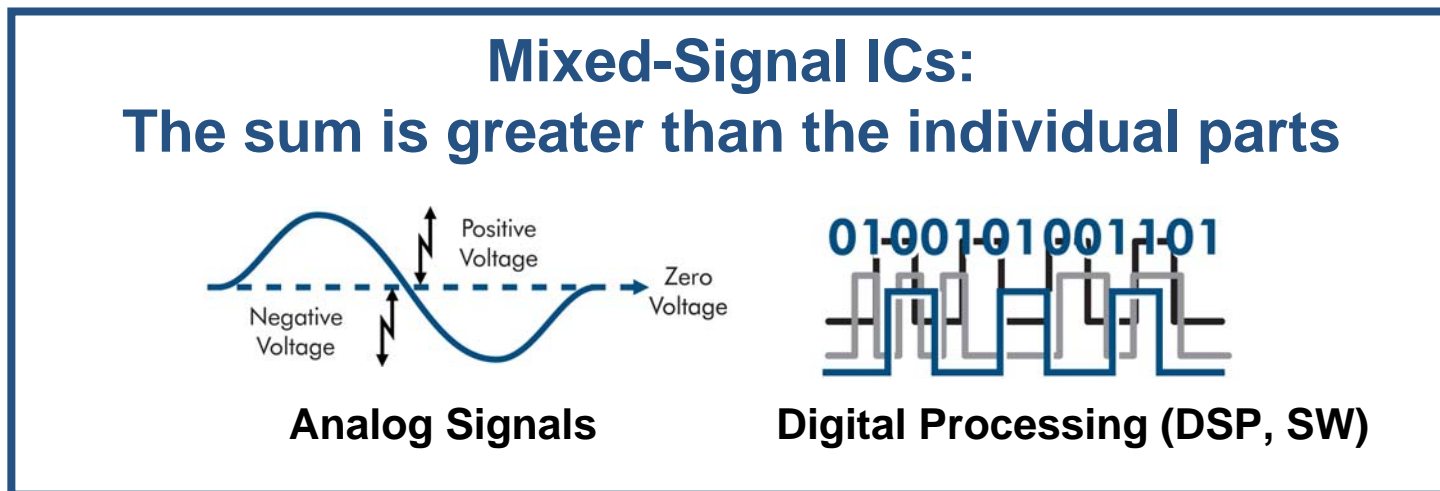
**Traditional Solution**



- ◆ Start with a clean sheet of paper to solve the customers' isolation problems
  - Identify market opportunity
  - Develop a deep understanding of the system
- ◆ Redefine legacy architecture
  - Eliminate need for bulky transformers
  - Resulting silicon DAA technology achieved 75% reduction in board space
  - Global programmability and multiple speeds in single footprint simplify design
- ◆ Market leadership in PC and embedded applications

# Leveraging Moore's Law to Reduce Cost

- ◆ Price will always be a factor, so use every tool available to reduce cost
- ◆ Moore's law provides ever increasing transistor budgets
  - The more "digital" the solution, the better for cost
  - Optimize architectures to integrate analog and digital to achieve the smallest footprint and highest performance possible



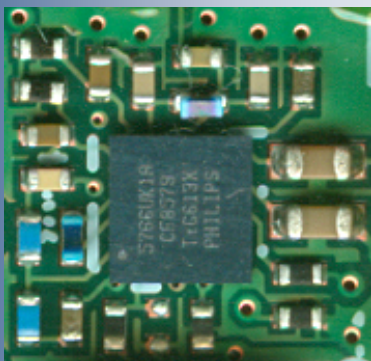
# Moore's Law: FM Tuner Example

## Silicon Labs' Si47xx



10 mm<sup>2</sup> board area  
1 component

## Traditional Solution

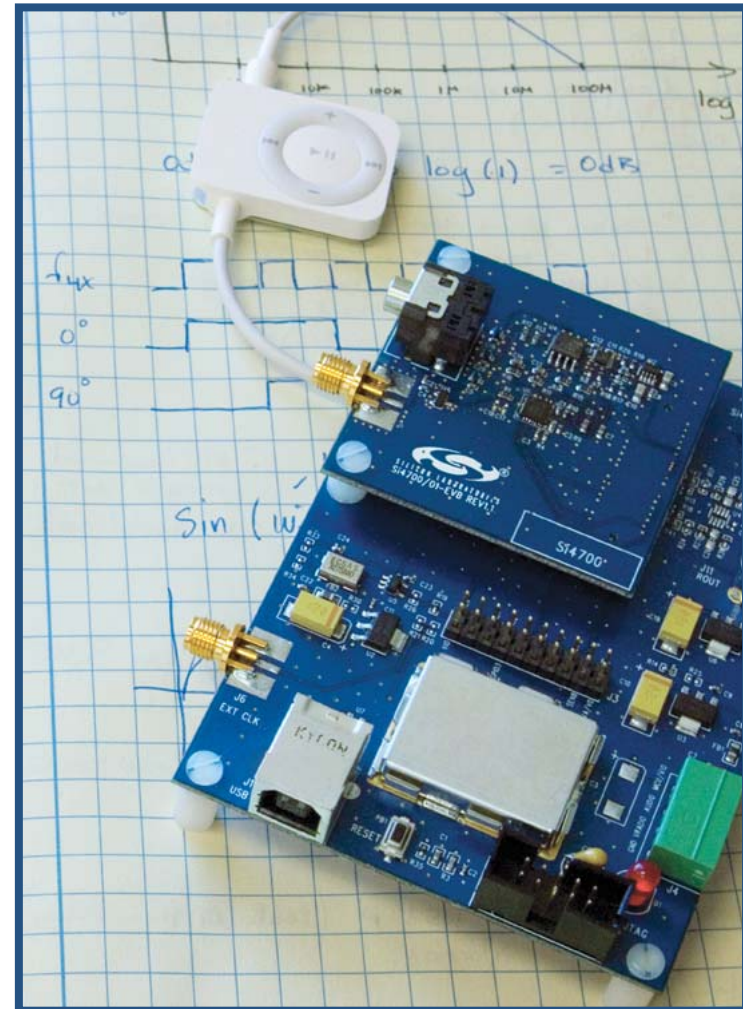


120 mm<sup>2</sup> board area  
30 components

- ◆ Leverage mixed-signal core competency
  - Combine RF with DSP in CMOS
  - Proven RF technology shipped in hundreds of millions of units
  - Solid track record of industry firsts
- ◆ Develop innovative FM receiver family
  - Highly integrated solution with superior performance
  - Reduced bill of materials results in a very cost effective solution
  - Digital low-IF architecture enables enhanced features
  - RDS, audio compression, digital I2S output
- ◆ Achieve revenue growth of more than 100%
  - 2006: \$40M product line in first year of production
  - 2007: 100M units shipped, doubling revenue

# From Innovation to Commercial Success

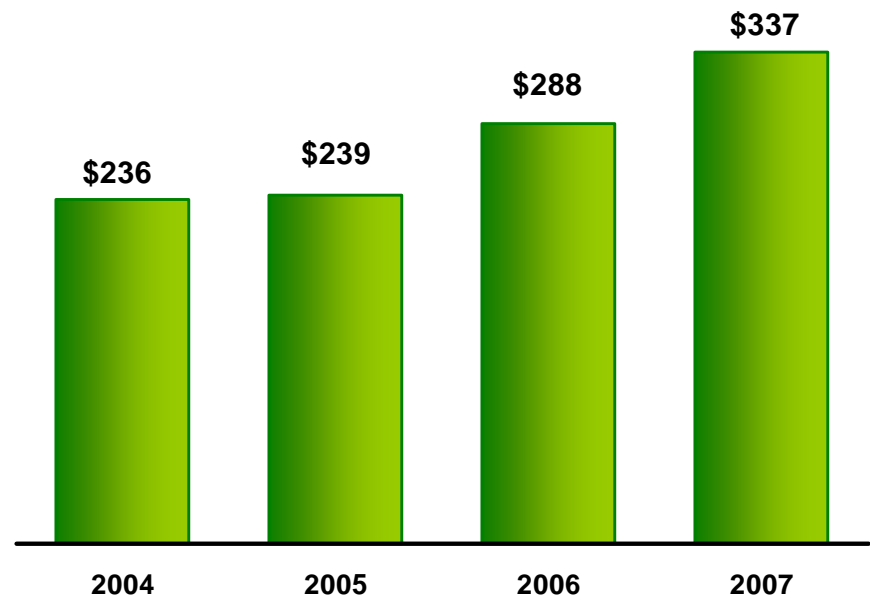
- ◆ Commercial success is the absolute measure of a company's achievements
  - Innovation for the sake of innovation can be a distraction
- ◆ Building a sustainable business model based on innovative technology
  - Anticipate trends in each product segment and look for key markets to drive growth
- ◆ Profitable growth funds future investment
  - Path to increased shareholder value driving a higher valuation



# Commercial Success

◆ Innovators with a proven track record of execution and commercial success:

- Consistently outgrow their industries
- Become market share leaders
- Build sustainable success



Silicon Labs Revenue Growth

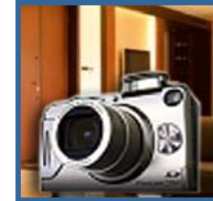
# Combining Talent with Collaboration

- ◆ Hire premier talent and reward excellence
  - Hire the best design, layout, test and applications engineering talent
- ◆ Foster collaboration
  - Leverage strengths and expertise
  - Share and reuse IP, don't reinvent unnecessarily
  - Make sure everyone knows how their piece of the project fits in with the bigger picture



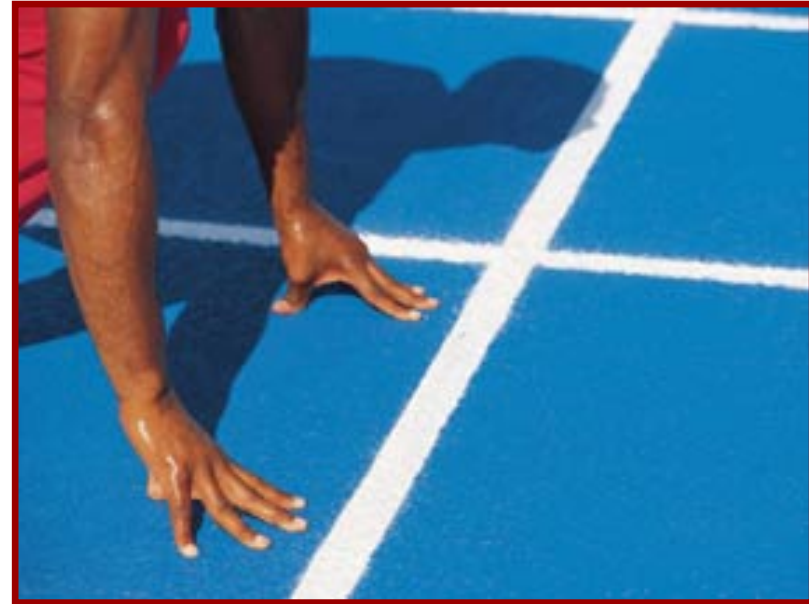
# Collaboration: MCU Example

- ◆ Acquired talented mixed-signal MCU company in 2003
- ◆ Leveraged 8051 core throughout company
  - Programmability speeds time to market
  - Creates new integration opportunities
  - Introduces new skill set
- ◆ Four consecutive years of double-digit revenue growth



# Execution and Desire to Win

- ◆ Meeting commitments matters
  - Accountability across the organization, to customers and to shareholders is what drives success
- ◆ Determination to beat the competition creates a sense of urgency
  - Keeps the focus on getting the job done and meeting schedules
  - Work hard and long hours when necessary to achieve goals
  - Enjoy the satisfaction of winning in the market place



# Competition Eclipsed: F900 Example

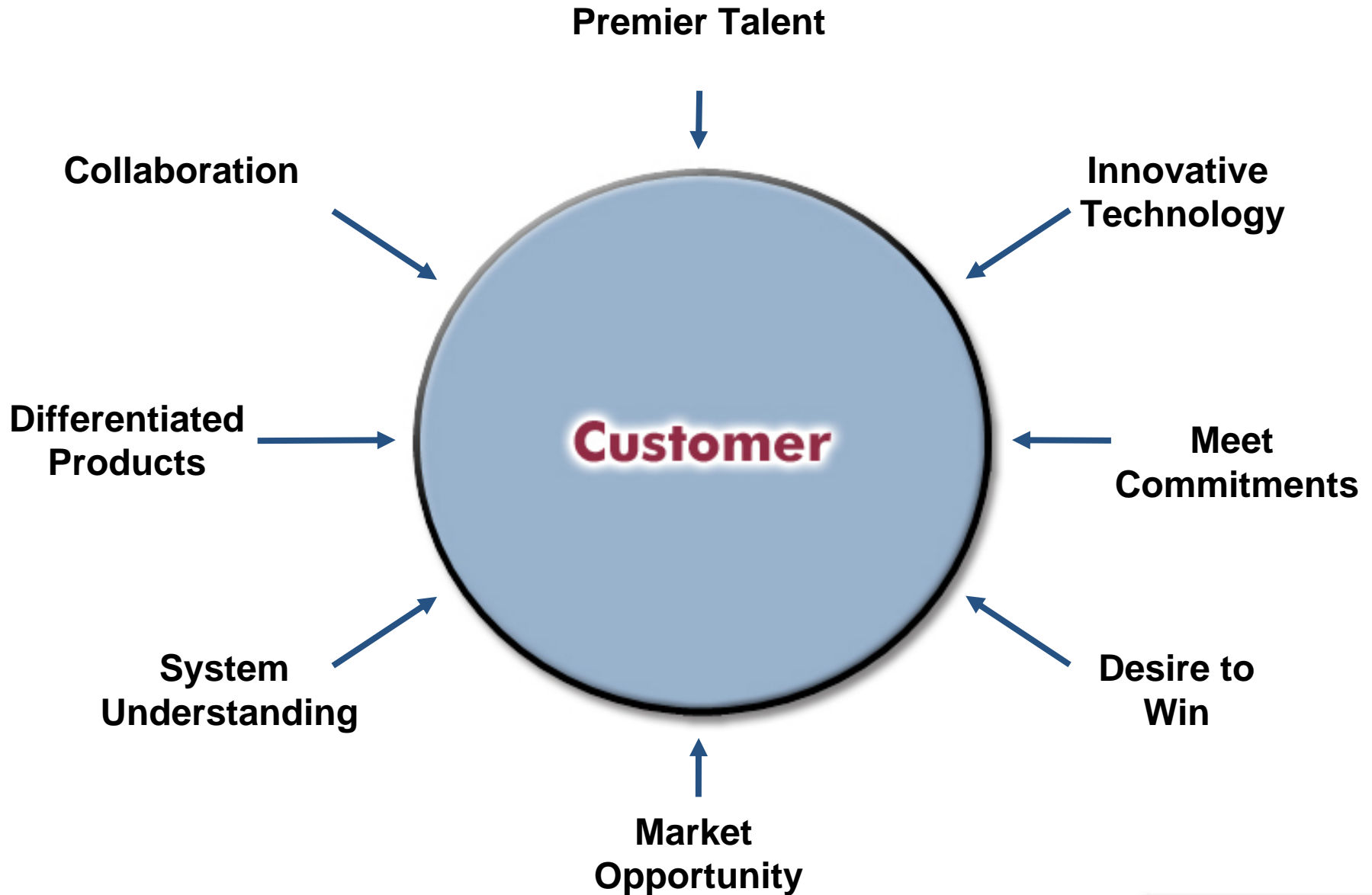
- ◆ F900: Industry's lowest voltage/lowest power MCU
  - Challenging mixed-signal problem
  - Market dominated by one player
  - F900 enables single-cell battery operation for the first time via an integrated DC/DC converter
  - Best-in-class power efficiency: doubles battery life in parallel dual-cell operation
  - Highest functional density: Industry's smallest 64 kB Flash device

**Low voltage/low power MCUs: Architected for low power**

| Technology/Features                              | Ultra-Low Power Sleep Mode | Fast Wake-up and Analog Measurements | Low Active-Mode Current |
|--|----------------------------|--------------------------------------|-------------------------|
| 0.18 um Process Technology                       |                            |                                      | ✓                       |
| Low-Leakage 0.9 – 3.6 V Power Management Unit    | ✓                          |                                      |                         |
| Zero Power Digital State Retention               | ✓                          | ✓                                    |                         |
| 0.9 V RAM Retention                              | ✓                          | ✓                                    |                         |
| LDO Voltage Regulator                            |                            |                                      | ✓                       |
| DC-DC Boost Converter                            |                            | ✓                                    | ✓                       |
| Fast Internal Voltage Reference                  |                            | ✓                                    |                         |
| 300 ksp/s Burst-Mode ADC with 16-bit Accumulator |                            | ✓                                    | ✓                       |
| Port Match Feature                               | ✓                          | ✓                                    |                         |
| 20 MHz Low Power Oscillator                      |                            |                                      | ✓                       |
| SmaRTClock Oscillator                            | ✓                          | ✓                                    |                         |



# Don't Forget it's All About the Customer

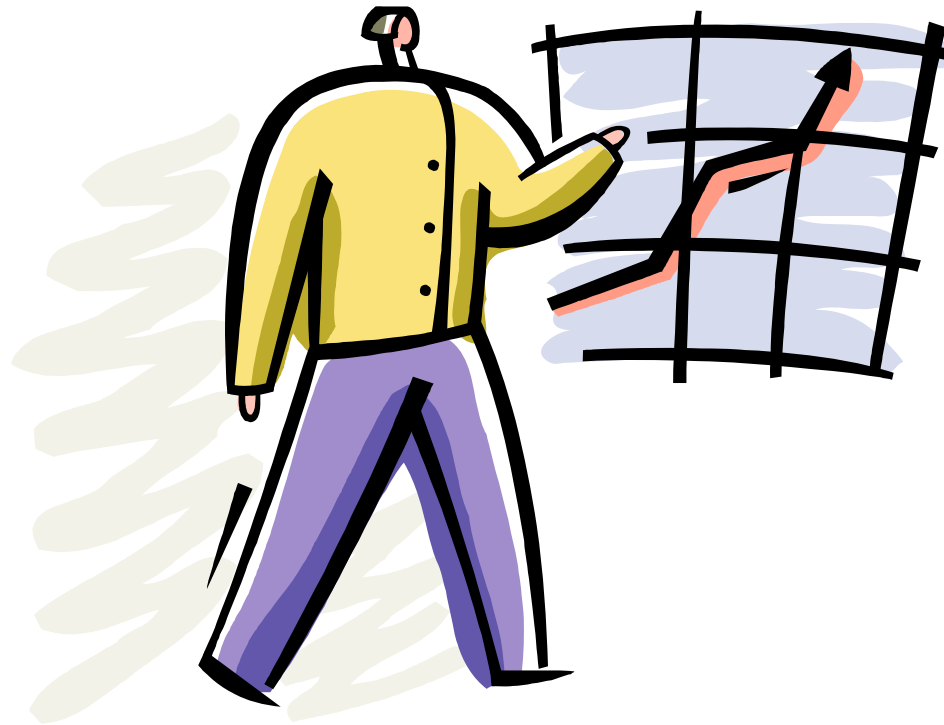


# Global Marketplace

- ◆ It's important to be close physically to customers
- ◆ Engineering talent will continue to be sourced globally
  - Engineering teams will work together “virtually” more and more
  - Need to quickly adapt to the changing geographies of the talent pool
- ◆ Geographic boundaries have become less relevant in a global electronics market

# The End Result

- ◆ Winning combination of growth and profitability
  - Better than industry growth
  - High gross margins
  - Focused investments
  - Strong earnings growth



# About Silicon Labs

- ◆ Semiconductor success story
  - Decade of mixed-signal innovation
  - 29% compounded annual revenue growth
  - > \$330M in revenue
- ◆ Proven, technology leadership
  - 2 billion mixed-signal, CMOS ICs shipped
  - Market leadership in STB and VoB
  - History of industry firsts
- ◆ World-class mixed-signal talent
  - Headquartered in downtown Austin
  - 575 employees
  - Engineering focused
  - Broad IP portfolio



# Summary

- ◆ Innovation is most powerful when it targets commercial success
- ◆ Commercial success also requires:
  - Talent and collaboration
  - Deep knowledge of the customer, application and market
  - Commitment and a desire to win
- ◆ Leveraging technology to reduce cost is part of the innovation
- ◆ Determine how to best capitalize on the globalization of the electronics industry
- ◆ Deliver a growing, profitable business that continues to fund new, exciting R&D projects





S I L I C O N   L A B S

[www.silabs.com](http://www.silabs.com)

# Fractional N PLL design: A tutorial

Axel Thomsen  
Silicon Laboratories Inc.  
Austin, TX

# Outline

- Applications: What can a frac n loop do?
- Delta sigma function and difficulties
- Noise Analysis: simple PLL and its noise compared to frac N and its extra noise source
- Nonlinearity effects
- Phase noise reduction technique
- Circuit building blocks: divider, phase detector, phase error DAC
- Example designs: good VCO with low bandwidth, bad VCO with high bandwidth
- Experimental data from a programmable crystal oscillator IC

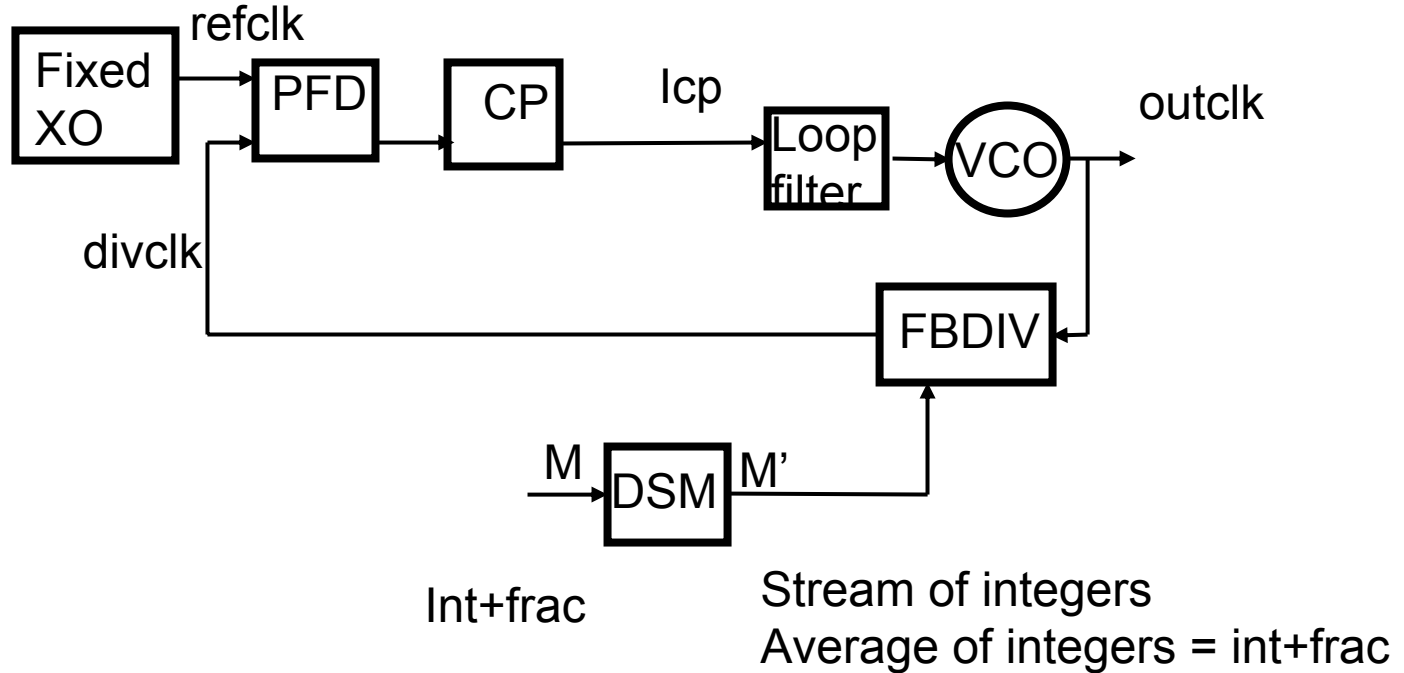
# Applications:

## What can a frac n loop do?

- produce arbitrary frequency relationships
- produce arbitrary phase relationships
- Modulation port (FM, PM): Numerically controlled oscillator
- Decouples update rate from channel spacing. Integer loop:  $\Delta f_{\text{out}} = f_{\text{update}}$ , so a 20kHz channel spacing results in 2kHz loop bandwidth

# A fractional N PLL

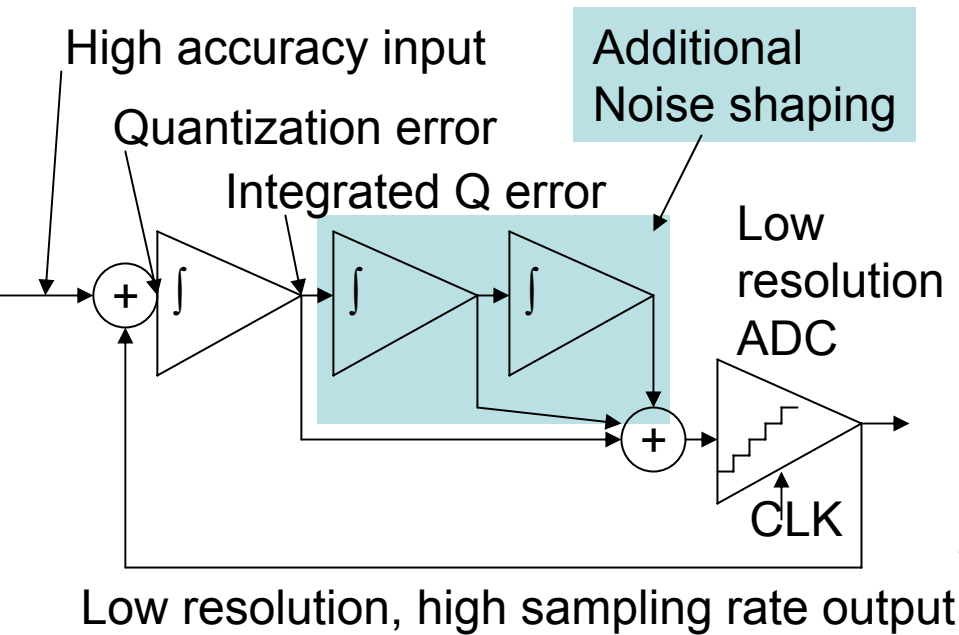
Average of divclk  
aligns with refclk



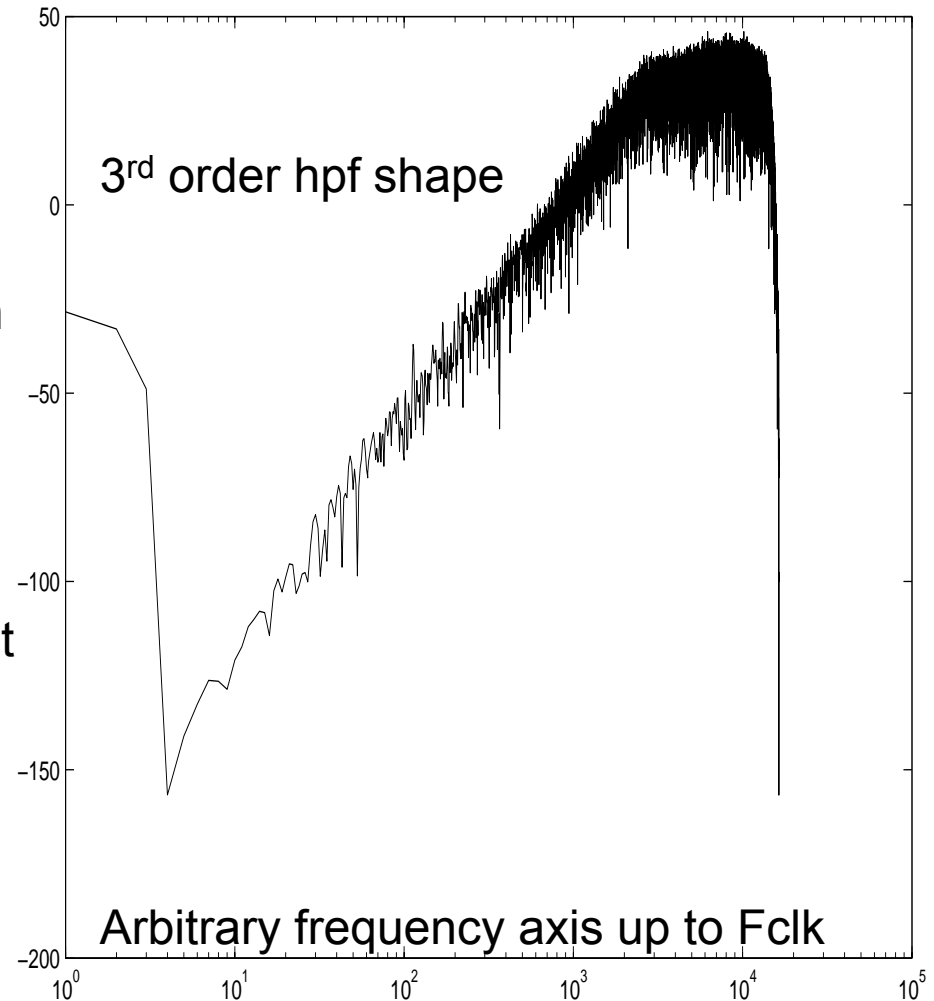
# Delta sigma modulator

- A method to create a sequence of integers that approximates a fraction
- Oversampling: sampling frequency exceeds nyquist criterium – in practice, it means that there is a bandwidth available where noise will not matter or filtering will not be problematic – ‘don’t care band’
- Noise-shaping: noise added by quantizing the fraction to an integer will appear mostly at high frequencies – in the ‘don’t care band’
- low frequency accuracy: use high gain at DC to match output stream to input value
- high frequency noise: Shape error ‘out of band’ with a HPF, then remove it by low pass filtering
- Caution: Fixed patterns occur for certain inputs e.g. 001001001 for  $\frac{1}{3}$

# Delta sigma modulator



$$\text{adcin} = 2 \cdot \text{int1} + 1.5 \cdot \text{int2} + 0.5 \cdot \text{int3} \text{ [Song]}$$



# Delta sigma modulator

- In a frac N loop the divide ratio (period of the feedback clock) is modulated to average a certain value.
- Where is the ‘Don’t care band’? Generally phase noise or jitter are measured wideband – we place noise beyond the loop bandwidth, up to the update rate and filter
- High OSR is good: here it is  $f_{\text{update}}/f_{\text{loopbw}}$

# Delta Sigma Modulator

- Noise shaping in phase is one order less than frequency
- Need to have sufficient filtering in 'don't care band' – low enough frequency and high enough order

# Delta Sigma Modulator

## Difficulties:

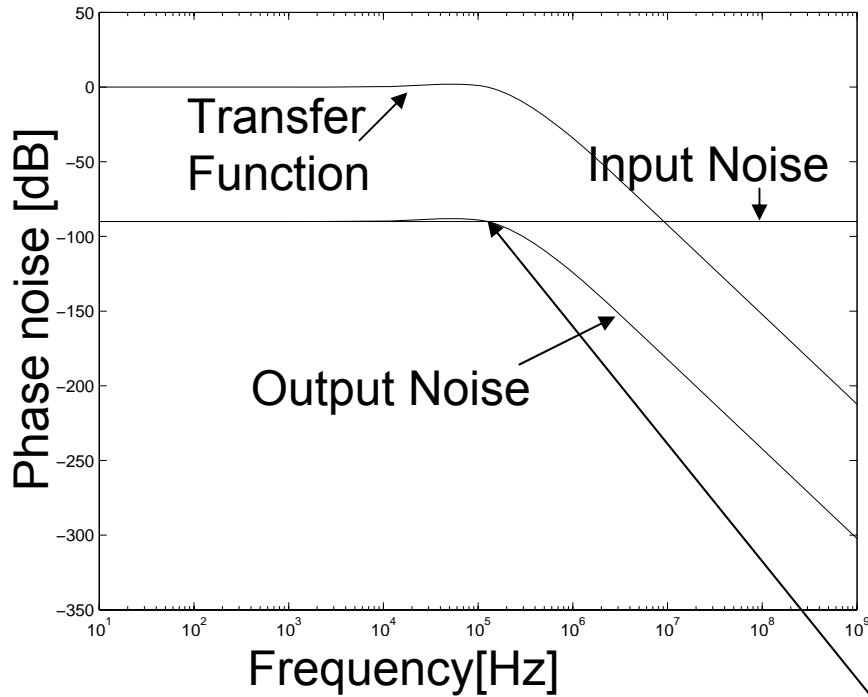
- Need dither to break up patterns (e.g. dither at comparator, set LSB to 1)
- linearity in processing high frequency noise is required – nonlinearity will cause spurs
- intermodulation will cause elevated 'in-band' noise

# Noise Analysis

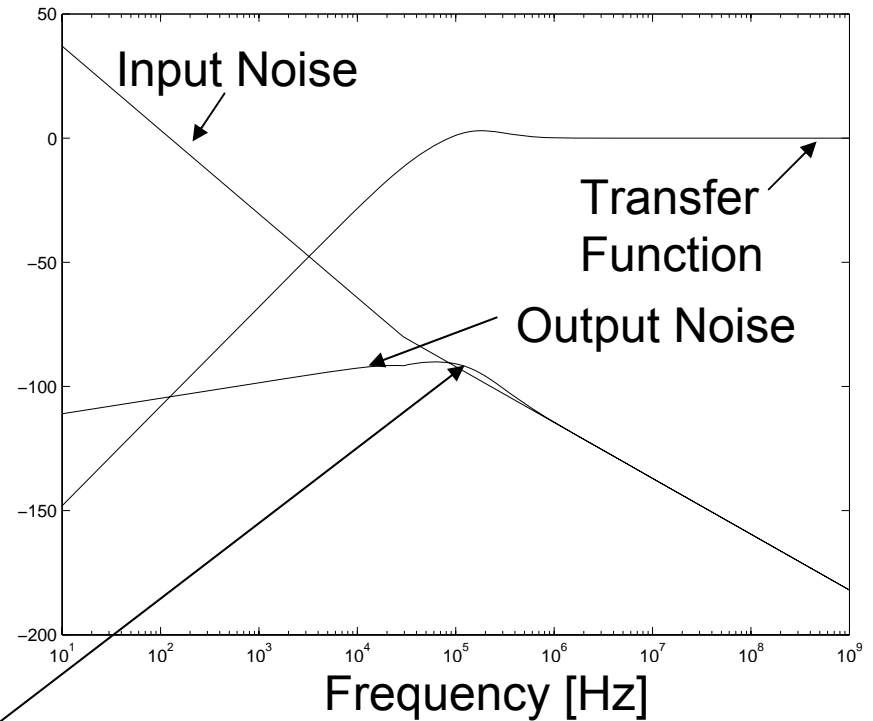
- simple PLL and its noise: PD, VCO
- LPF for PD: loop BW plus higher poles
- HPF for VCO: loop BW and lower zero
- Peaking caused by low frequency zero, high frequency poles, lack of phase margin
- Optimization – set loop bw to make PD and VCO equal contributors (wide bw for bad VCO, low bw for good VCO)
- Rule of thumb – max bandwidth  $f_{\text{update}}/10$

# Noise Analysis of integer loop

Phase detector

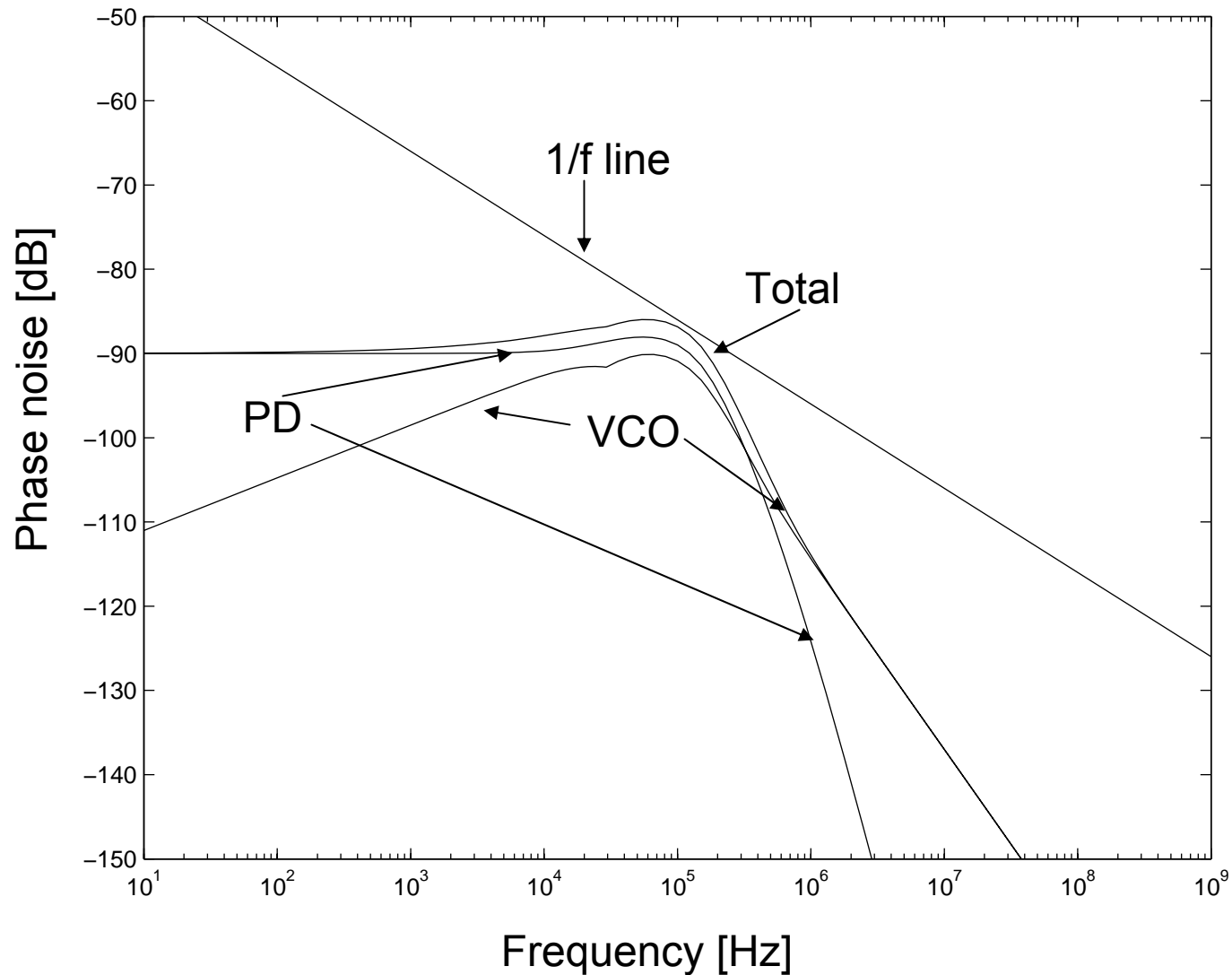


VCO



Optimum noise of the PLL: line up these two points

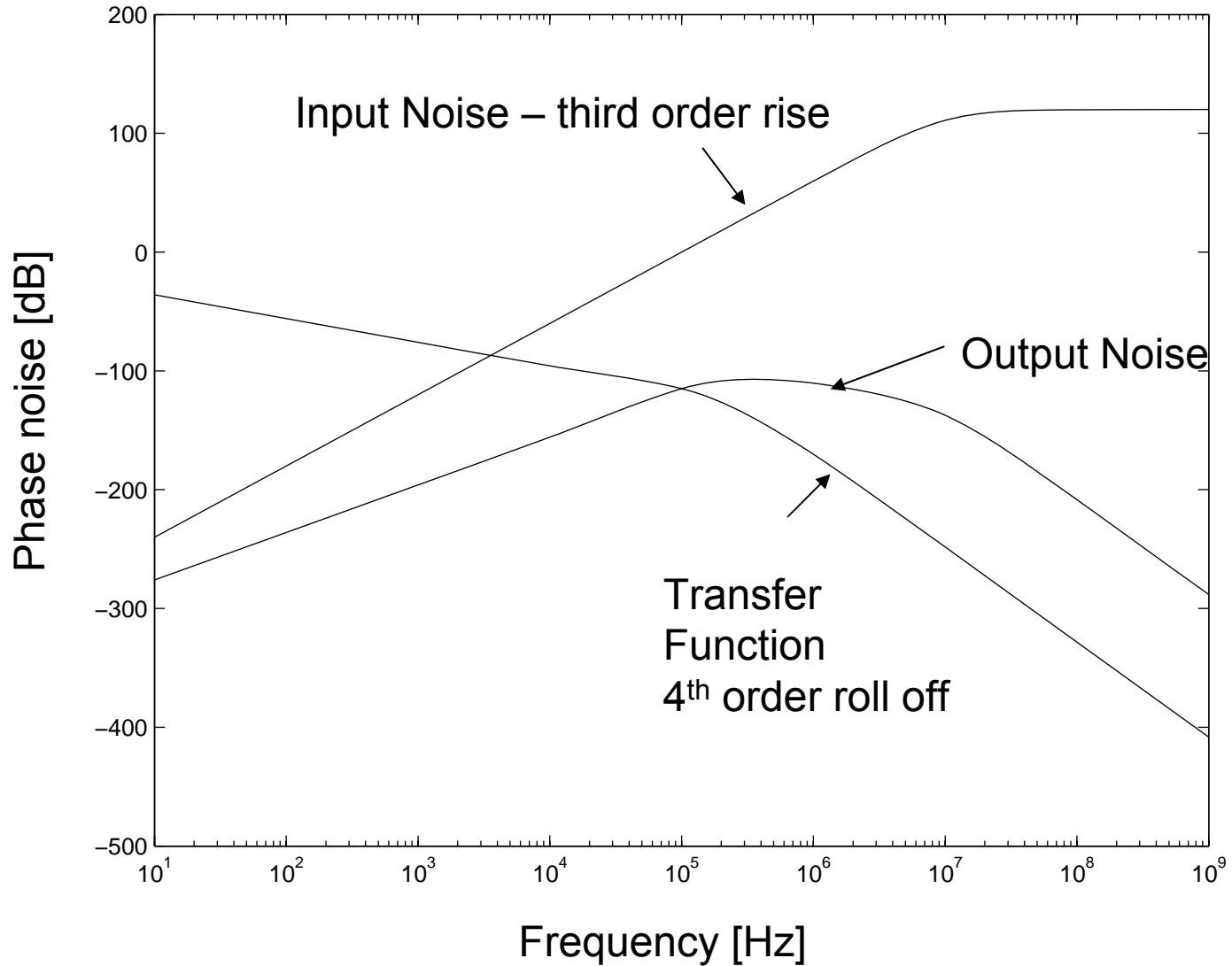
# Noise spectrum of integer loop



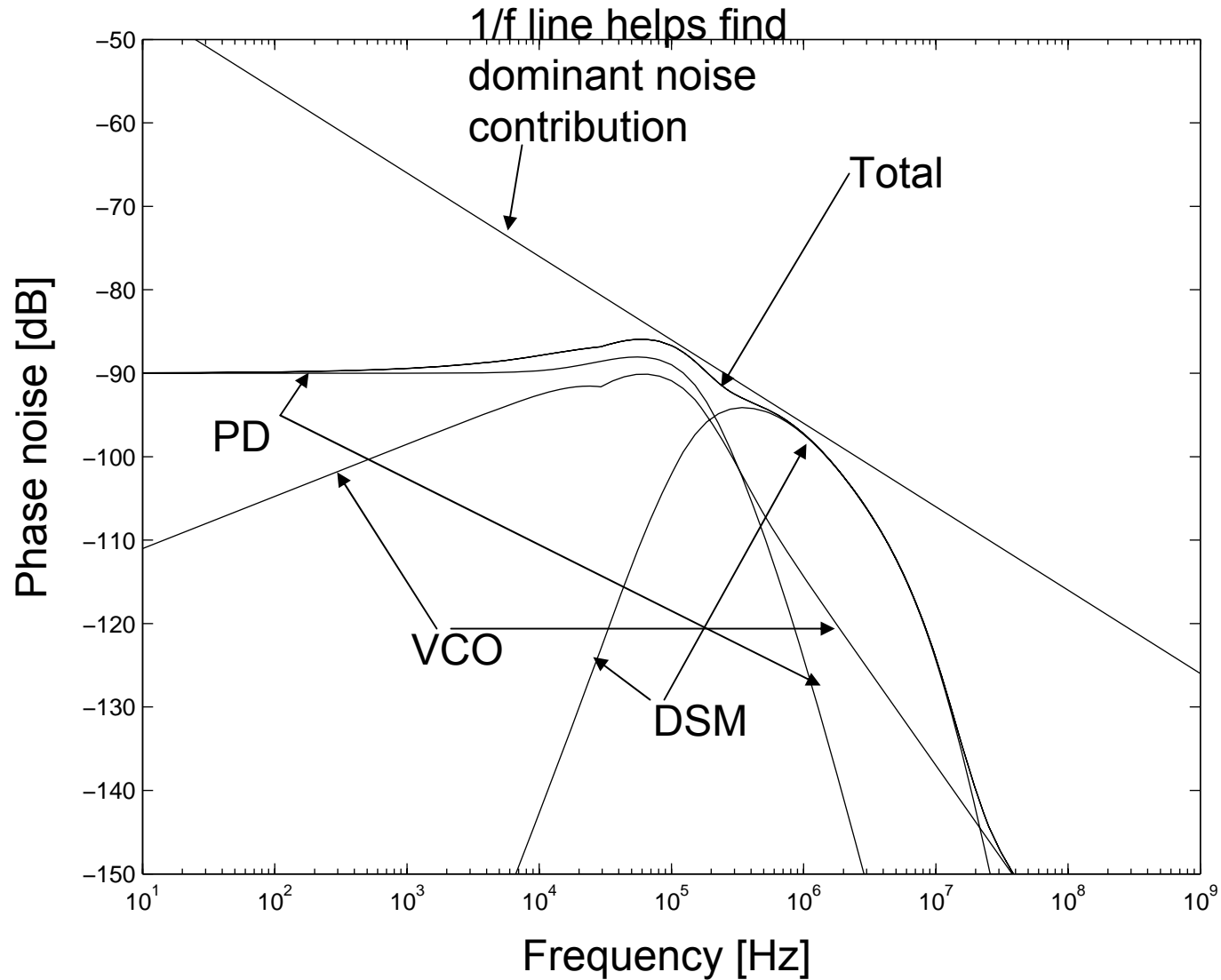
# Noise Analysis

- frac N and its extra noise source: PD, instantaneous phase error, VCO
- Additional noise source: instantaneous phase error introduced by divider
- Similar to PD noise in transfer function
- Noise shaped by high pass of N-1 order!
- Must include N poles in LPF transfer function to remove this contribution

# Noise contribution of the DSM



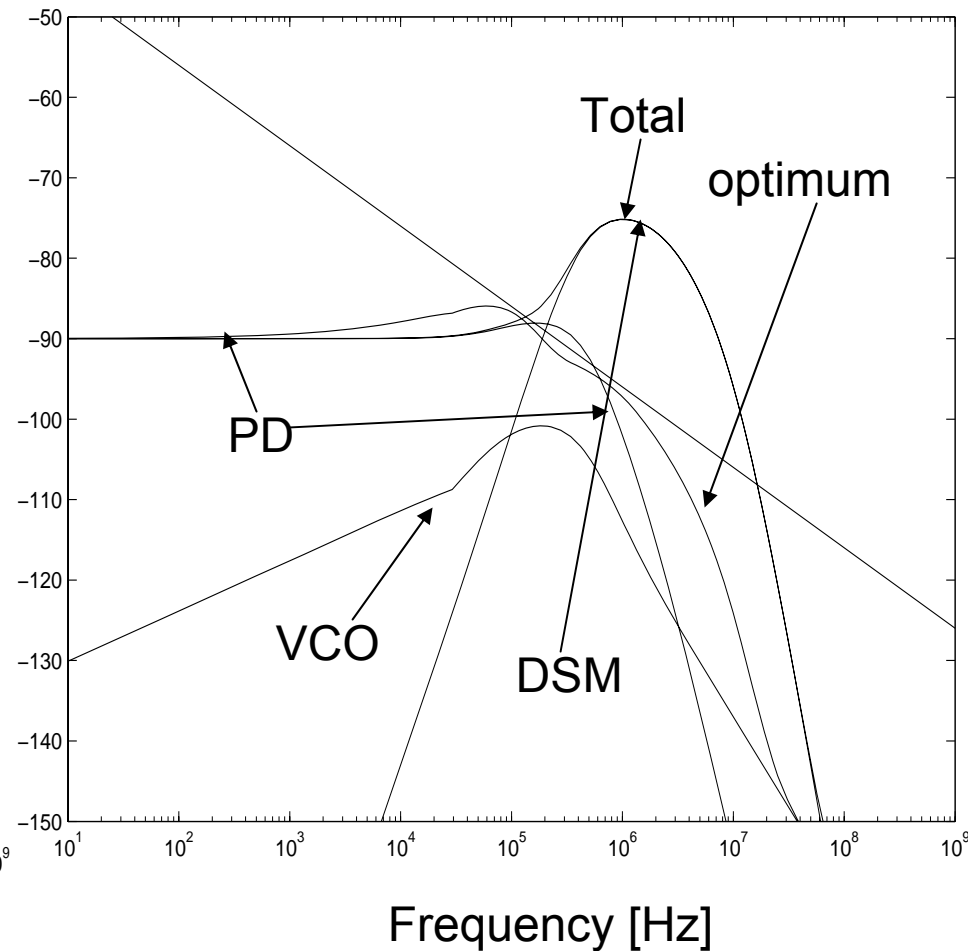
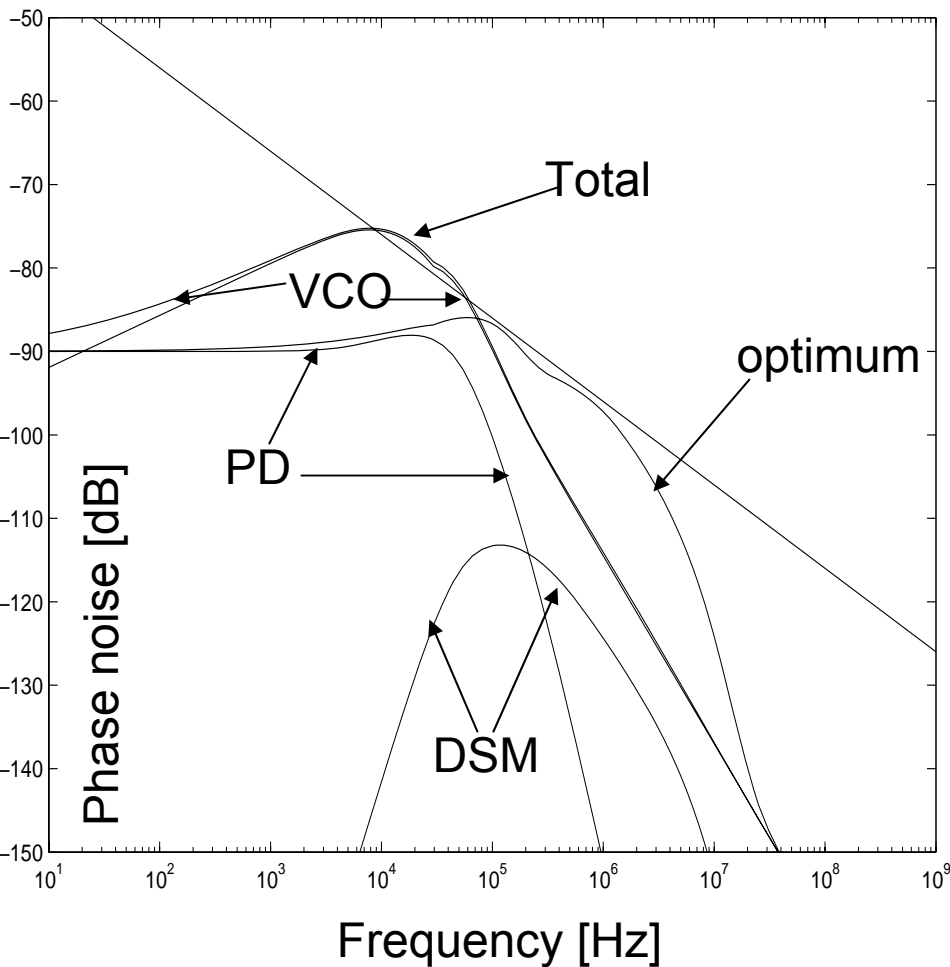
# Total loop noise



# Effect of wrong loop bandwidth

Low bandwidth – VCO dominates

High bandwidth – DSM (PD) dominates



# Impact of instantaneous phase noise

- Requires low loop bandwidth to create don't care band  $f_{\text{loopbw}} \ll f_{\text{update}}/10$
- Requires extra filtering that costs phase margin
- Limited useful bandwidth when used as a modulator
- Everything gets better for high update rates!

# How else to get rid of quantization noise: phase error cancellation

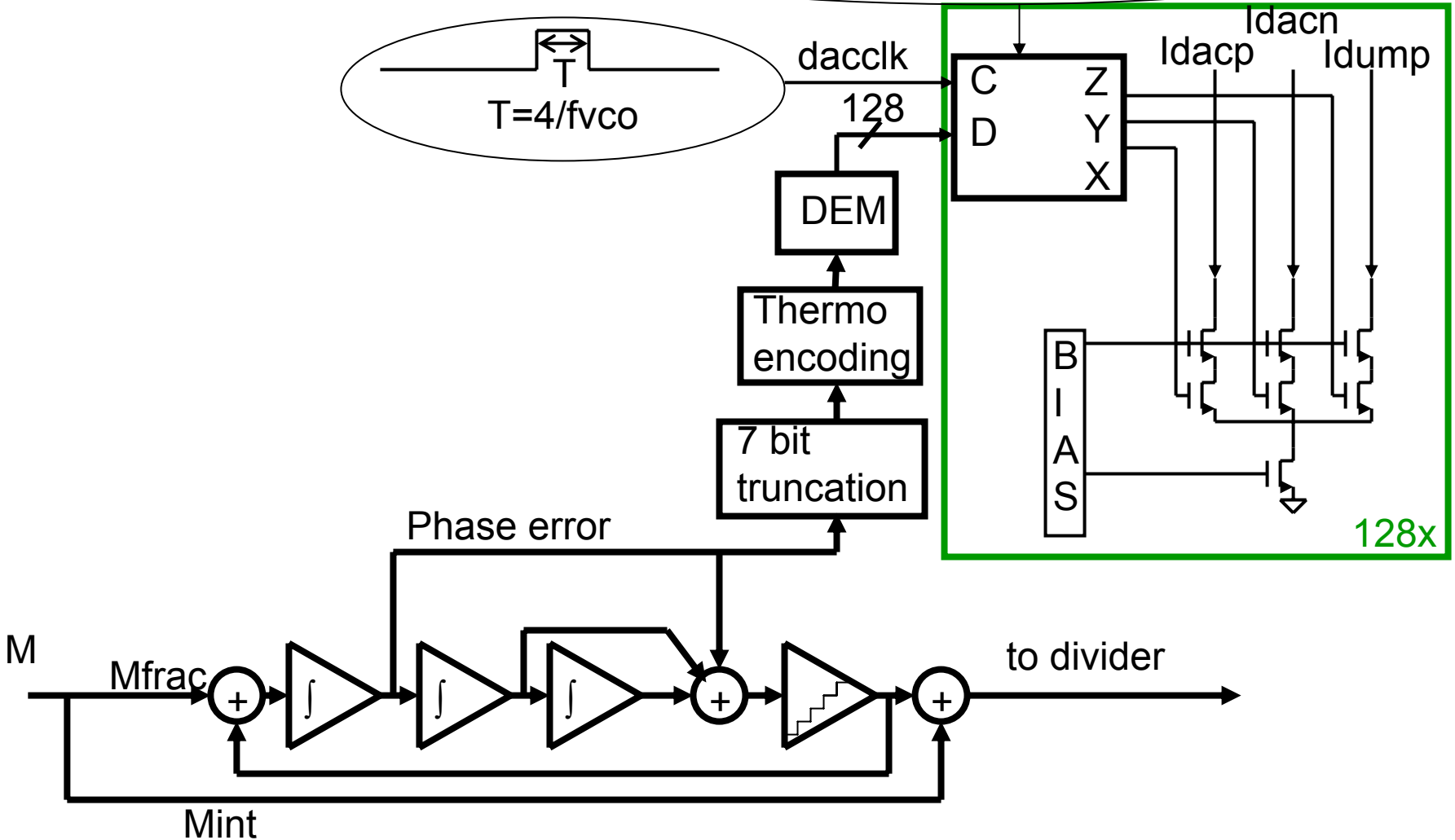
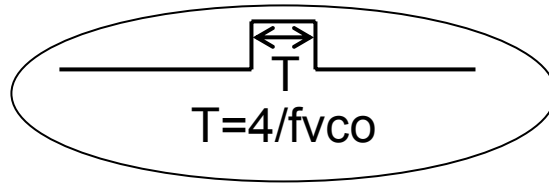
- Filtering is most common way – but sometimes the don't care band is too small
- Quantization noise is known a priori – it is calculated in the delta sigma itself
- Instantaneous period error = input-feedback
- Instantaneous phase error = output of integrator 1
- No extra digital hardware required
- Charge delivered by charge pump can be cancelled by DAC

$$Q_{cp} = K_{cp} * \Delta\Phi = I_{cp} * \Delta\Phi * T_{VCO} = Q_{DAC}$$

- Limitation: gain error, dac resolution, dac nonidealities

# Phase error cancellation

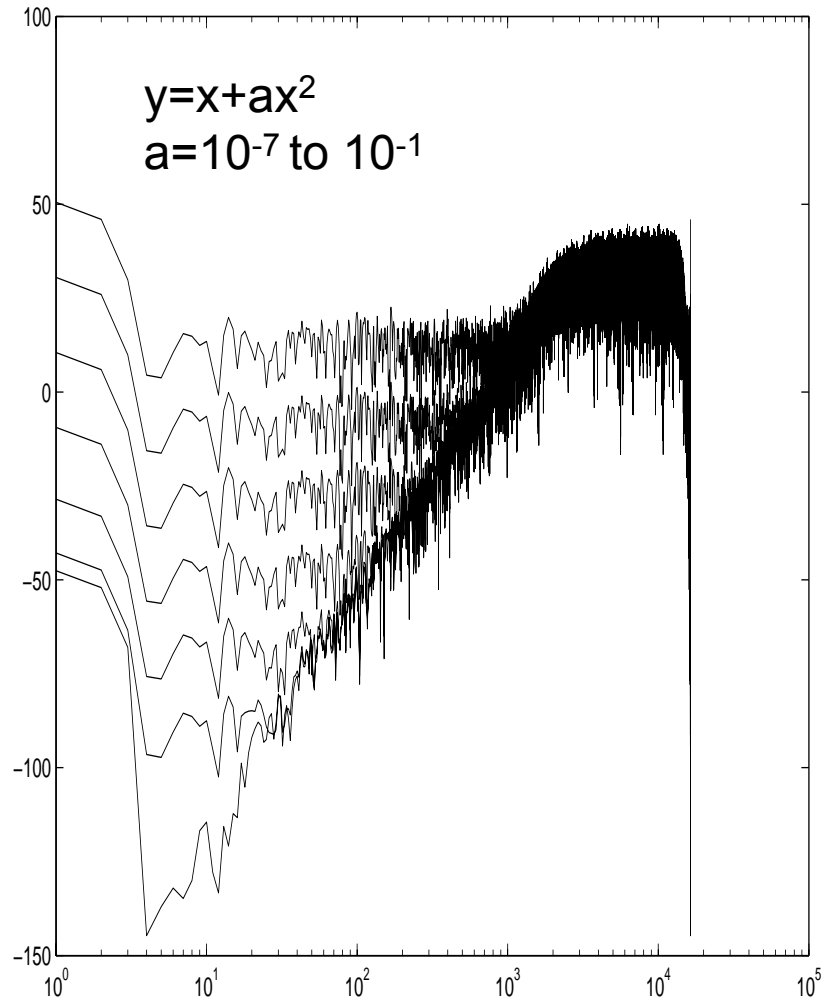
Logic:  $X=CD$ ;  $Y=CD$ ;  $Z=\bar{X}+\bar{Y}$ , overlapping



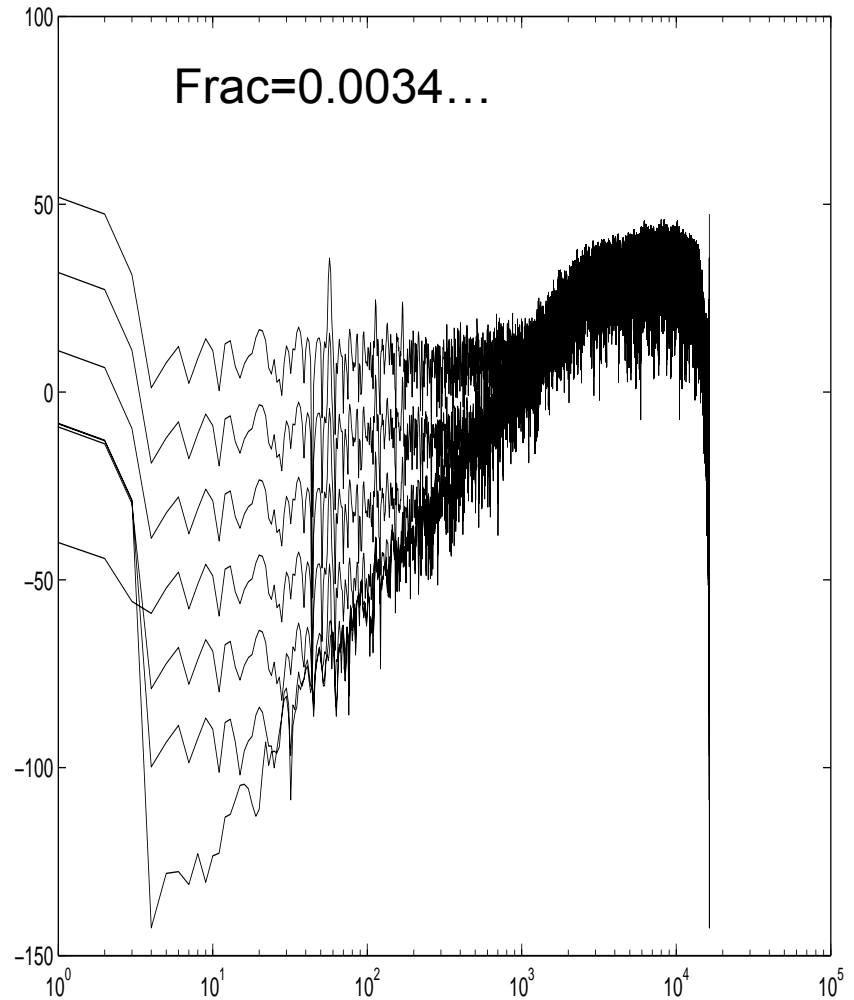
# Noise Analysis

- Additional noise source: intermod in PD
- What happens in a nonlinearity  $x^2$ ?
- Create signals at  $\sin(f)$ ,  $\sin(2f)$
- Creates intermod at  $\sin(f_1-f_2)$ ,  $\sin(f_1+f_2)$
- There is a lot of out of band noise, it does not take large nonlinearity to create noticeable intermodulation

# Effect of Intermodulation



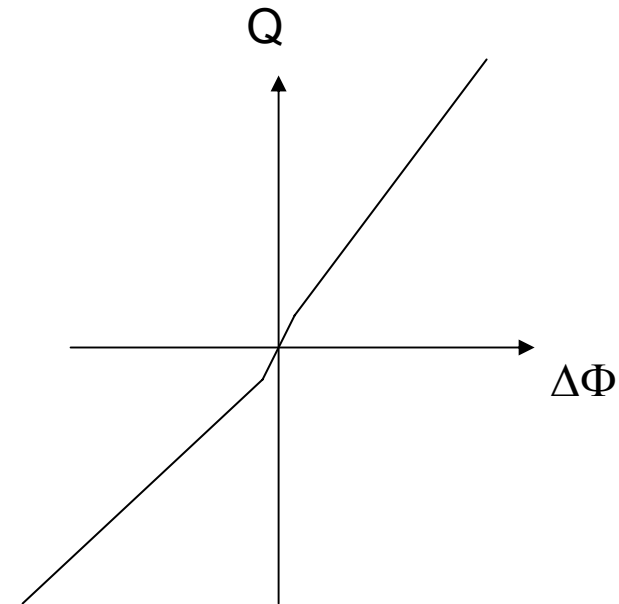
Typical spectrum after  $y=x+ax^2$   
is applied: low frequency noise fills in



Special case for near integer input:  
Spurs get generated

# Circuit building blocks: phase detector

- Impact of nonlinearity on noise shaped signal is shown
- Phase detector/charge pump converts phase error to charge packet  $Q = k * \Delta\Phi$
- Any deviation from this linear expression results in intermodulation, noise, spurs

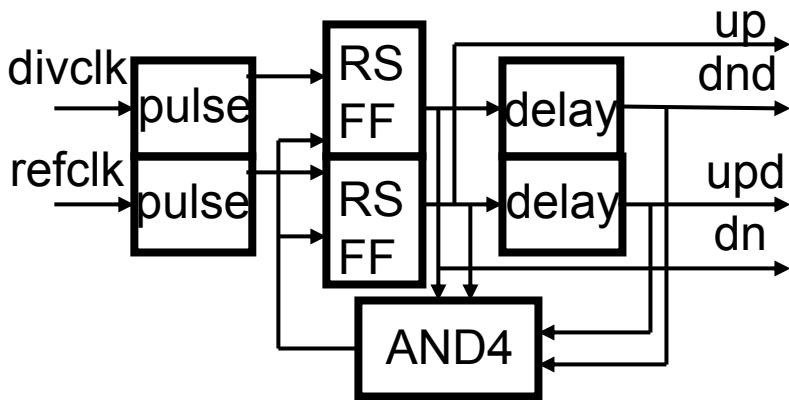


# Phase detector evolution 1

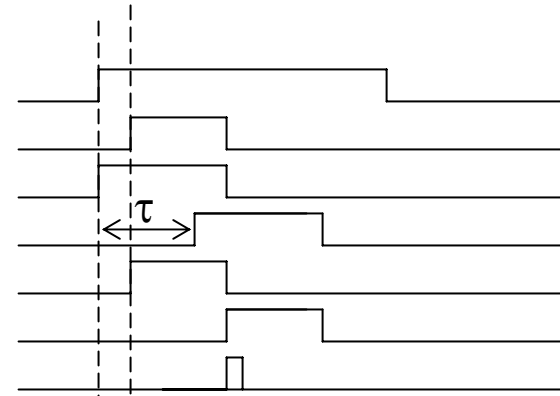
## Goals:

- Linearity is very important
- avoid change of sequence around zero crossing      up-down-reset vs. down-up-reset
- Fully differential operation for even order distortion suppression
- Frequency acquisition behavior like UpDownReset PFD.

# Phase detector logic

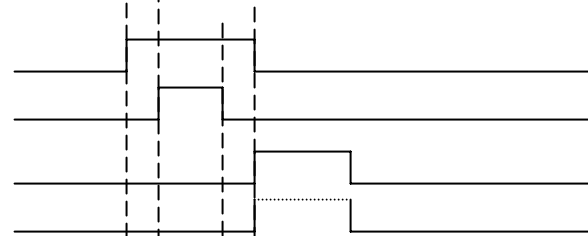


Refclk  
Divclk  
Up  
Up\_del  
Down  
Down\_del  
reset



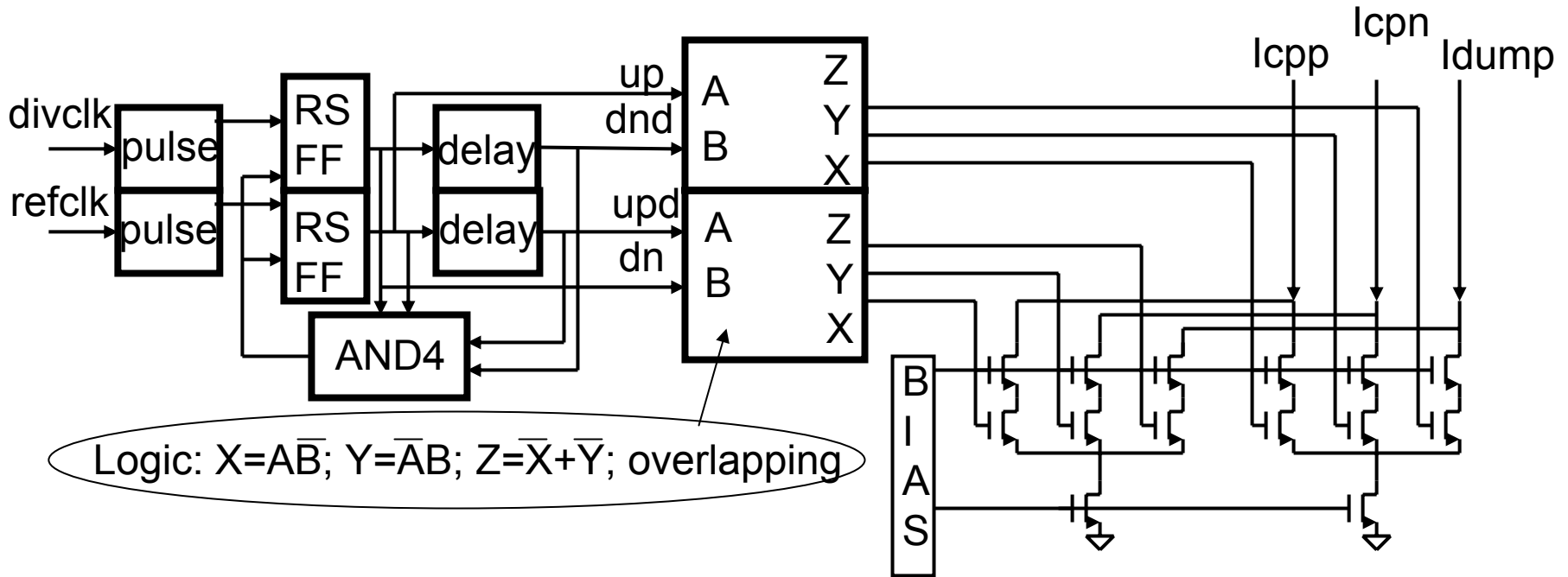
$Up \cdot \overline{dnd}$   
 $\overline{Dn} \cdot \overline{upd}$   
 $\overline{Up} \cdot dnd$   
 $\overline{Dn} \cdot upd$

lcpn1  
lcpp1  
lcpn2  
lcpp2



$\Delta\Phi$   $\Delta\Phi$

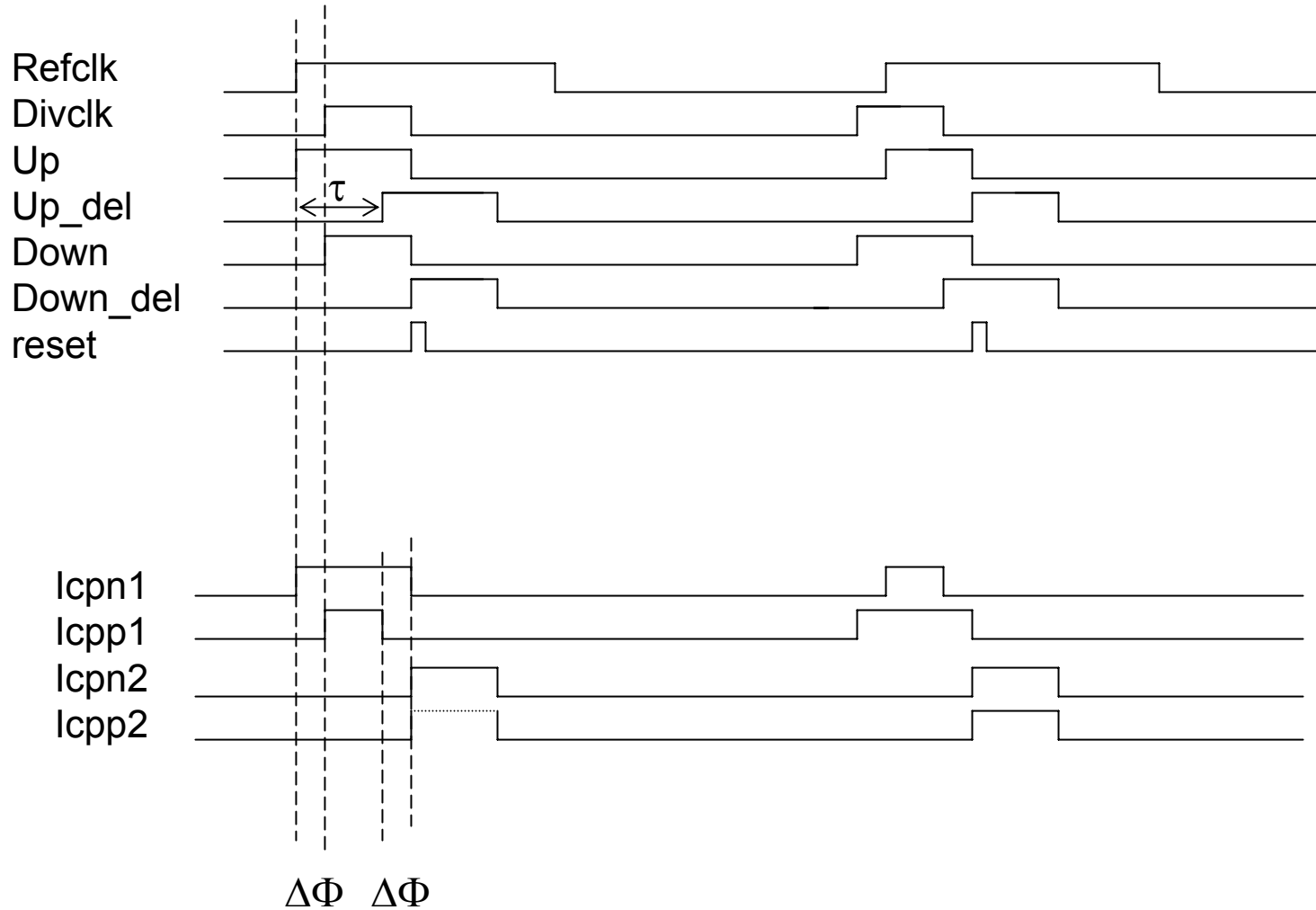
# Phase detector implementation



Fully symmetrical, fully differential

For  $\Delta\Phi < \text{delay}$  very linear – less than 1ps deviation from straight line

# Phase detector waveforms

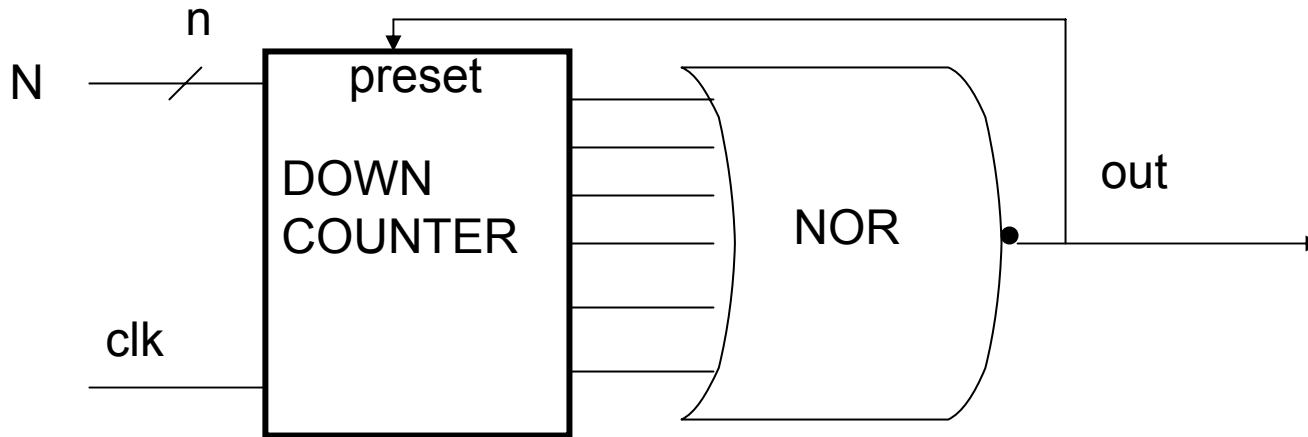


# Circuit building blocks: Divider

- Multibit DSM requires multi-rate divider
- Phase error from divider must be avoided
  - retiming required
- Divider output drives DSM to calculate next divider value
- Timing issues! Divider runs at VCO speed!
- Startup issues! Drives its own clock.

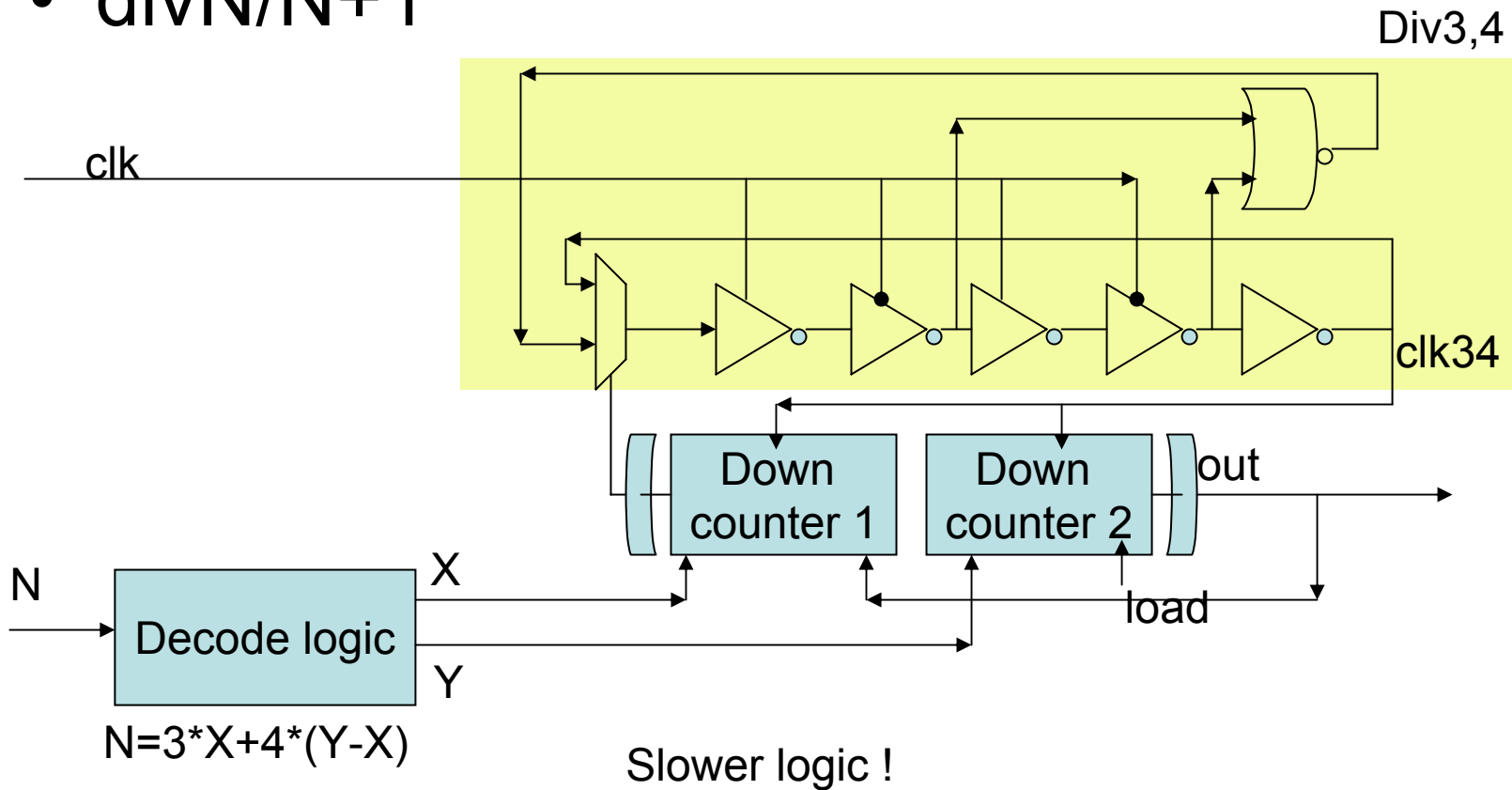
# Circuit building blocks: Divider

- Programmable down counter



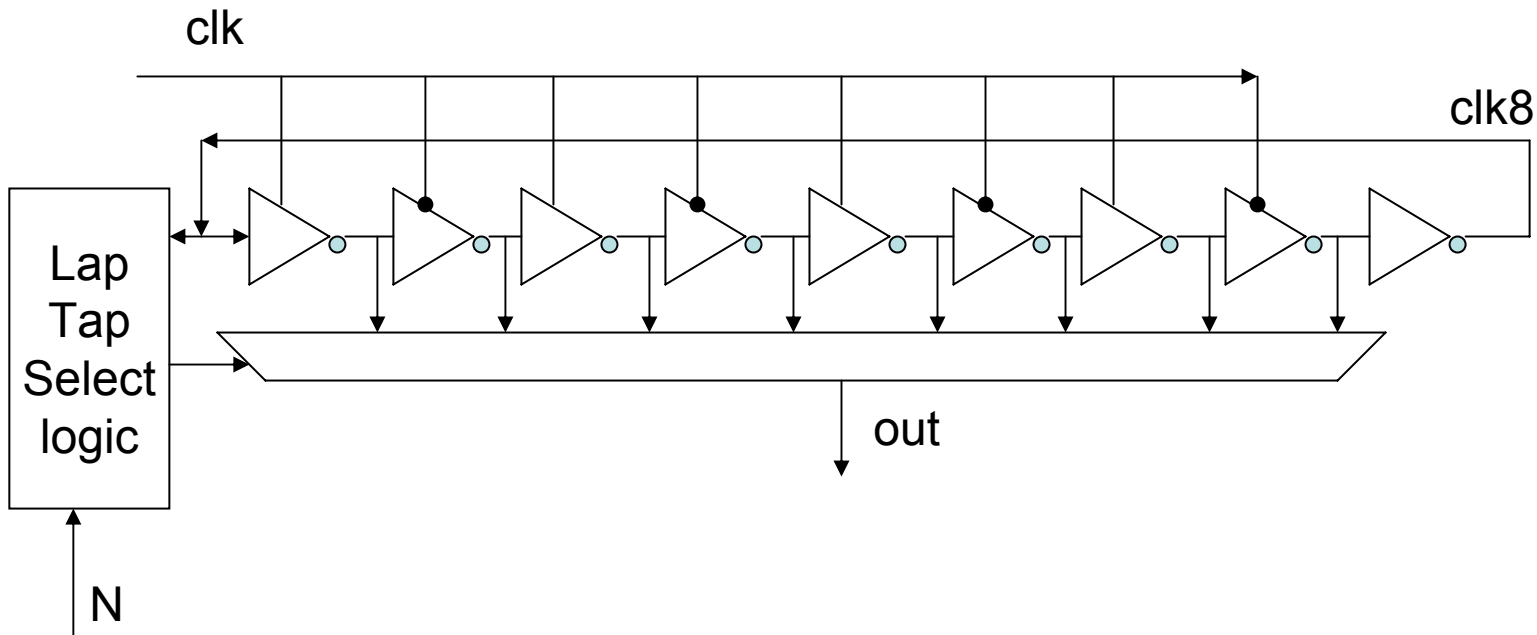
# Circuit building blocks: Divider

- $\text{div}N/N+1$



# Circuit building blocks: Divider

- Phase select divider: de Muer, Si570

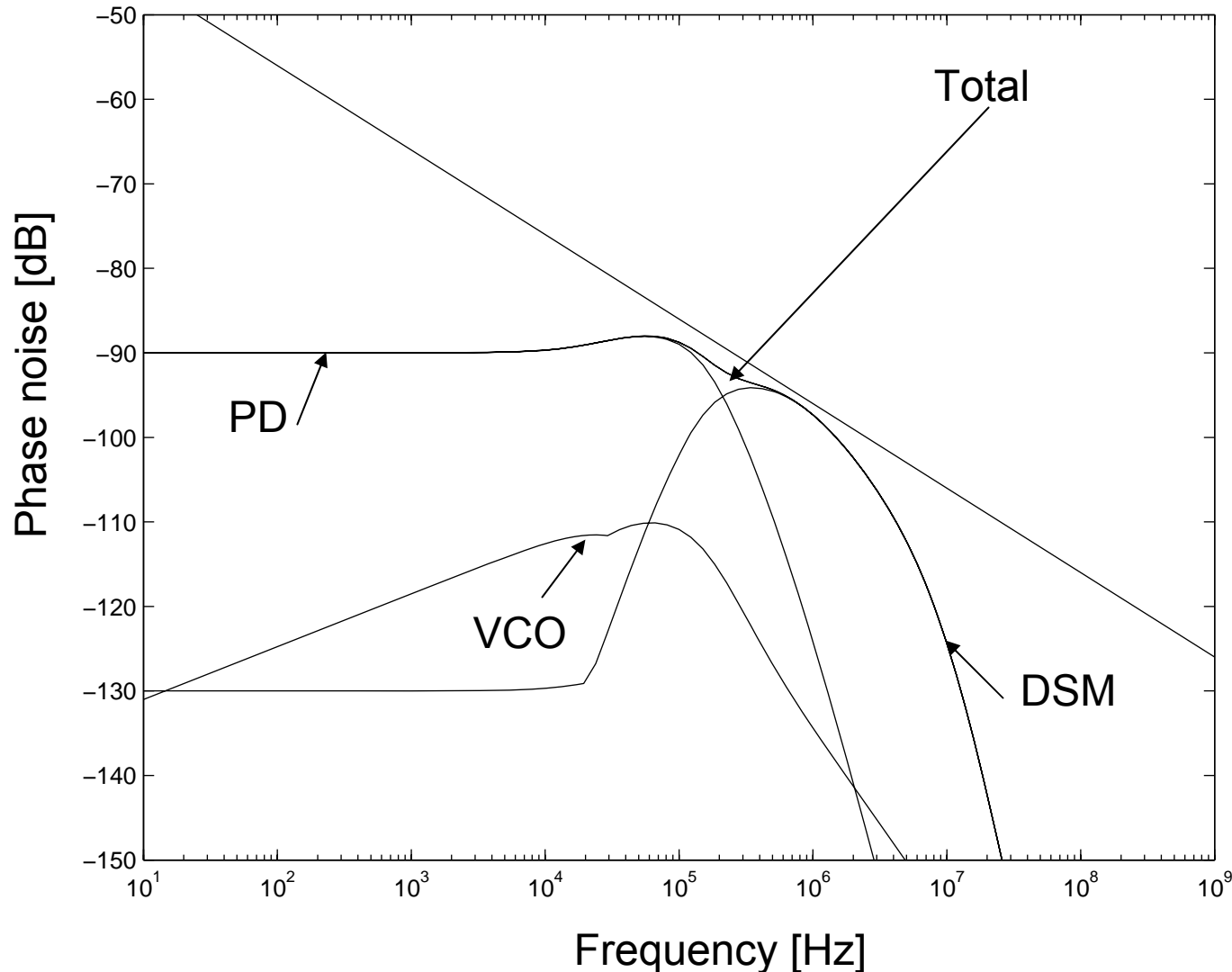


Slowest logic !

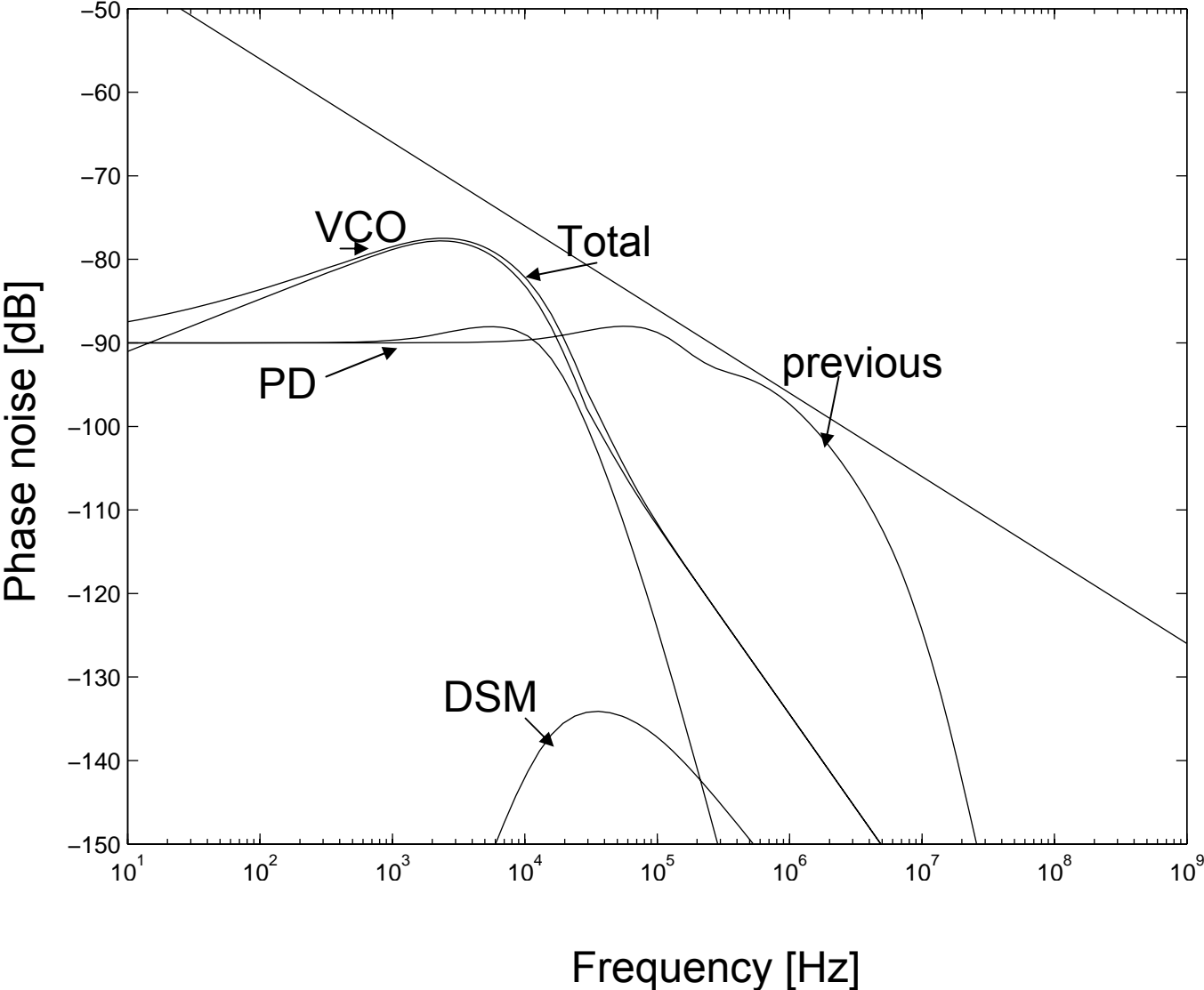
# Example design1

- good VCO with low bandwidth, high update rate
  - Good VCO puts target design at low bandwidth
  - Frac noise is best attenuated by low bandwidth and additional poles
  - PD noise becomes insignificant at low bandwidth
  - Biggest risk: nonlinearity in PD

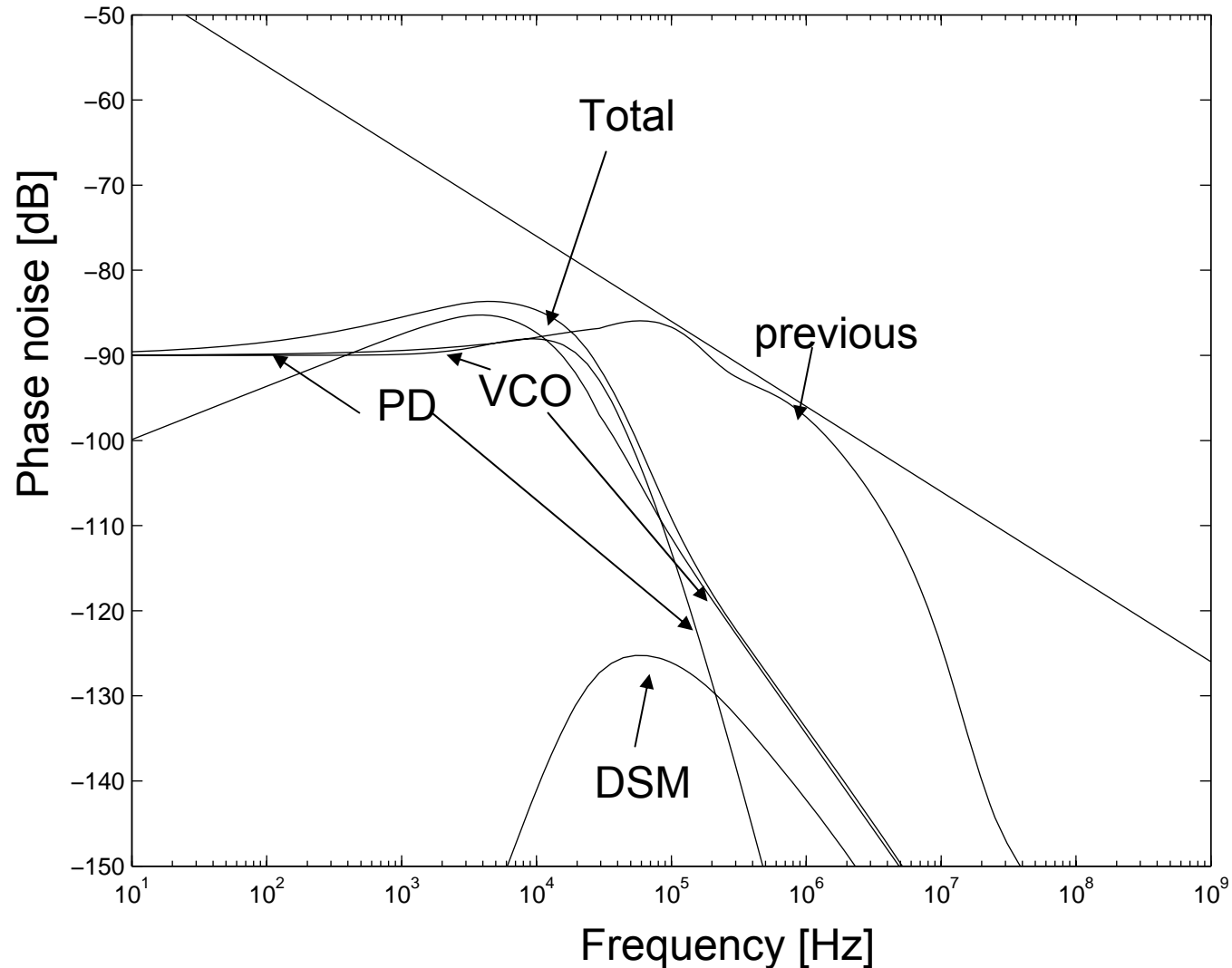
Very good VCO, so pd, DSM dominate  
we should reduce the loop bandwidth



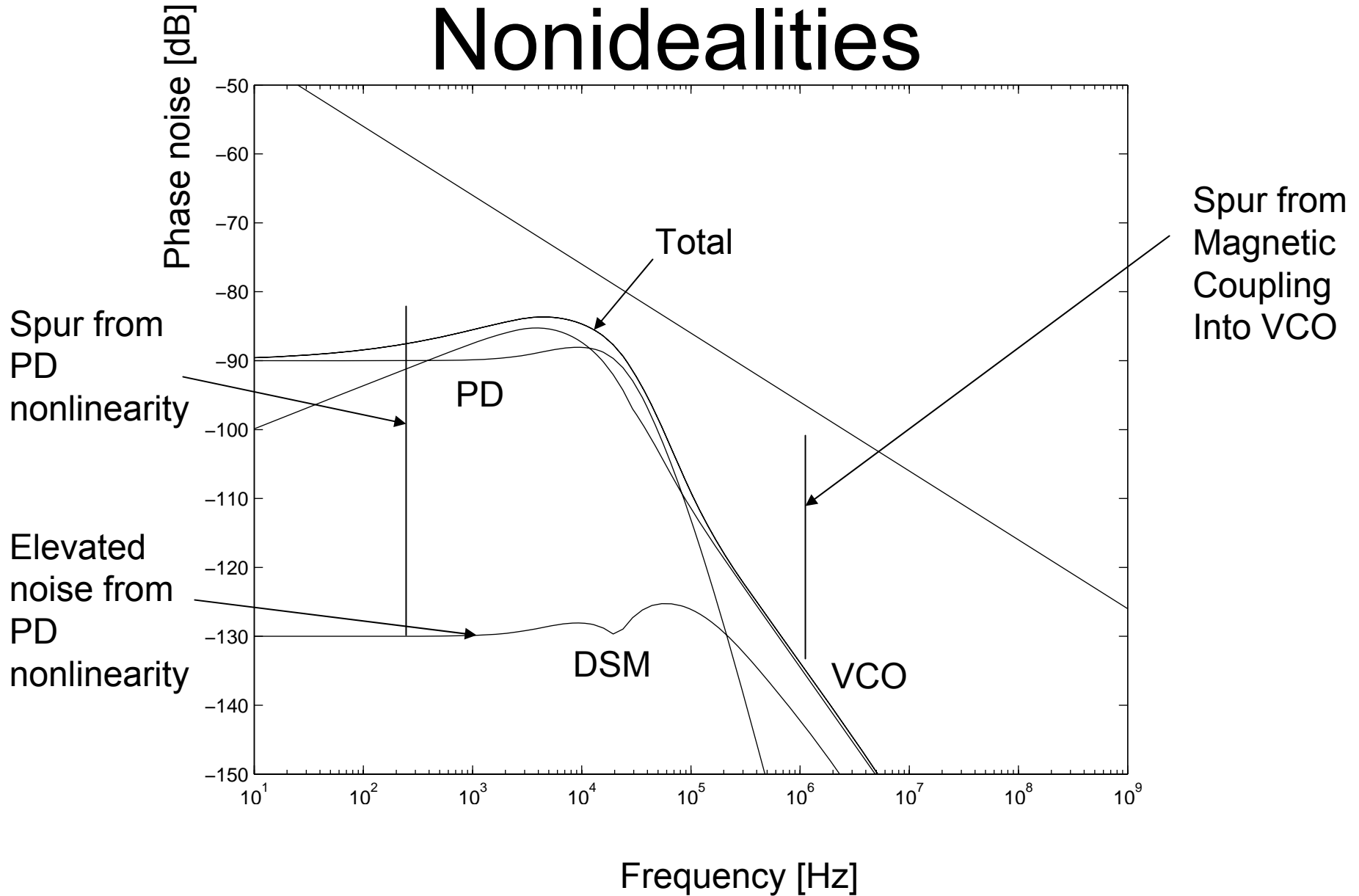
# Bandwidth too low, VCO dominates



# Optimum bandwidth – PD and VCO are even contributors, DSM noise is hidden!



# Nonidealities

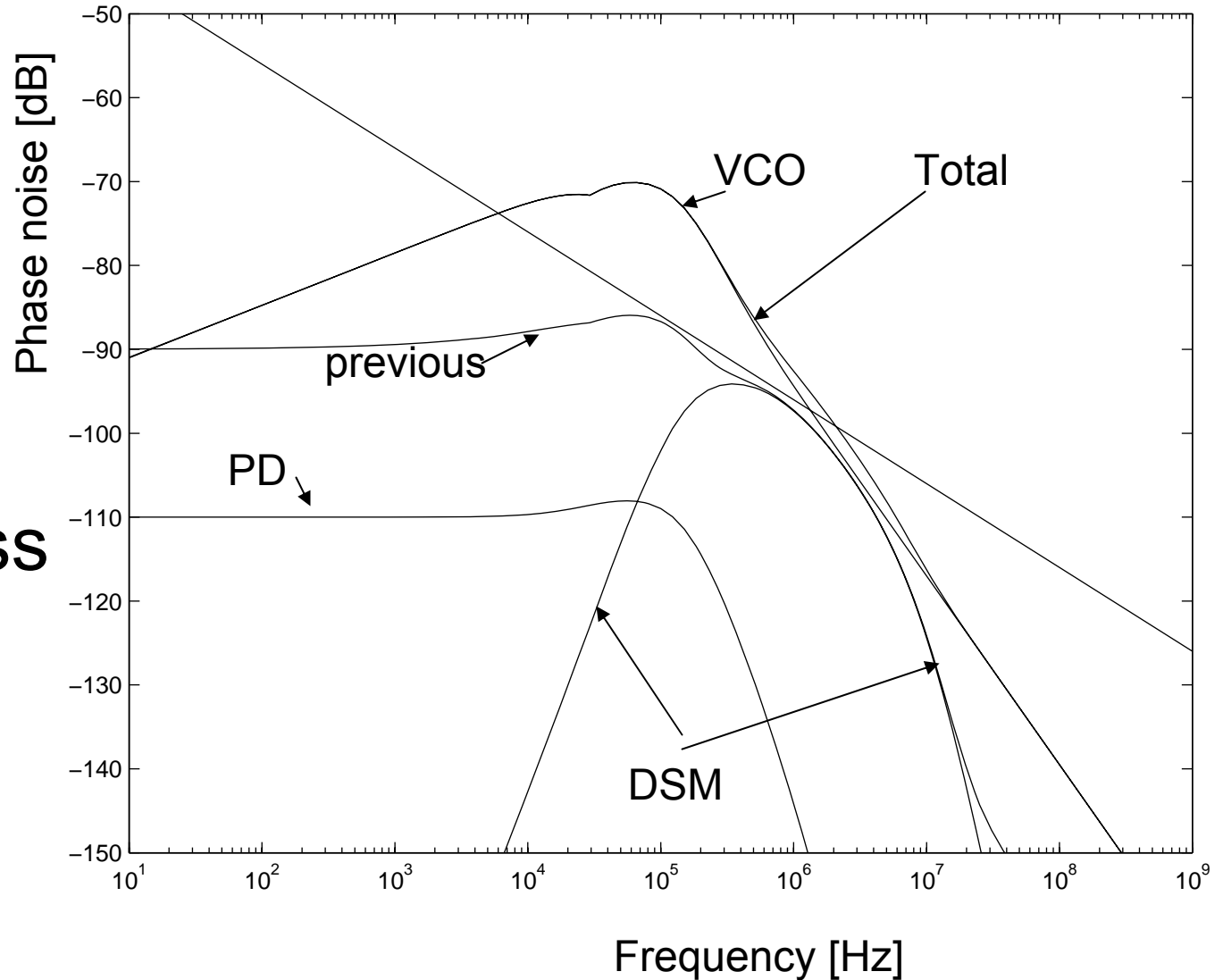


# Example design 2

- bad VCO with high bandwidth – challenging situation
- Try without phase error cancellation first
- See effectiveness of phase error cancellation

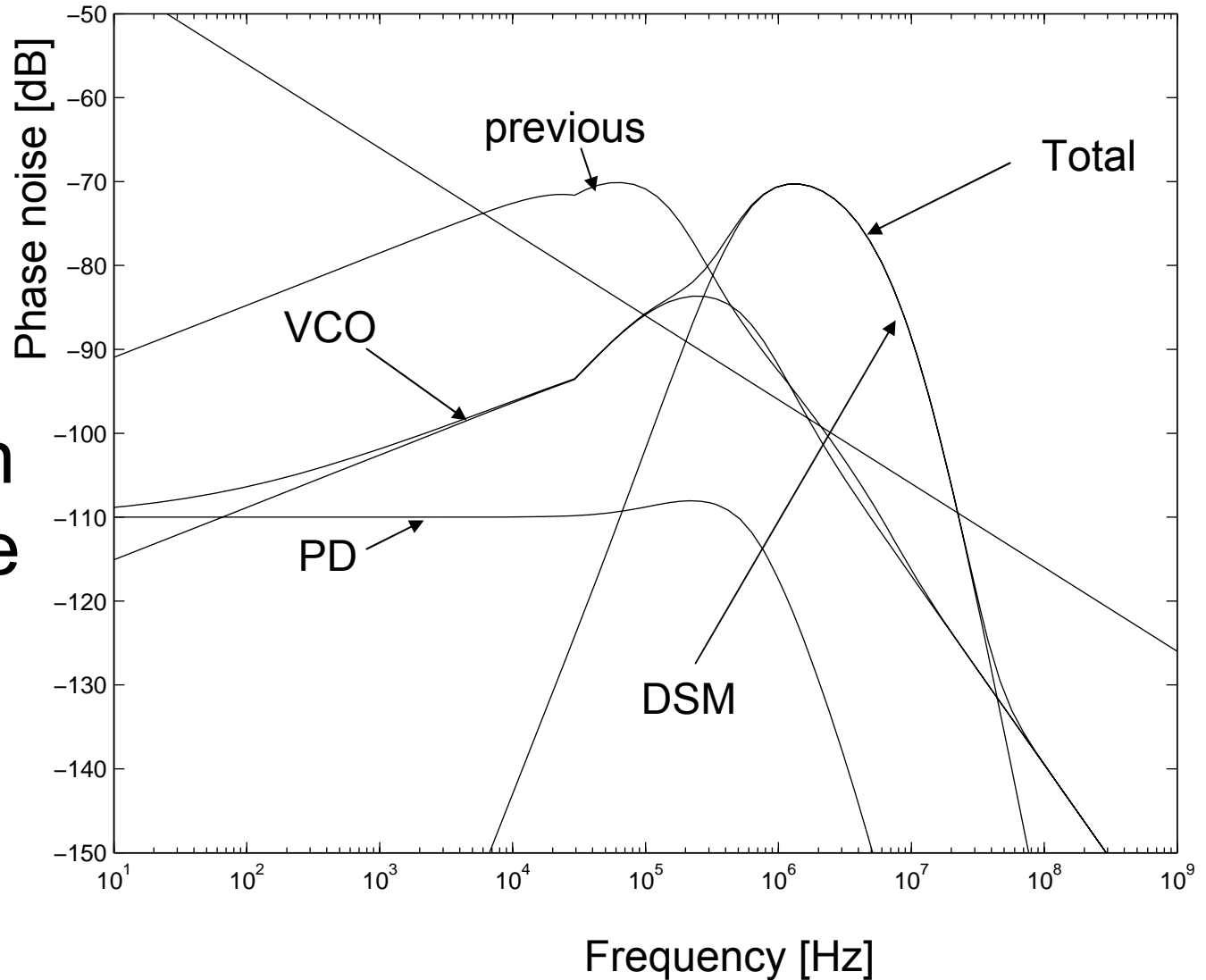
# Design Example 2

Bad VCO  
Need to  
increase  
bandwidth  
to suppress  
noise

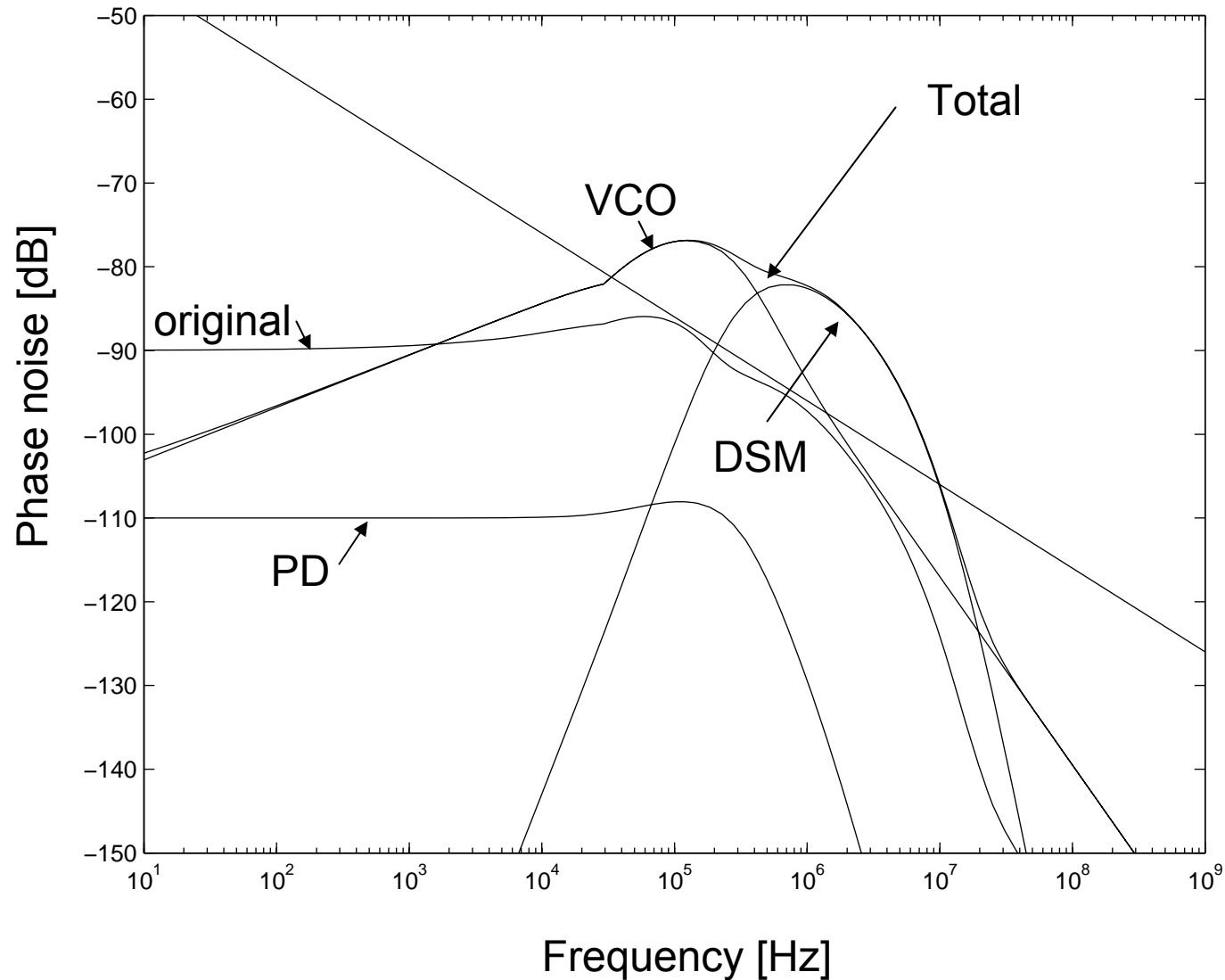


# Design Example 2

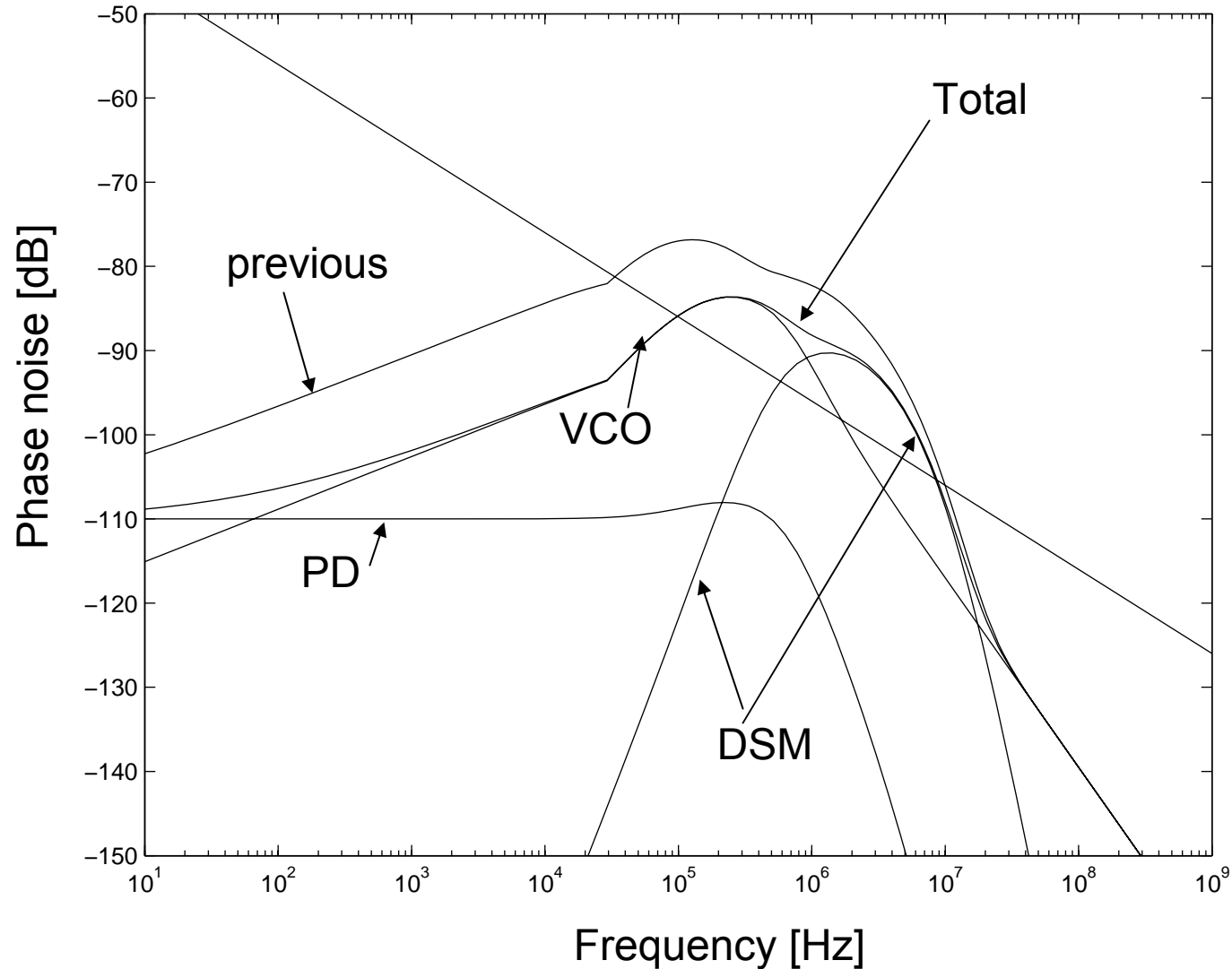
- Opening bandwidth brings enormous increase in DSM noise



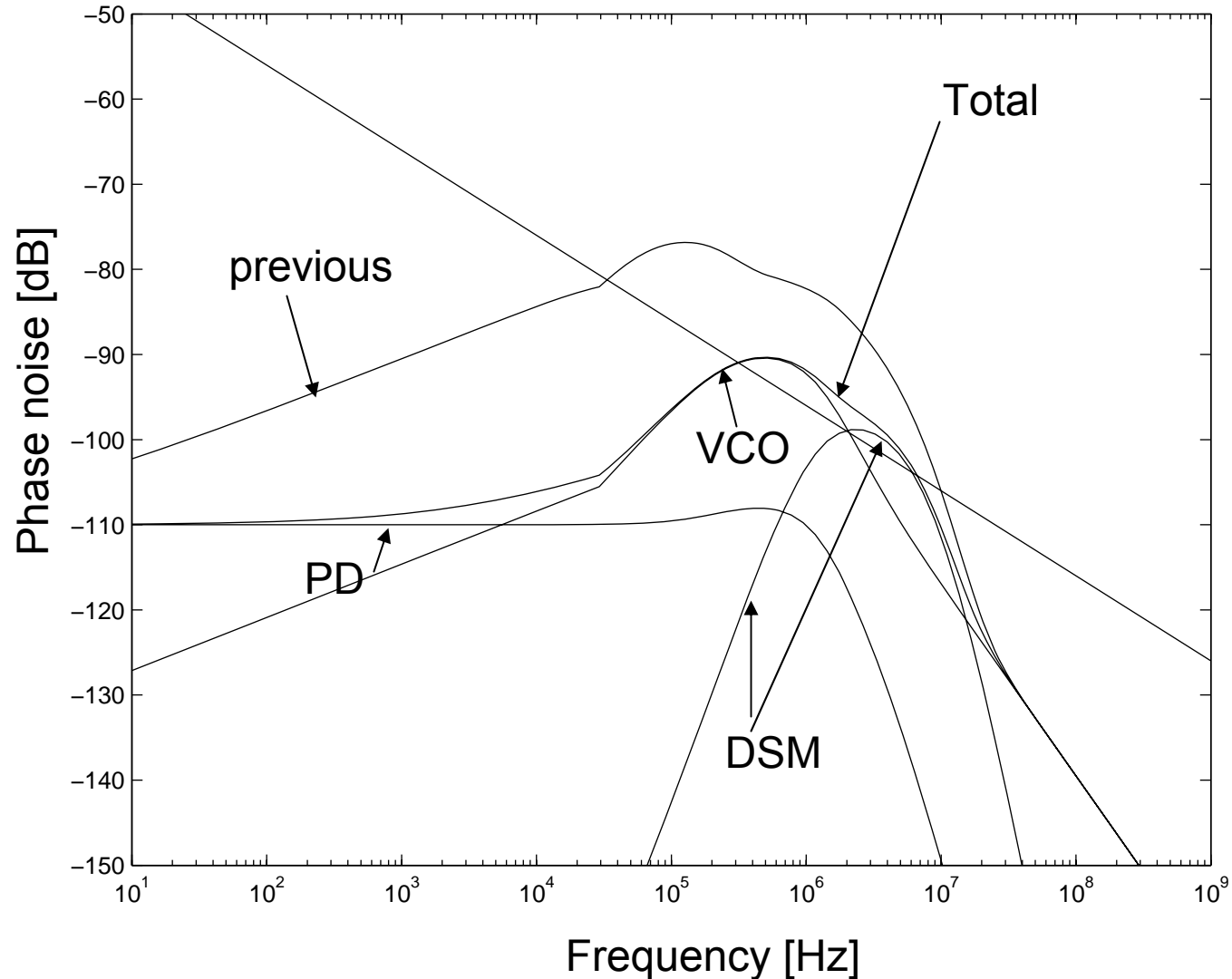
# Example 2: Optimum bandwidth



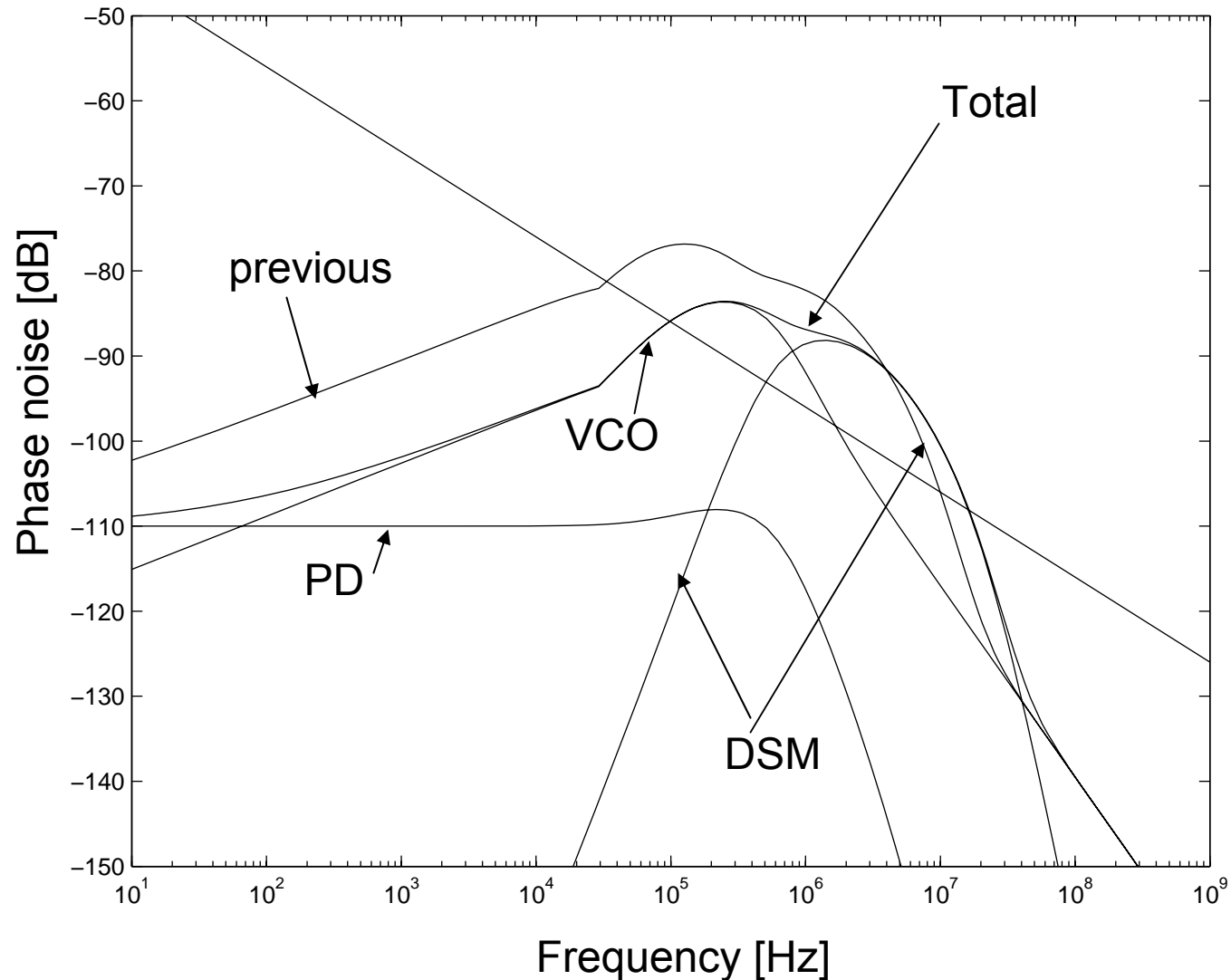
# A 20dB reduction in DSM noise with phase error cancellation helps a lot



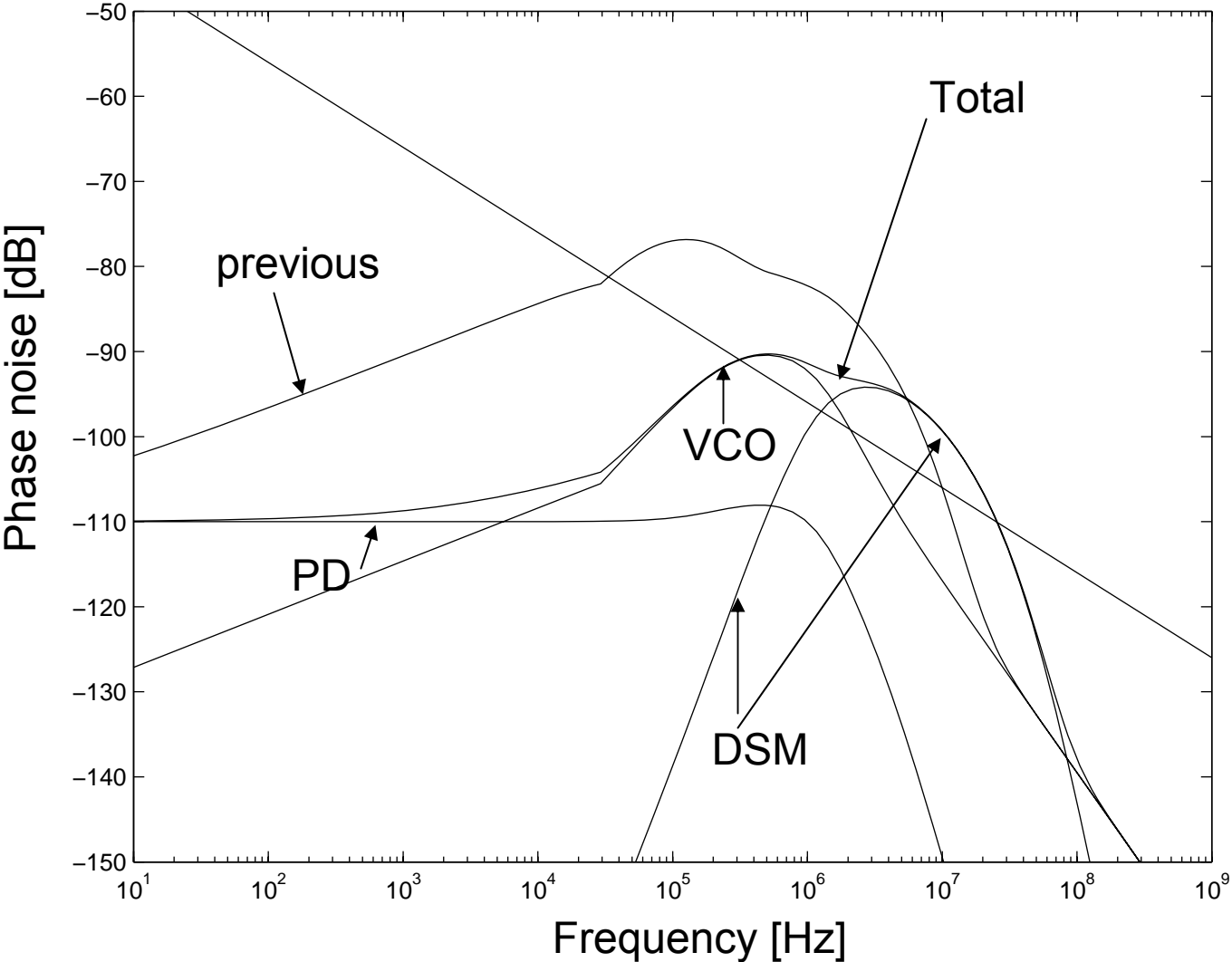
# A 40dB reduction in DSM noise with phase error cancellation helps even more



If I can increase my reference frequency, I can take care of the noise via filtering (here 2x increase)



If I can increase my reference frequency, I can take care of the noise via filtering (here 4x increase)



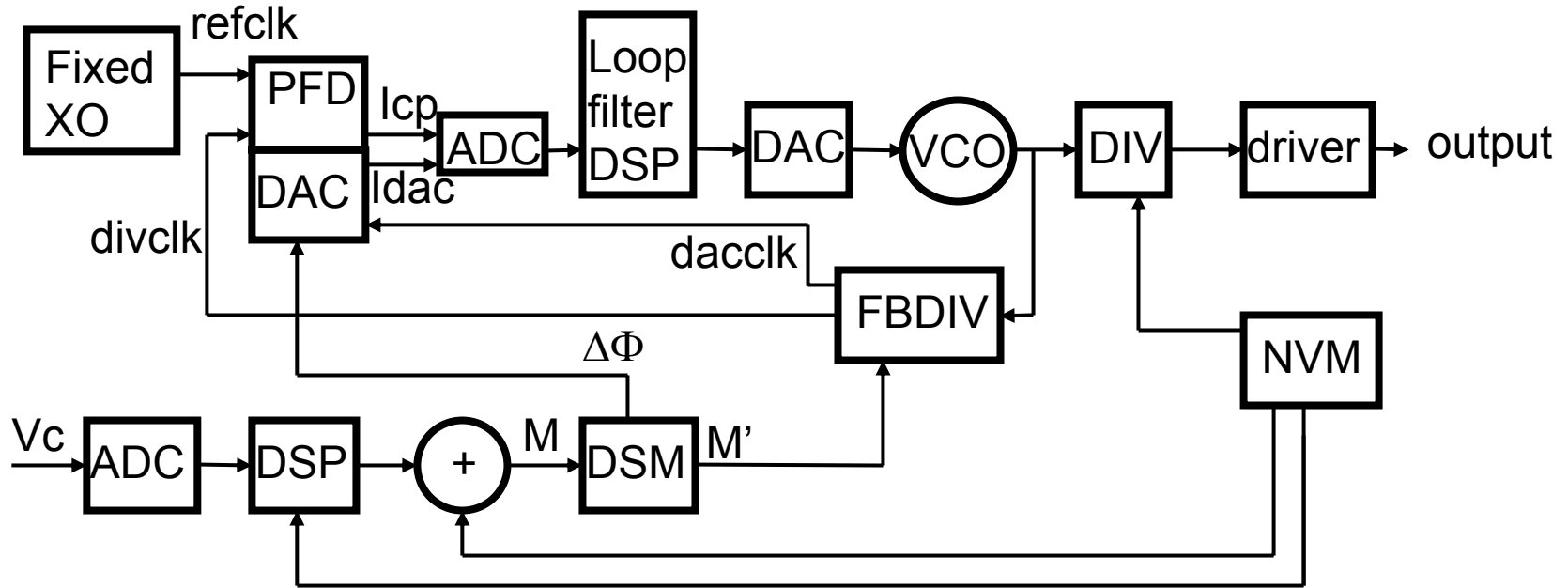
# Classic crystal oscillator issues

- Traditionally, crystals have to be cut and trimmed to achieve a specific resonance frequency.
- Large lead times, qualification cycles
- Limited frequency range for fundamental mode Xtals – 4 to 60MHz
- High manufacturing cost for high frequency Xtals such as inverted mesa crystals
- High temperature coefficient for SAW resonators

# A programmable crystal oscillator

- A fixed frequency crystal with loose accuracy specs can be stocked and qualified
- A fractional N PLL can create any frequency needed to high precision
- Multiplier stored in OTP
- Can also emulate VCXO operation

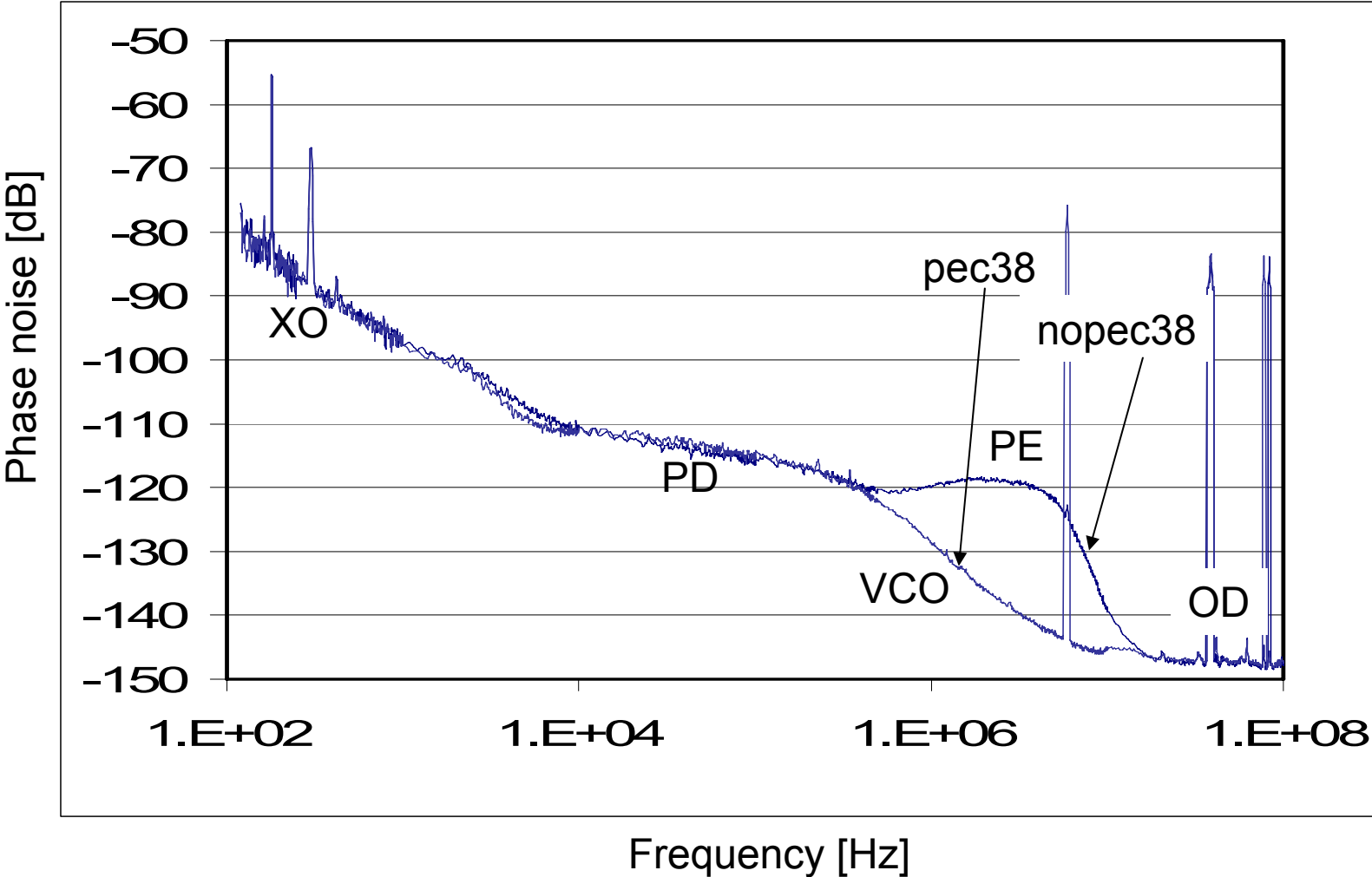
# Chip architecture



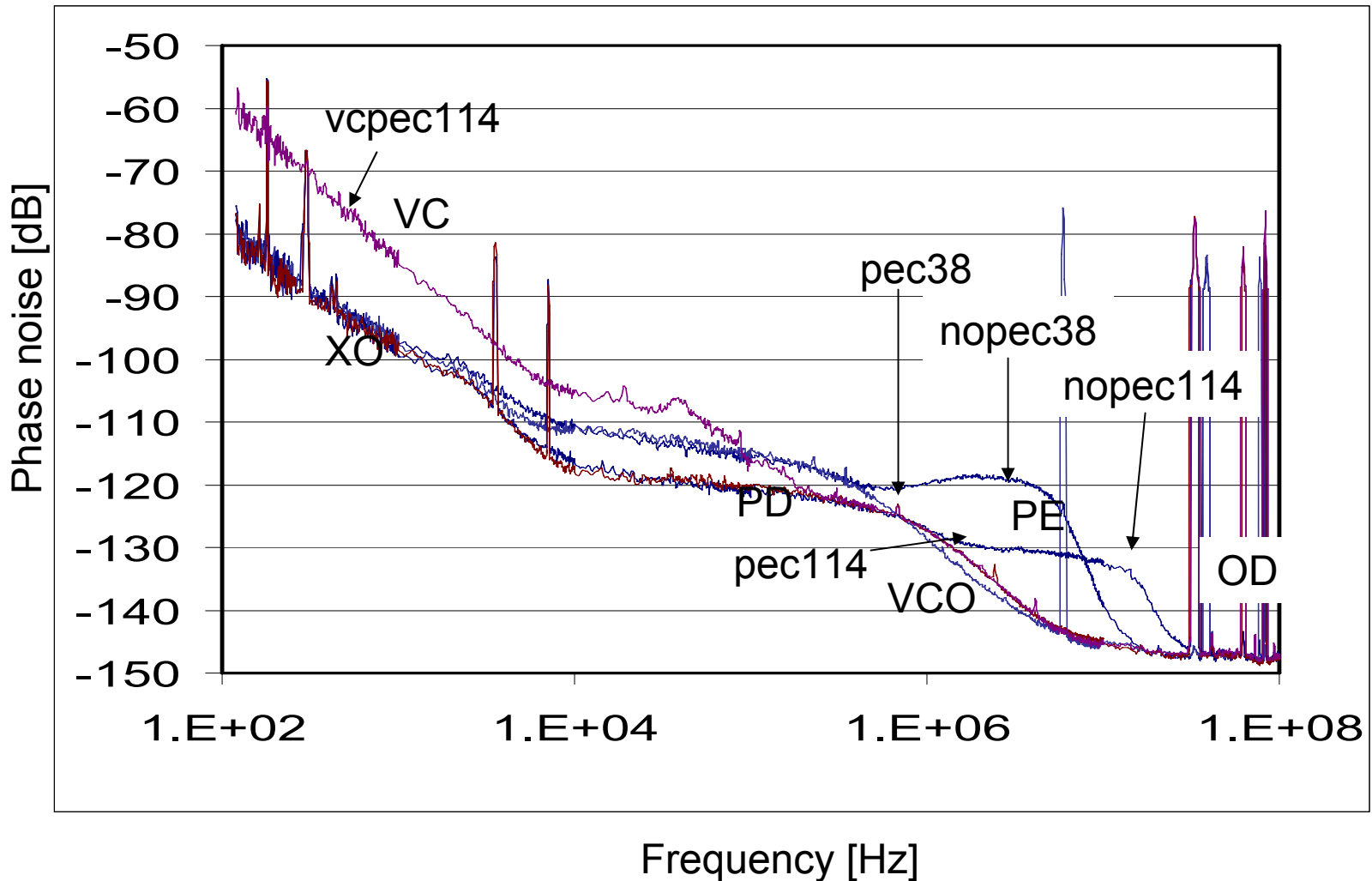
# Experimental Results

- Phase noise vs  $f_{xo}$
- Phase noise vs PEC
- Phase noise from VC operation
- Spurs

Results 1: phase noise performance for different modes:  
SSB noise [dBc/rtHz] vs. frequency [Hz], f<sub>out</sub>=666MHz



Results 2: phase noise performance for different modes:  
SSB noise [dBc/rtHz] vs. frequency [Hz],  $f_{out}=666\text{MHz}$

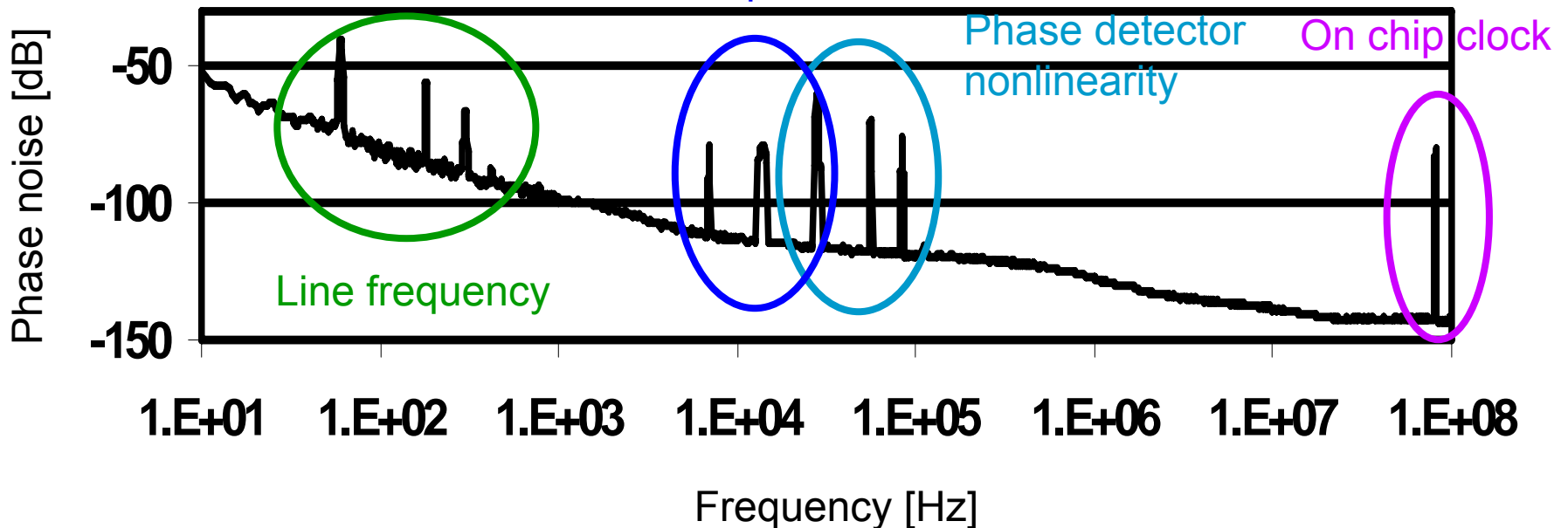


# Results: spurious performance for $M=40+1/1024$

SSB phase noise [dBc/rtHz] vs. frequency [Hz],

$f_{out}=571.44\text{MHz}$

Mixing between  
XO and output

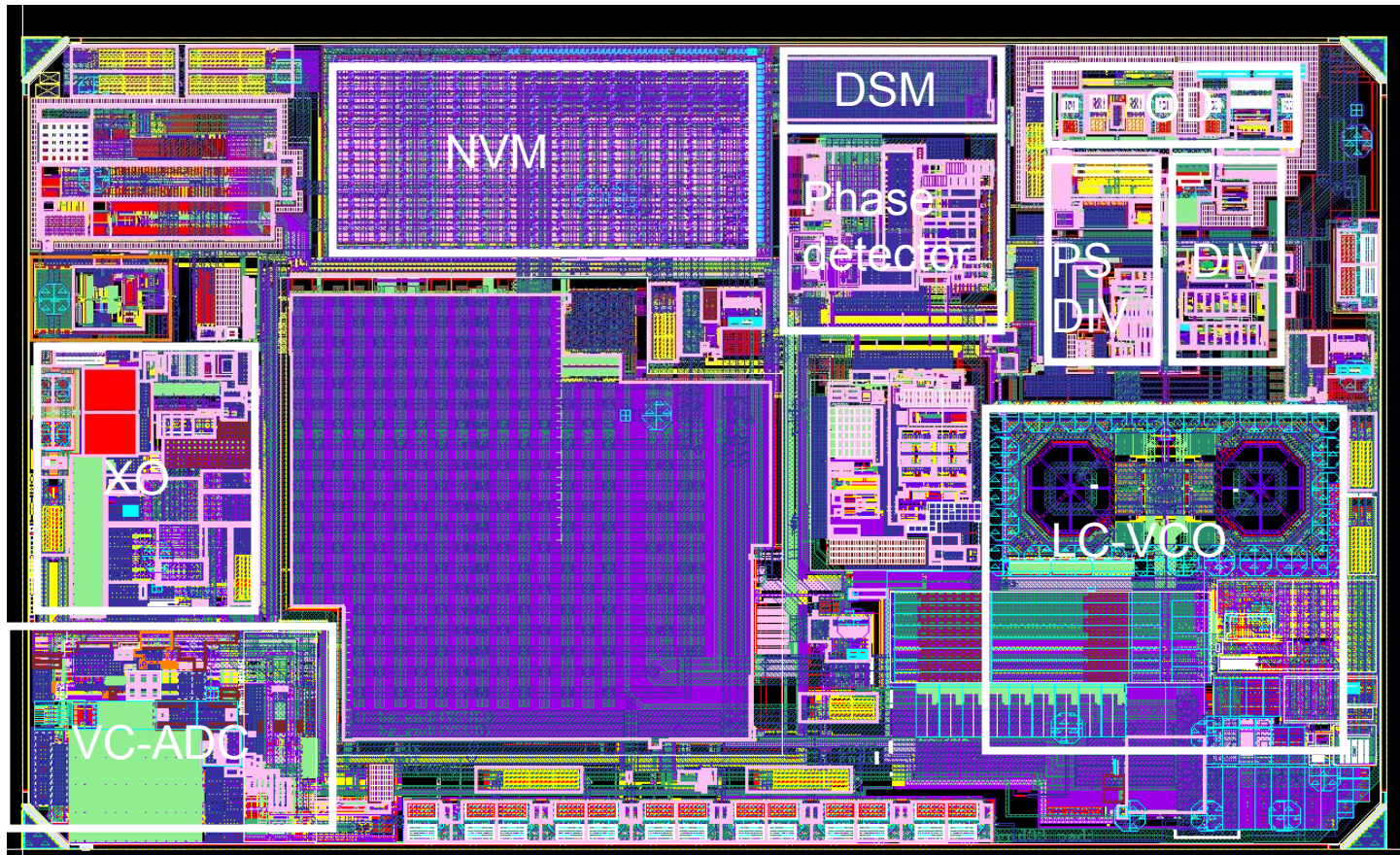


# Results summary

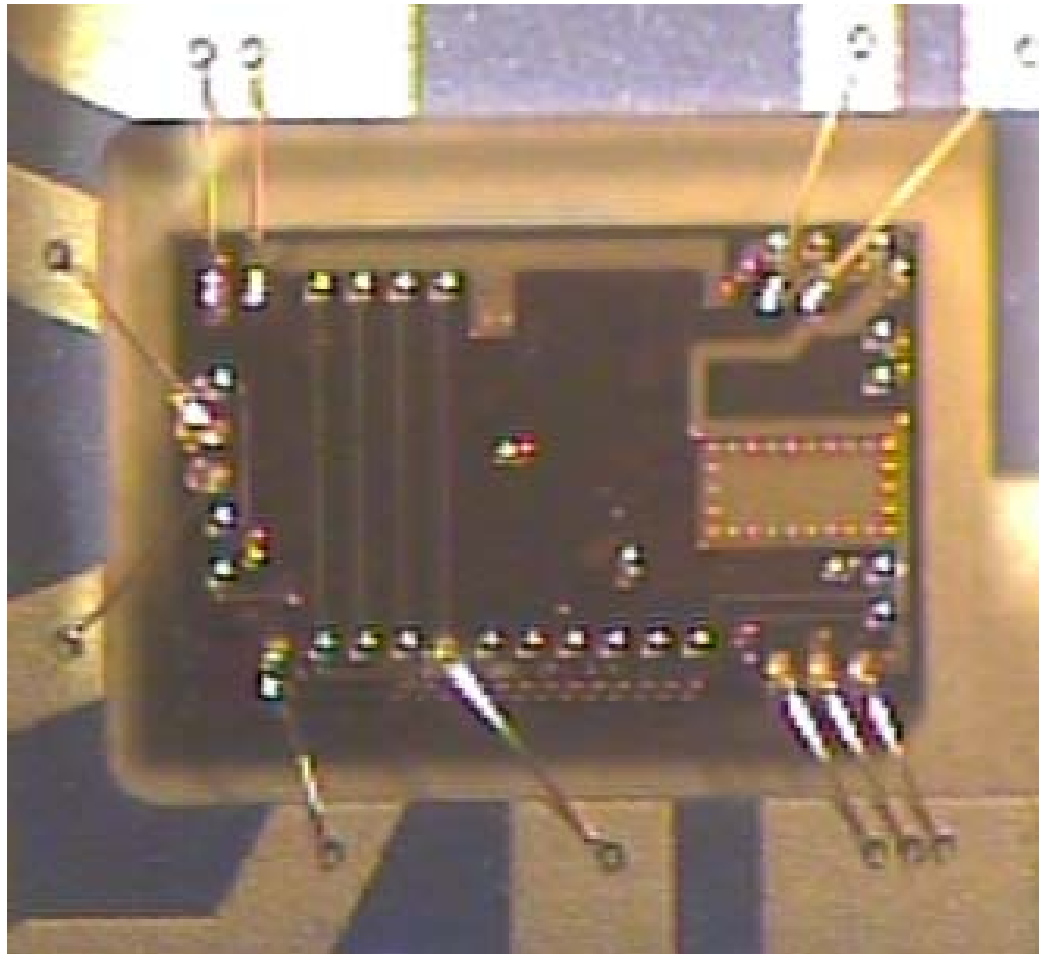
|               |                  |
|---------------|------------------|
| Technology    | 130nm CMOS       |
| Die area      | 4mm <sup>2</sup> |
| OC48 Jitter   | 0.3ps rms        |
| OC192 Jitter  | 0.3ps rms        |
| Core current  | 70mA             |
| Total current | 100mA            |
| Supply        | 1.8V to 3.3V     |
| Gain from VC  | 45 to 180 ppm/V  |

- Wideband fractional N PLL with -124dBc noise floor in-band – best reported
- Spurs in worst case remain below 60dBc

# Layout plot: die size 4mm<sup>2</sup>



# Die photo in package



# Conclusion

- Key parameters in the design of a fractional N PLL are VCO performance and update rate
- When VCO performance is poor or update rate is low the design is challenging
- Phase error cancellation can help in such a situation
- Fractional loops can achieve low enough jitter even for demanding applications like optical communication

# Some useful references

1. Bram de Muer, Michiel Steyaert, CMOS fractional N synthesizers, Kluwer, 2003
2. M H Perrott, techniques for high data rate modulation and low power operation of Fractional N Frequency Synthesizers., Ph D Thesis, MIT 1997
3. Riley, Copeland, Kwasniewski, Delta Sigma Modulation in Fractional N frequency synthesis, IEEE-JSSC, vol 28, no 5, pp.553-559
4. S. Parmati, L. Jansson, I. Galton, A wideband 2.4-GHz delta-sigma fractional-NPLL with 1-Mb/s in-loop modulation IEEE Journal of [Solid-State Circuits](#), Volume 39, Issue 1, Jan. 2004, pp:49 - 62
5. Staszewski et al, All-Digital PLL and Transmitter for Mobile Phones, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. 12, DECEMBER 2005, pp 2469-2482
6. Michael H. Perrott, Theodore L. Tewksbury III, Charles G. Sodini, A 27-mW CMOS Fractional-Synthesizer Using Digital Compensation for 2.5-Mb/s GFSK Modulation, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 32, NO. 12, DECEMBER 1997,pp 2048-2060
7. Enrico Temporiti, Guido Albasini, Ivan Bietti, Rinaldo Castello, Matteo Colombo A 700-kHz Bandwidth delta sigma Fractional Synthesizer With Spurs Compensation and Linearization Techniques for WCDMA Applications IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 39, NO. 9, SEPTEMBER 2004, pp 1446-1454
8. Swaminathan, A.; Wang, K. J.; Galton, I.; A Wide-Bandwidth 2.4 GHz ISM Band Fractional-N PLL With Adaptive Phase Noise Cancellation IEEE Journal of [Solid-State Circuits](#), Volume 42, [Issue 12](#), Dec. 2007 Page(s):2639 - 2650
9. ISSCC 2008 ,19.1 C-M. Hsu, M. Straayer, M. Perrott, A Low-Noise Wide-BW 3.6GHz Digital  $\Delta\Sigma$  Fractional-N Frequency Synthesizer with a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation
10. ISSCC 2008 19.2 K. Wang, A. Swaminathan, I. Galton, Spurious-Tone Suppression Techniques Applied to a Wide-Bandwidth 2.4GHzFractional-N PLL
11. ISSCC 2008 19.3 C. Weltin-Wu, E. Temporiti, D. Baldi, F. Svelt1, A 3GHz Fractional-N All-Digital PLL with Precise Time-to-Digital ConverterCalibration and Mismatch Correction
12. ISSCC 2008 19.4 X. Yu, Y. Sun, L. Zhang, W. Rhee, Z. Wang, A 1GHz Fractional-N PLL Clock Generator with Low-OSR  $\Delta\Sigma$  Modulation andFIR-Embedded Noise Filtering