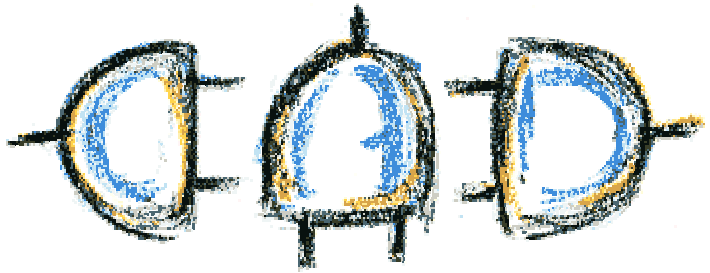
A set of RT- and gate-level benchmarks



CAD Group

Fulvio Corno
Maurizio Rebaudengo
Matteo Sonza Reorda

Politecnico di Torino

Dip. Automatica e Informatica

`http://www.cad.polito.it/`

ITC'99 Benchmark meeting at ITC'98

Motivation

- **Industrial benchmarks are hard to find**
- **Most real designs have weird structures:**
  - **many clocks**
  - **embedded memories**
  - **mix of synthesized & hand-designed parts**
- **Difficult to evaluate research tools on realistic examples.**

Bench characteristics

- **Both RT-level and gate-level descriptions available**
- **“Pure” Synchronous behavior**
- **Global reset signal**
- **Single clock, single phase**
- **No memories**
- **Wide range of sizes and complexities.**

RT-level VHDL

- **Cleanly synthesizable (Synopsys)**
- **One or many processes**
- **No concurrent statements outside processes.**

Gate-level EDIF

- **Ad-hoc library with elementary gates**
- **Flattened**
- **Fault lists available (single stuck-at)**
- **Netlist reader library available.**

Development

- **Gathered a set of VHDL files**
  - **FTP sites**
  - **students' class works**
  - **combination of smaller descriptions**
- **Uniformed VHDL style**
  - **add reset, join clocks, …**
  - **original behavior not preserved**
- **Synthesized Netlists.**

Circuit characteristics

	gates	#FF	PI	PO	#VHDL lines	#process	Notes
b01	45	5	2+2	2	110	1	fsm
b02	25	4	1+2	1	70	1	isbcd
b03	150	30	4+2	4	141	1	arbiter
b04	480	66	11+2	8	80	1	minmax
b05	608	34	1+2	36	319	3	elab_ram
b06	66	9	2+2	6	128	1	int_handler
b07	382	51	1+2	8	92	1	line
b08	168	21	9+2	4	89	1	find_incl
b09	131	28	1+2	1	103	1	ser_par
b10	172	17	11+2	6	167	1	voting system
b11	366	30	7+2	6	110	1	scramble
b12	1,000	121	5+2	6	567	4	simon game
b13	309	53	10+2	10	296	5	meteo
b14	3461	247	32+2	54	518	1	viper
b15	6931	447	35+2	70	648	3	80386
b16		N		1	68	N	hard_to_init
b17	21,191	1407	36+2	97	135	6	3*b15
b18	49,293	3308	35+2	30	94	1	2*b14+2*b17
b19	98,726	6618	45+2	40	65	2	2*b18
b20	7,741	494	32+2	22	1,040	3	b14+b14’
b21	7,931	494	32+2	22	63	1	b14+b14
b22	12,128	709	32+2	22	1,547	4	14+b14’+b14”

Download

- http://www.cad.polito.it/tools/#bench
- **POLI-RT: VHDL RT-level benchmarks**
- **POLI-GATE: Gate-level version synthesized with Synopsys VHDL Compiler**
- **POLI-FAULT: Fault lists generated with Sunrise's faultsim**
- **POLI-INP: Test patterns generated with RAGE [ITC'96]**