Comprehensive Standard Cell Characterization Considering Random Line-Edge Roughness Lithography Variation

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ABSTRACT

As the transistors are scaled down, undesirable performance mismatch in identically designed transistors increases and hence causes greater impact on circuit performance and yield. Since Line-End Roughness (LER) does not decrease as the device shrinks and has been reported to be in the order of several nanometers, it has evolved as a critical problem in the sub-45nm devices and may lead to serious device parameter fluctuations and performance degradation for the future VLSI circuit. In this paper, we present a new cell characterization methodology which uses the non-rectangular gate print-images generated by lithography and etch simulations with the random LER variation to estimate the device performance of a sub-45nm design. We systematically analyze the random LER by considering the impact on circuit performance due to LER variation and suggest the maximum tolerance of LER to minimize the performance degradation. We observed that the driving current is highly affected by LER as the gate length becomes thinner. We performed lithography simulations using 45nm process window to examine the LER impact of the state-of-the-art industrial devices. Results show that the rms value of LER is as much as 10% from its nominal line edge, and the saturation current can vary by as much as 10% in our 2-input NAND cell.

1. INTRODUCTION

The significance and complexity of process variation is increasing in a circumstance of increasing challenges from manufacturing limitations. Among multiple variation issues, lithographic printability variation is one of the most fundamental challenges because it directly impacts yield and performance. In particular, the random lithography variation is caused by random uncertainties in the fabrication process such as Line-Edge Roughness (LER), the random defects due to missing and/or extra material etc. At the same time, many non-lithographic sources of variation such as dopant variation [1, 2] and gate dielectric thickness (T_{ox}) variation [3, 4] are also resulted in aggressive scaling. Among them, LER has regarded as a small fraction of the statistical variability in the past since the critical dimensions (CD) of MOSFETs were orders of magnitude larger than the roughness. However, as the aggressive scaling continues into the nanometer regime, LER does not scale accordingly and becomes an increasingly larger fraction of the gate length. For channel lengths above 30 nm, the random dopants are the dominant source of fluctuations, but below this channel length, the LER takes over and becomes the dominant fluctuation source.

Since LER is mainly caused by erosion of polymer aggregates at the edge of photo-resist (PR) during development and fully depends on some complex chemical formulae, it is so difficult to generate the LER image in print-images of layouts, and in our knowledge no commercial lithography simulation tools can generate print-images caused by LER. Even though LER is a kind of random variation, it is undesirable and has to be analyzed because it highly degrades the device performance. LER is on the order of several nanometers [5, 6], and can be one of the performance limiting components for 45nm and below technologies.

In this paper, we propose a comprehensive standard cell characterization method that accounts for random LER variation. Specific contributions in this paper are the following:

- We derive a new analytical LER variation model, which can generically handle any rms amplitude and frequency of LER and integrate the LER variation into our print-image and layout extraction flow so that it can characterize the random LER mismatch variation.
- The accuracy of our LER model is validated from the physics based TCAD simulation introducing the strain silicon used in the 45nm node standard cell.
- We present a method to account the LER variation in both statistical and deterministic analysis flows.

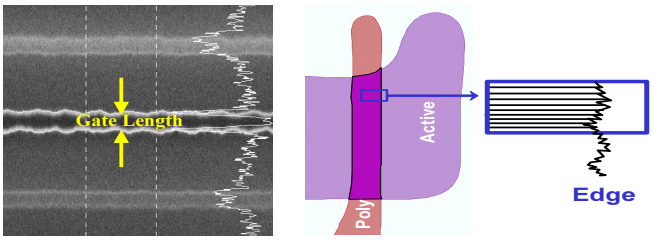
The rest of the paper is organized as follows: Section 2 describes the comprehensive characterization flow. This section presents effective gate length extraction method and sensitivity characterization method. Experimental results are discussed in Section 3, followed by conclusions in Section 4.

2. FORMULATION AND SIMULATION

2.1 Random LER Modeling

LER, one of the dominant random variations, is caused by the interaction of light and thermal bombardment with the molecular nature of photoresist materials in the acid generation, the acid diffusion and development process in chemically amplified resists (CAR). As shown in Figure 1(a), the severe CD variation is evolved at the line edge, despite patterning an isolated straight line structure. To address the LER effect of the wafer printed image as shown in Figure 1(b), we first formulate the LER and apply to our printed image. LER is a random fluctuation in the gate length along the complete width of the device and has influence on both edges of the gate.

For a set of print-image, we slice the gate image into the small segmentations less than the longitudinal frequency of LER as shown in Figure 1(b). At the line edge, LER roughly shows a tendency of a sinusoidal distribution having a frequency (f_y) which depends on the nature of photo-resist material and the contrast of aerial image, and can be determined from the experimental SEM image. Thus, the line



(a) SEM of gate LER [6] (b) LER implementation

Figure 1: Random LER lithography variation.

edge can be first assumed as the sinusoidal equation like as Eq. 1 and Eq. 2 as shown in Figure 2(b).

$$\sigma_l = \sigma_r = \frac{L_{max}}{\sqrt{2}} \tag{1}$$

where, L_{max} is the maximum amplitude of the sinusoidal edge. For each segmented gate, the increment of the gate length due to the left LER (L_{l_seg}) and the right LER (L_{r_seg}) can be shown as below:

$$\begin{aligned} \Delta L_{l\_seg} &= L_{max} \cdot [\sin(y_l \cdot f_y)] \\ \Delta L_{r\_seg} &= L_{max} \cdot [\sin(y_r \cdot f_y)] \end{aligned} \tag{2}$$

where, y_l and y_r are the left and the right position of the sliced segmentation along the width direction and f_y is the longitudinal spatial frequency of LER at the line edge toward the gate width direction, respectively. The spacial frequency of LER is typically lower than 20 to 30 cycles/micron [5] and we refer the frequency data from the SEM images.

LER is applied with another random number for a small segmentation simultaneously considering the high frequency noise factor ρ_2 as shown in Figure 2(c), then the gate length increment of the chopped rectangle at the left edge (that of the right edge (ΔL_{r_seg}) has the same formula) is changed as following:

$$\Delta L_{l\_seg} = L_{max} \cdot \frac{1}{2} \cdot [\sin(y \cdot f_y) + \rho_2] \tag{3}$$

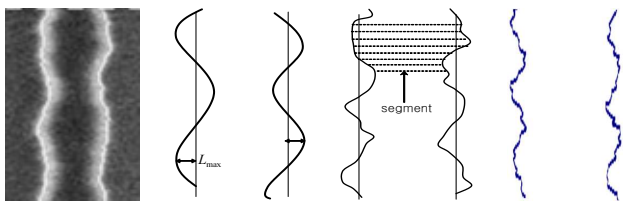
To implement the LER for a chopped rectangle, we formulate the new gate length taking both lithography proximity (systematic) and LER (random) into consideration as following:

$$L_{pi\_seg} = L_{sys\_seg} + \Delta L_{l\_seg} + \Delta L_{r\_seg} \tag{4}$$

where, L_{sys_seg} is the gate length of a segmented rectangle due to the systematic variation. Figure 2(d) shows the result of our implementation into the print-image.

2.2 Random LER-Aware Extraction

In this step, we extract the effective gate length for post lithography print-images using a gate segmentation technique. Lithography variations result in a non-rectangular shapes for both poly and diffusion layers. For a standard cell, area of the diffusion region defines the drive-strength of the cell. Diffusion rounding due to lithography variations is a critical variational source. However, the print-image of active diffusion layer has a non-trivial impact on the non-rectangular gate because the contours in this layer show rounding patterns connecting to power rails which causes much variation of the effective gate length and width [8].



(a) SEM (b) Sin. edge (c) Sin. edge with noise (d) Implementation

Figure 2: Implementation of random LER.

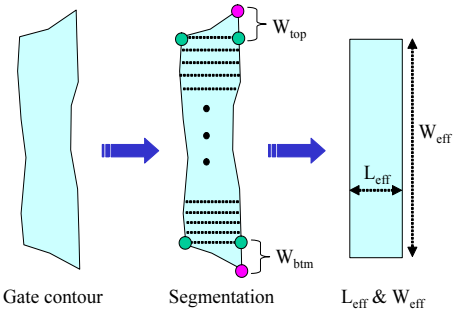


Figure 3: Gate segmentation for non-rectangular gate

The proposed algorithm is illustrated in Algorithm 1 for random LER-aware extraction. To extract the print-image, we first construct four lookup tables for on-current, I_{on} and off-current, I_{off} of the NMOS and PMOS devices using commercial simulation tool [7]. We then find the 4 intersection points using poly and diffusion print-images. These points represent the gate/channel region. From these points, we identify the effective gate width (W_{eff}) and rounded diffusion area as shown in Figure 3.

Next, we segment the gate region by a set of equal width rectangular polygons. Each segment then has a width, W_{seg}. The current for each segment, I_{seg} is computed using the nominal current from the rectangular device. The equivalent or total current for the gate region is computed by summing all these segment currents. Prior to obtaining L_{eff} for each device, we update the equivalent current with that due to the rounded diffusion area. We use the formulation in [8]

Algorithm 1 Effective gate length

Require:A set of lookup table, gate print-images I
Table $gate \leftarrow poly \cap active$
$nmos \leftarrow gate \cap nwell$
$pmos \leftarrow gate - nmos$
$f_y \leftarrow$ spatial frequency of LER for I
σ_{ler} from Eq. 1
for each *cell* $C \in I$ **do**
  for each *nmos* $N \in C$ **do**
    Find intersection points between poly & active
    Set W_{eff} & diffusion rounding
    $I_{sum} \leftarrow 0$
    for each *slice* $S \in N$ **do**
      ρ_1 & $\rho_2 \leftarrow -1 \leq rand() \leq 1$
      L_{seg} from Eq. 3 and Eq. 4
      $I_{sum} += I_{seg}$; I_{seg} from I_{on} & I_{off} lookup table
    end for
    Update I_{sum} from Eq. 5 and 6
    L_{eff} from I_{sum} lookup table
  end for
  for each *pmos* $P \in C$ **do**
    Same sequence as *nmos*
  end for
end for

to compute the equivalent currents due to diffusion rounding. The device currents, I_{on} and I_{off} are updated using following formulations:

$$I_{on} = I_{on\_nom} \times \left(1 + \frac{0.5 * (W_{top} + W_{btm})}{W_{nom}}\right) \quad (5)$$

$$I_{off} = I_{off\_nom} \times C \times exp\left(\frac{L_{nom}}{L'}\right) \quad (6)$$

where I_{on_nom}, I_{off_nom}, L_{nom}, and W_{nom} are the on current, the off current, the gate length, and the gate width of the nominal rectangular device, respectively. W_{top} and W_{btm} is the top height and the bottom height of the rounded diffusion area respectively as shown in Figure 3. C is a fitting parameter and L' is the effective channel length at the edge of rounded diffusion. From the total I_{on} and I_{off} current, L_{eff}s are computed using the lookup table.

2.3 TCAD Simulation and Validation

To verify the proposed LER model on device performance in terms of the driving current, we employ a TCAD simulator [9] with the strained silicon in which Tensile strain is introduced in the NMOS channels by using a post-salicide silicon-nitride capping layer. To save a simulation time and memory usage, we use a quasi-3D simulation in which the LER-implemented print-image (Figure 2(d)) is considered in the TCAD simulation, then a set of 2D simulation is carried out. Some of the most important parameters of the device are: the range of Gate lengthes caused by LER is from 25nm up to 60nm (the nominal gate length is 40nm), oxide thickness is 1.2 nm and capping layer thickness is 75 nm.

We compare the result in term of the amount of LER between the rigorous TCAD simulation and the circuit simulation used for LER characterization. To compensate the internal difference between TCAD simulator and circuit simulator, we normalize the current value to the current of a device without LER. Figure 4 shows the comparison of the saturation current to validate the proposed LER model and represents the great agreement. The maximum error between TCAD simulation and the proposed result is as much as 2.2%, and the average error is about 0.6% when comparing the driving current due to LER.

2.4 LER-Aware Cell Characterization

Timing analysis requires that the standard library cells are pre-characterized for delay and slew. These are stored in a two-dimensional table indexed by input slew and output load. Each cell is characterized using a circuit simulator (e.g., SPICE simulator).

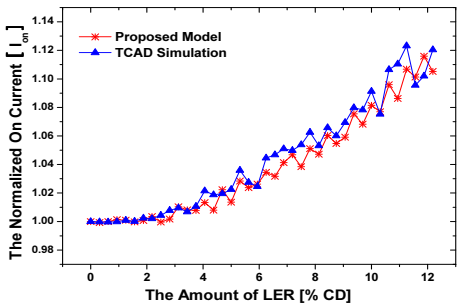


Figure 4: Comparison with TCAD results

Let L_{nom} be the original drawn dimension of the gate-length for each device in a cell. As a result of the non-rectangular gate extraction, let the new gate-length be, L_{pi}. Then, this L_{pi} has a systematic component, L_{sys} and a component due to the random LER variations, ΔL_{ler}. This can be represented as:

$$L_{pi} = L_{sys} + \Delta L_{ler} \quad (7)$$

In order to characterize for the effect of systematic lithography variations, the standard characterization procedure is used. The characterization is carried out by annotating L_{sys} for each device in the cell. The L_{sys} is a deterministic value and a standard delay / leakage characterization by setting each device to the new effective gate-length/width due to systematic variations is performed. In order to characterize for random LER variations, the standard cell is characterized for sensitivity to ΔL_{ler}. During sensitivity characterization, the variations in each device need to be accounted. Let p be number of devices in a cell. Let the random LER variation for each device k be ΔL_k. Since these random variations is much smaller than the nominal L_{pi}, performance characteristics of the cells are almost linear functions within the range of the variations ΔL_i.

For delay characterization, the delay of a timing arc, D can be represented as follows:

$$D = D_0 + \sum_{k=1}^{p} d_k \Delta L_k \quad (8)$$

where D_0 is the nominal delay value and is characterized by extracting L_{eff}, L_{sys} due to printed contours in poly and diffusion layers. Each device LER, ΔL_k is modeled as a distribution $N(0, \sigma)$. The quantities d_k are direct sensitivities of cell delay with respect to the LER variations, ΔL_k.

Thus, each cell in the library is characterized for a nominal delay, D_0 by setting all devices to their corresponding contour-based effective gate lengths and zero LER. Additionally, the cells are characterized for sensitivity to LER on each device by setting a separate random variable, ΔL_k and the corresponding delay variation is computed. Assuming delay variation due to each device is statistically independent, the cell's delay sensitivity can then be obtained using following relation:

$$d_{eq} = \sqrt{\sum_i d_i^2} \quad (9)$$

3. EXPERIMENTAL RESULTS

Since the rms roughness is typically on the order of several nm [5] which does not shrink with the device shrinkage, LER brings a critical timing and power impact in the sub-45nm. Our experimental results for 45nm process show that the amplitude of LER can be as much as 10% from its nominal line edge at the typical process condition. Thus, we swept the LER variation from zero to 12 % of the nominal gate length. We first investigate the driving current variation with the amount of LER, then the delay variation with the different process conditions and LER value in our 45nm two input NAND standard cell.

Figure 5 shows the driving current variation with the different magnitude of LER for NMOS devices of two input NAND cell. We performed lithography simulations using 45nm process window to determine the amplitude of LER.

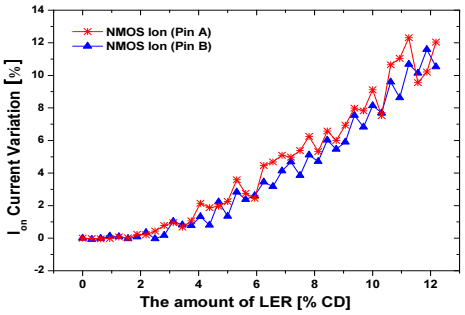


Figure 5: Current variation with LER amplitude.

The nominal gate length is 40nm, and the percent amount of LER means the edge rms roughness in terms of the nominal CD. The result reveals that the variation of the saturation current can be as much as 10 % where the rms LER value becomes 10 % from its nominal line edge.

For the systematic variation, we use lithography simulation to obtain different print-images/contours at different process corners. The process corners are defined for three different conditions: **(a)** a typical condition **(b)** $+3\sigma$ and **(c)** -3σ variations. The $\pm 3\sigma$ variations result in the lower ($\sim$thinner line) and upper ($\sim$thicker line) bounds of the process window. Each layer in the input cell layout is simulated with three different conditions. These three images for poly and diffusion layers result in a combination of nine different imaged. From these nine combinations, we choose the combinations that result in the ***best*** and ***worst*** case timing corners. The ***best*** (***worst***) timing corner occurs when the poly has minimum (maximum) value and the diffusion has largest (smallest) width.

We analyzed for delay variation with LER by applying L_{pi} to each device. The results for a nand cell is illustrated in Figure 6. The results indicate that the delay variation is trivial at the small amount of LER (less than 3% of nominal CD). However, we found the delay slope is so steep when the roughness of LER increase. The reason why the delay decreases is that the saturation current are exponentially increased as the gate length decrease on the basis of our current look-up tables.

We also induced the edge roughness for the case where no systematic variations were applied. We then compute the effective delay sensitivity using the formulations in Section 2.4 for the device LER variations at various lithography corners. The results for few cells from the 45nm bulk technology libraries are presented in Table 1.

Here column I are the sensitivities due to LER when considering no systematic lithography variations. Columns II, IV, VI are delay sensitivities due to LER when considering systematic litho variations at typical, best and worst corners respectively. Columns III, V, VII are the errors in these

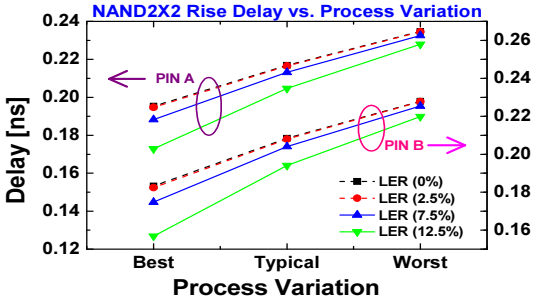


Figure 6: Timing variation with LER in NAND cell.

Table 1: Delay sensitivity due to LER variations

	d_{eff} @L_{nom} I	d_{eff} @typ II	Err (%) III	d_{eff} @$best$ IV	Err (%) V	d_{eff} @$worst$ VI	Err (%) VII
Inv	3.933	4.077	3.7	5.819	42.7	3.349	-17.8
NOR	3.544	4.070	14.8	5.581	37.1	3.612	-11.2
NAND	3.189	3.962	24.2	4.955	25.1	2.787	-29.6
DFF Delay	6.947	7.913	13.9	9.803	23.9	8.452	6.8
DFF Setup	9.136	9.694	6.1	12.514	29.1	6.462	-33.3

three corners when compared with that due to no systematic variations. The results indicate that the sensitivities due to LER variations increase at typical and best case corners when comparing with that due to no systematic variations; however the sensitivities at worst case corner are smaller. Thus, there is a non-trivial change in the sensitivities at different corners due to LER and need to be accounted appropriately during timing/leakage analysis.

4. CONCLUSION

In this paper, a new LER-aware characterization methodology which uses the non-rectangular gate print-images generated by lithography and etch simulations with the random LER variation has been reported in the sub-45nm design. We have systematically analyzed the random LER in terms of the impact on circuit performance due to LER variation and observed that the driving current was highly affected with LER as the gate length becomes thinner. Our experiments on a 2-input NAND cell using these LER values indicated that the rms LER could be about 10% from its nominal line edge, and the saturation current could vary by as much as 10% in our 45nm standard cell. We will further work the impact on the leakage current and other stress effects.

5. ACKNOWLEDGMENTS

This work is partially sponsored by NSF and SRC.

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