Layout Optimizations for Double Patterning Lithography

David Z. Pan, Jae-seok Yang, Kun Yuan, Minsik Cho†, and Yongchan Ban
Dept. of ECE, The University of Texas at Austin, Austin, TX 78712
†IBM T. J. Watson Research Center, Yorktown Heights, NY 10598
{dpan, jsyang, kyuan}@cerc.utexas.edu, minsikcho@us.ibm.com, ycban@cerc.utexas.edu

***Abstract*—Lithography process has become one of the most fundamental limitations for 22nm technology node because of the following reasons: 1) combining immersion and computational lithography, which is the most advanced lithography scheme, may not be enough to be used for 22nm patterning, 2) EUV (Extreme Ultra-Violet) lithography may not be available for mass production in the near future. As a practical solution, pitch doubling technique known as double patterning lithography (DPL) has become a strong candidate for 22nm lithography process. Since layout decomposition in DPL plays an important role in addressing the patterning quality, this paper will discuss some recent advancement of decomposition and optimization techniques for DPL friendly layout. We will also discuss the research challenges for double patterning from an EDA perspective.**

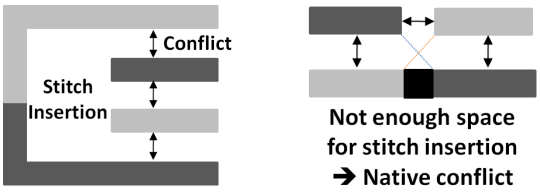
I. Introduction

Current lithography technology has been facing severe limitations because 193nm based lithography tool is hard to print sub-30nm half pitch patterns [1]–[6]. The smallest printable feature size is defined as K1·λ/NA where K1 is referred to as K-factor for a given process showing the difficulty of lithography. λ is wave-length of the light source, and NA is the numerical aperture determined by lens size. Since the lower bound of K-factor is 0.28 [7], it is challenging to print sub-30nm patterns with current lithography equipments.

One possible solution to overcome the limitation is to use high NA lithography system. Chip makers have been using immersion lithography for sub-40nm patterning which enhances NA from 0.93 (dry) to 1.35 (wet). However, it is hard to find new liquid material to increase NA more than 1.35 in the near future. E-beam lithography and nanoimprint are not yet in the mainstream [8], as well. As an ideal solution, EUV lithography has been proposed. Since the wavelength of EUV light source is 13.5nm, sub-10nm patterning is possible with EUV. However, EUV lithography equipment is not available for 22nm production due to technical barriers such as the lack of power sources, resists, and defect-free masks [9] [10].

An alternative choice for sub-22nm technology node is DPL [11]. In DPL, pitch size which limits the patterning resolution, becomes twice than that of single patterning. Double patterning can be implemented in three ways: Litho-Etch-Litho-Etch (LELE), Litho-Freeze-Litho-Etch (LFLE), and Self-Aligned Double Patterning (SADP). LELE uses two lithography exposures and etches on hard-mask to create smaller chip features. LELE uses fewer processing steps than SADP, but requires more accurate overlay control to align two exposures [12]–[15]. LFLE works by freezing the developed resist pattern of the first exposure, then adding a second resist layer immediately on top for the second exposure. The resist pattern is etched at one time after developing. LFLE uses fewer processing steps [16] [17]. SADP works by depositing a spacer layer over the chip covering all hard mask features. The covered layer is selectively etched away leaving two sidewalls along any ridge, then the ridge is removed [18]. The overlay requirement of SADP is less stringent than for other double patterning methods. However, SADP is only applicable for 1-D patterning having the same transistor length and requires more processing steps.

Every type of DPL requires layout decomposition before manufacturing [19] [20]. When two features are located closely within the minimum design rule, they need to be decomposed on two different masks for LELE and LFLE. SADP also requires layout decomposition to assign a feature to a specific sidewall. During decomposition, coloring conflict can be resolved by inserting stitches as shown in Fig. 1(a) without layout modification. However, minimum stitch insertion is preferred because of the following reasons: 1) stitch insertion requires overlap margin for overlay, resulting in unwanted chip area increase, 2) stitches may result in significant printability degradation due to overlay error and line-end effect [21].



(a) Resolvable conflict (b) Native Conflict

Fig. 1. Resolvable and native conflict.

Several decomposition methods to achieve minimum stitch insertion have been proposed after placement and routing [22] [23]. However, decomposition after layout generation may be too late to resolve all the conflicts. Fig. 1(b) shows a case in which stitch insertion cannot resolve a conflict. Such an irresolvable conflict is called a native conflict which can only be removed by layout modification. Therefore, an effort to reduce native conflicts should be taken during placement, routing, and redundant via optimization to shorten design time.

This paper will discuss the recent achievements to enhance decomposability and patterning quality in DPL.

In this paper, we will survey layout decomposition methods developed recently in section II. DPL friendly routing approaches will be introduced in section III. In section IV, we show other layout optimization issues for better double patterning quality. We draw the conclusion and point out some research directions in Section V.

II. Layout Decomposition

Double patterning layout decomposition can be categorized as rule-based and model-based methods. Rule-based approach is relative simple to apply, while time-expensive lithography modeling is required in model-based methodology.

Many research works, e.g., [22] [23] focus on rule-based methods. In [22], Kahng et al. proposed a practical double patterning layout decomposition flow. They first apply graph techniques to detect the features associated with irresolvable conflict cycles. When an odd number of conflicts are detected in a conflict graph, a stitch is inserted to break the conflict cycle. Then, the algorithm decomposes a design to minimize the number of stitches based on ILP formulation. Various design constraints, such as minimum width and minimum overlap margin, are also taken into account.

Yuan et al. [23] developed an ILP based layout decomposition algorithm for simultaneous conflict and stitch minimization. To enable effective co-optimization, they first proposed a grid model to provide fine resolution for splitting options. As Fig. 2 shows, the whole layout will be mapped into grids. Each grid is either empty or fully occupied by the pattern, and each occupied grid will be assigned one color. Any boundary between occupied grids is a potential splitting location. After formulating their algorithm into ILP problem, they also developed several speedup techniques to reduce problem size and improve the runtime and scalability. Their results show significant improvement over traditional two-phase decomposition flow which separates coloring and splitting stages.

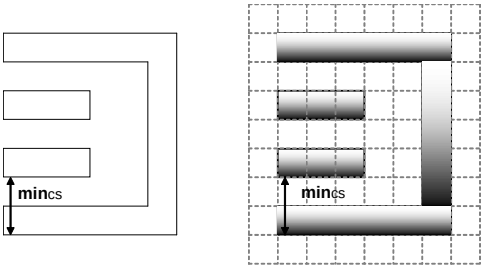
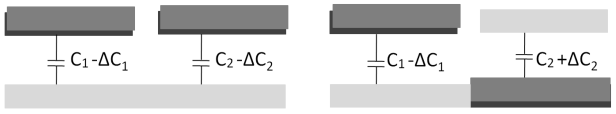


Fig. 2. Grid layout model for layout decomposition.

There are layout decomposition flows which include lithography simulation. In [24], Bailey et al. make use of Optical Proximity Correction (OPC) to analyze the quality of the decomposition. The validation result will be returned to the flow for iterative refinement. Chiou et al. [25] further apply a model-base pattern splitting method to locally correct irresolvable coloring errors after rule-based decomposition.



(a) Decomposition without overlay compensation (b) Decomposition with overlay compensation

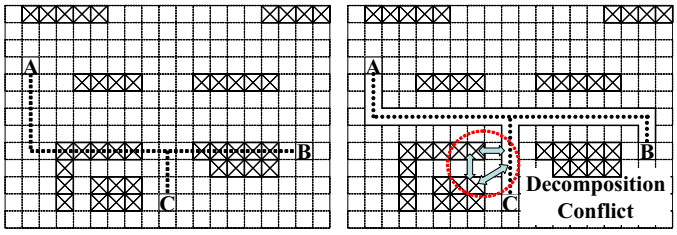
Fig. 3. Overlay compensated decomposition.

In [26], Yang et al. proposes an overlay aware timing analysis method from measurement of translation, rotation, and magnification overlay, and shows that decomposition plays a roll to compensate the overlay effect in terms of timing variation. Fig. 3 shows an observation how to compensate the overlay effect by decomposition. When we do not consider overlay during decomposition, the variation of a coupling capacitance between two metal layers are in the same direction as shown in Fig. 3(a). However, Fig. 3(b) shows less timing variation because C_1 decreases when C_2 increases with overlay.

III. DPL Friendly layout optimization

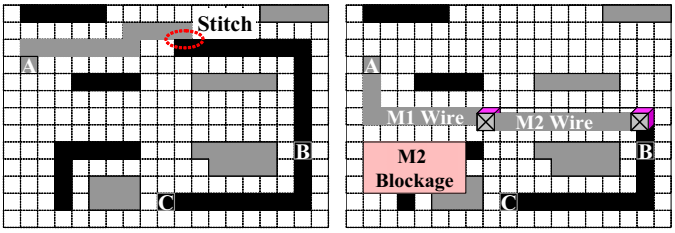
Layout decomposition is the most critical step for DPL, as discussed in Section I and II, especially highly complex for metal layers due to 2D patterns. However, layout decomposition itself can be very complex and NP-Complete, which cannot be solved by a 2-coloring algorithm. Therefore, such criticality and complexity of layout decomposition clearly requires design time consideration, more specifically during detailed routing and redundant via insertion. Current industrial effort to accomplish layout decomposition is to first finish detailed routing and via insertion, then perform layout decomposition for DPL. If there is any indecomposable polygon, rip-up&rerouting should be performed repeatedly to fix the conflict, resulting in long design-turn-around-time. A detailed routing oblivious DPL may generate highly complex patterns which may increase the indecomposable wire length. Additionally, finding a decomposable layout is not sufficient for successful DPL processes; the number of stitches should be minimized to make a layout robust against overlay error. Therefore, it is critical to consider DPL in a correct-by-construction manner during detailed routing and redundant via insertion.

Fig. 4 motivates why DPL-friendly detailed routing is a key to the successful DPL. For a net A-B-C, its Steiner tree is shown in Fig. 4(a). If a conventional router connects this net, it may generate a solution in Fig. 4(b) which is not decomposable (even with stitches) due to the conflict inside the circle, although it achieves the shortest possible wire length. If DPL-friendly detailed routing is applied to this net, we can get either (c) or (d) which is both decomposable for DPL with different overheads. We have a stitch in Fig. 4(c) but two vias in Fig. 4(d), in order to make a layout decomposable. Therefore, a detailed routing can play a critical role in improving layout decomposability by exploring the best trade-off among wire length, stitch, and via.



(a) Net A-B-C and its Steiner tree with WL=21 in the dotted line are shown. The checked boxes are the blockages on M1.

(b) A routing solution from a conventional detailed router has WL=24, but with decomposition conflicts inside the dotted circle.



(c) One DPL-friendly solution is shown with one stitch and WL=34.

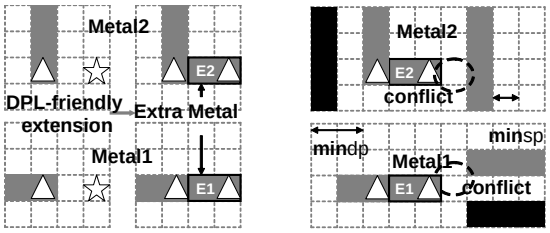
(d) Another DPL-friendly solution is shown without any stitch and WL=28, but with 2 vias.

Fig. 4. This example motivates DPL consideration during detailed routing. Detailed routing algorithm can make effective trade-off among layout decomposability, wire length, the number of stitches, and the number of vias.

Cho et al. [21] presents the first DPL friendly detailed routing algorithm which performs routing and layout decomposition in one shot, in a correct-by-construction manner. The key idea in [21] is to perform detailed routing and layout decomposition *simultaneously* in a correct-by-construction manner, in order to accomplish high layout decomposability and reduce the number of overlay-error-prune stitches. In detailed, while routing a net, the algorithm in [21] finds a path which introduces fewer DPL-related conflicts with the already routed wires. Since decomposition is done along with detailed routing, [21] directly outputs a decomposed layout without an extra time-consuming decomposition step. Experimental results in [21] show that the proposed approach improves the quality of layout significantly in terms of decomposability and the number of stitches with 3.6x speedup, compared with a current industrial DPL design flow.

Redundant via, widely used yield improvement technique, could introduce complexity in DPL compliance. Fig. 5(a) shows a motivational example, where the top rectangles are metal2 and the bottom rectangles are metal1. As Fig. 5(a) indicates, E1 and E2 are the extra metals, which is used to cover the via and the redundant via in both layers. To avoid introducing additional stitch, these extensions should have the same color because the metal and the via touches in corresponding layer. However, this may cause conflicts due to the coloring assignment of existing layout. In Fig. 5(b), the *stitch-free extension* will introduce a conflict in both metal1 and metal2.

As a solution of the problem, Yuan et al. [27] developed a detailed routing framework to perform double patterning lithography and redundant via co-optimization. First, they



(a) (b)

Fig. 5. Illustration of redundant via DPL-compliance problem

proposed an ILP based post-routing redundant via insertion algorithm to maximize insertion rate, while introducing zero conflict and minimal extra stitches to existing layout. Moreover, to better resolve this problem in design side, the authors also developed a DPL-friendly detailed router with redundant via consideration.

IV. Other Layout Optimization Issues

To relieve the complexity and difficulty of layout decomposition, many layout optimization and correction studies are conducted in terms of double patterning friendly OPC, gridded design, process-design co-optimization, etc.

For post layout correction, many studies [28]–[31] proposed a new OPC method to adapt double patterning and layout decomposition problem. In [28], Li at al. introduced an overlap correction method on the stitching locations. For any re-cut and/or redesigned pattern after verification, they categorized DP decompositions and introduced a new Adaptable OPC (Ad-OPC) algorithm by reusing post OPC layout to speed up the correction and improve its convergence according to environment surrounding. In a similar way, Gheith at al. in [29] suggested a DPL OPC method which can be able to consider interlayer misalignment and corner rounding at decomposed edges. Stitch point optimization for 3D wafer-topography effect due to stack structure is studied in [31]. Kamohara et al. investigate the impact of light reflectivity on the stitch point and suggested an optimal layout.

Gridded design rule based on one dimensional layout is one of solutions of DPL layout optimization. Many research works, e.g., [32] [33] have been reported a simple design rule for double patterning application. The basic idea is that the target design layout is drawn with a single pitch and a single line/space type to get the best process-robust layout. In [32], Bencher et al. demonstrated the scaling capability of gridded design rule to 16nm and 22nm logic nodes and reported the results of their implementation on Intel 45nm node poly-silicon layer. Smayling et al. in [33] reported results of gridded rule for 22nm logic design in SADP.

Process-design co-optimization [34] [35] has been actively studied to overcome the resolution limit. In [34], Rubinstein et al. used pattern matching technique and suggested through focus model to find process weak pattern for double patterning. The pattern matcher is orders of magnitude faster than full simulation, and can be used to quickly scan layouts for process sensitivities. This through-focus model allows the

pattern matcher to test if a layout contains any focus hotspot, or to predict how sensitive a given pattering through the focus change. In [35], Smayling et al. reported an illumination optimization to adapt their gridded design rule. They also optimized several variables including lithography, mask, RET, circuit design, and potential process extensions.

V. Conclusion and Future Directions

Double patterning is a leading candidate for 22nm lithography solution and probably 15nm technology node depending on EUV availability. In this paper, we show several layout decomposition approaches for minimum stitch, and layout optimization for better double patterning lithography: simultaneous decomposition and routing, redundant via optimization, new OPC method for overlap correction on stitches. They work together to enhance double patterning decomposability and patterning quality.

Since double pattering is under active developing, it provides still many research opportunities for EDA engineers in mainly three ways: layout decomposition for better patterning quality, double patterning friendly layout optimization including DPL aware standard cell design and placement, and overlay error consideration in design tools. In addition, to enhance more lithography quality, multiple patterning for a contact layer or other critical layers will provide more research opportunities.

VI. Acknowledgment

This work is supported in part by NSF CAREER Award, SRC, IBM Faculty Award, Qualcomm, Fujitsu, Sun, KLA-Tencor, and equipment donations from Intel.

References

[1] L. Huang and D. F. Wong, "Optical Proximity Correction (OPC)-Friendly Maze Routing," in *Proc. Design Automation Conf.*, Jun 2004, pp. 186 – 191.

[2] Y.-R. Wu, M.-C. Tsai, and T.-C. Wang, "Maze Routing with OPC Consideration," in *Proc. Asia and South Pacific Design Automation Conf.*, Jan 2005, pp. 198 – 203.

[3] T.-C. Chen and Y.-W. Chang, "Routability-driven and Optical Proximity Correction-aware Multilevel Full-Chip Gridless Routing," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26, no. 6, pp. 1041–1053, Jun 2007.

[4] J. Mitra, P. Yu, and D. Z. Pan, "RADAR: RET-Aware Detailed Routing Using Fast Lithography Simulations," in *Proc. Design Automation Conf.*, Jun 2005, pp. 369 – 372.

[5] T. Kong, H. Leung, V. Raghavan, A. K. Wong, and S. Xu, "Model-assisted routing for improved lithography robustness," in *Proc. of SPIE*, vol. 6521, Feb 2007, p. 65210D.

[6] H. J. Levinson, *Principles of Lithography, 2nd Edition*. SPIE Publications, 2005.

[7] A. K. Wong, *Resolution Enhancement Techniques in Optical Lithography*. SPIE Publications, 2001.

[8] L. W. Liebmann, "Layout impact of resolution enhancement techniques: impediment or opportunity?" in *Proc. Int. Symp. on Physical Design*, Apr 2003, pp. 110–117.

[9] O. Wood, C.-S. Koay, K. Petrillo, H. Mizuno, and S. Raghunathan, "Integration of EUV lithography in the fabrication of 22-nm node devices," in *Proc. of SPIE*, vol. 7271, Feb 2009.

[10] M. Dusa, J. Finders, and S. Hsu, "Double patterning lithography: The bridge between low k1 ArF and EUV," in *mic*, Feb 2008.

[11] K. Lucas, C. Cork, A. Miloslavsky, G. Luk-Pat, L. Barnes, J. Hapli, J. Lewellen, G. Rollins, V. Wiaux, and S. Verhaegen, "Interactions of double patterning technology with wafer processing, OPC and design flows," in *Proc. of SPIE*, vol. 6924, Feb 2008.

[12] D. Laidler, P. Leray, K. D'have, and S. Cheng, "Sources of Overlay Error in Double Patterning Integration Schemes," in *Proc. of SPIE*, vol. 6922, Feb 2008.

[13] W.-K. Ma, J.-H. Kang, C.-M. Lim, H.-S. Kim, S.-C. Moon, S. Lalbahadoersing, and S.-C. Oh, "Alignment system and process optimization for improvement of double patterning overlay," in *Proc. of SPIE*, vol. 6922, Feb 2008.

[14] I. Englard, R. Piech, C. Masia, N. Hillel, L. Gershtein, D. Sofer, R. Peltinov, and O. Adan, "Accurate in-resolution level overlay metrology for multi patterning lithography techniques," in *Proc. of SPIE*, vol. 6922, Feb 2008.

[15] D. Choi, C. Lee, C. Bang, D. Cho, M. Gil, P. Izilson, S. Yoon, and D. Lee, "Optimization of high order control including overlay, alignment, and sampling," in *Proc. of SPIE*, vol. 6922, Feb 2008.

[16] T. Ando, M. Takeshita, R. Takasu, Y. Yoshii, J. Iwashita, S. Matsumaru, S. Abe, and T. Iwai, "Pattern Freezing Process Free Litho-Litho-Etch Double Patterning," in *Proc. of SPIE*, vol. 7140, Feb 2008.

[17] H. Sugimachi, H. Kosugi, T. Shibata, J. Kitano, K. Fujiwara, , , M. Mita, A. Soyano, S. Kusumoto, M. Shima, and Y. Yamaguchi, "CD Uniformity improvement for Double-Patterning Lithography (Litho-Litho-Etch) Using Freezing Process," in *Proc. of SPIE*, vol. 7273, Feb 2009.

[18] W. Shiu, H. J. Liu, J. S. Wu, T.-L. Tseng, C. T. Liao, C. M. Liao, J. Liu, and T. Wang, "Advanced self-aligned double patterning development for sub-30-nm DRAM manufacturing," in *Proc. of SPIE*, vol. 7274, Feb 2009.

[19] T.-B. Chiou, R. Socha, H. Chen, L. Chen, S. Hsu, P. Nikolsky, A. van Oosten, and A. C. Chen, "Development of layout split algorithms and printability evaluation for double patterning technology," in *Proc. of SPIE*, vol. 6924, Feb 2008.

[20] N. Toyama, T. Adachi, Y. Inazuki, T. Sutou, Y. Morikawa, H. Mohri, and N. Hayashi, "Pattern decomposition for double patterning from photomask viewpoint," in *Proc. of SPIE*, vol. 6521, Feb 2007.

[21] M. Cho, Y.-C. Ban, and D. Pan, "Double Patterning Technology Friendly Detailed Routing," in *Proc. Int. Conf. on Computer Aided Design*, Nov 2008.

[22] A. Kahng, C.-H. Park, and H. Yao, "Layout Decomposition for Double Patterning Lithography," in *Proc. Int. Conf. on Computer Aided Design*, Nov 2008.

[23] K. Yuan, J.-S. Yang, and D. Z. Pan, "Double patterning layout decomposition for simultaneous conflict and stitch minimization," in *Proc. Int. Symp. on Physical Design*, March 2009.

[24] G. Bailey, A. Tritchkov, J. Park, L. Hong, V. Wiaux, E. Hendrickx, S. Verhaegen, P. Xie, and J. Versluijs, "Double pattern eda solutions for 32nm hp and beyond," in *Proc. of SPIE*, vol. 6521, Feb 2007.

[25] T.-B. Chiou, R. Socha, H. Chen, L. Chen, S. Hsu, P. Nikolsky, A. van Oosten, and A. C. Chen, "Development of layout split algorithms and printability evaluation for double patterning technology," in *Proc. of SPIE*, March 2008.

[26] J.-S. Yang and D. Z. Pan, "Overlay Aware Interconnect and Timing Variation Modeling for Double Patterning Technology," in *Proc. Int. Conf. on Computer Aided Design*, Nov 2008.

[27] K. Yuan, K. Lu, and D. Z. Pan, "Double patterning lithography friendly detailed routing with redundant via consideration," in *Proc. Design Automation Conf.*, July 2009.

[28] Y. Pan, H. Zhang, and Y. Chen, "A new OPC method for double patterning technology," in *Proc. of SPIE*, vol. 6924, Feb 2008.

[29] M. Gheith, L. Hong, and J. Word, "OPC for reduced process sensitivity in the double patterning flow," in *Proc. of SPIE*, vol. 7274, Feb 2009.

[30] X. Li, G. Luk-Pat, C. Cork, L. Barnes, and K. Lucas, "Double-patterning-friendly OPC," in *Proc. of SPIE*, vol. 7274, Feb 2009.

[31] I. Kamohara and T. Schmoeller, "Split, overlap/stitching, and process design for double patterning considering local reflectivity variation by using rigorous 3D wafer-topography/lithography simulation," in *Proc. of SPIE*, vol. 7274, Feb 2009.

[32] C. Bencher, H. Dai, and Y. Chen, "Gridded design rule scaling: taking the CPU toward the 16nm node," in *Proc. of SPIE*, vol. 7274, Feb 2009.

[33] M. C. Smayling, C. Bencher, H. D. Chen, H. Dai, and M. P. Duane, "APF pitch-halving for 22nm logic cells using gridded design rules," in *Proc. of SPIE*, vol. 6925, Feb 2008.

[34] J. Rubinstein and A. R. Neureuther, "Through-focus pattern matching applied to double patterning," in *Proc. of SPIE*, vol. 7274, Feb 2009.

[35] M. C. Smayling and V. Axelrad, "32nm and below logic patterning using optimized illumination and double patterning," in *Proc. of SPIE*, vol. 7274, Feb 2009.