Layout Decomposition of Self-Aligned Double Patterning for 2D Random Logic Patterning

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ABSTRACT

Self-aligned double pattering (SADP) has been adapted as a promising solution for sub-30nm technology nodes due to its lower overlay problem and better process tolerance. SADP is in production use for 1D dense patterns with good pitch control such as NAND Flash memory applications, but it is still challenging to apply SADP to 2D random logic patterns. The favored type of SADP for complex logic interconnects is a two mask approach using a core mask and a trim mask. In this paper, we first describe layout decomposition methods of spacer-type double patterning lithography, then report a type of SADP compliant layouts, and finally report SADP applications on Samsung 22nm SRAM layout. For SADP decomposition, we propose several SADP-aware layout coloring algorithms and a method of generating lithography-friendly core mask patterns. Experimental results on 22nm node designs show that our proposed layout decomposition for SADP effectively decomposes any given layouts.

Keywords: Double patterning, SADP, decomposition, lithography, random logic patterning, sub-30nm

1. INTRODUCTION

SADP is a pitch-splitting sidewall image method that also utilizes two masks: a *core* mask and a *trim* mask. The core mask defines core mandrel patterns, and the sidewall spacer is deposited onto all sides of a mandrel pattern to enable pitch doubling in the patterning. The trim mask removes unnecessary patterns by blocking or unblocking with photoresist (PR). Since the most critical patterning control in SADP is not governed by lithography, but by the deposition of the sidewall spacer, it guarantees less overlay requirements and excellent variability control compared to LELE DPT [1–5].

However, SADP allows only a single width of sidewall spacer which forms either a single wire width or a single wire space. Therefore, SADP was previously limited by the lack of flexibility in terms of layout decomposition. Thus, SADP is in production use for 1D patterns in NAND Flash memory applications but applying SADP to 2D random logic patterns is challenging [5–7]. Due to its limitation, SADP might require three masks for 2D-type application. However, since the manufacturing cost of logic products is dominated by the mask cost, a two-mask SADP approach is necessary for successful product application. Thus, layout decomposition for random 2D-type complex logic features which have various wire width and space is a primary challenging issue for a two-mask SADP process.

In this paper, we propose rigorous layout decomposition methods on SADP technique for sub-30nm random shaped logic metal layouts. This paper describes methods for automatically choosing and optimizing the manufacturability of base core mask patterns, generating assist core patterns, and optimizing trim mask patterns in SADP process. The major contributions of this paper include the following:

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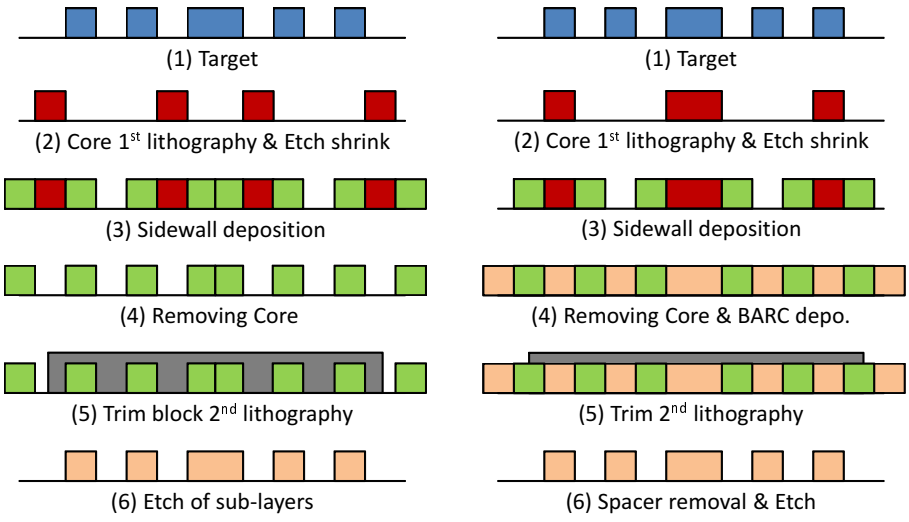
- Methods of SADP mask decomposition with a two-mask approach for random 2D-type logic features are proposed. Base core mask patterns are made up of main core patterns which are chosen from the original layout using our SADP-aware layout coloring and of assist core patterns which can be generated in a lithography friendly manner.
- The layout coloring highly affects the manufacturability of the core mask and trim mask layout. To resolve manufacturing conflict on the core mask layout, we propose a grouping and merging algorithm. Meanwhile, we propose a trim mask friendly coloring incorporated with shortest-path coloring which can produce the best coloring layout for the trim mask layout.
- We evaluate our technique on $22nm$ node industrial standard cells and SRAM logic designs. By introducing layout retargeting we can achieve a feasible SADP decomposition for random 2D design which shows various spaces and widths

The rest of the paper is organized as follows. Section 2 describes SADP lithography process and the challenging issues. Section 3 presents several layout coloring approaches for DRC-free decomposed mast layouts and algorithms of the core mask generation. A type of SADP compliant layouts is presented in Section 4. Experimental results are discussed in Section 5, followed by conclusions in Section 6.

2. SPACER-TYPE DOUBLE PATTERNING

We first summarize some terminologies and notations which are used throughout this paper:

- *Core mask*: the first mask in the SADP process flow.
- *Mandrel*: the printed patterns generated by the core mask where the sidewall spacers are subsequently formed.
- *Main mandrel*: the base mandrel layout which is a chosen subset of the design intent.
- *Additional mandrel*: the extra mandrel layout whose features need to be newly generated.
- *Secondary metal*: the layout except the main mandrel in the original layout. It is generated by merging of spacer patterns of mandrel layouts.



(a) SIM-type SADP (b) SID-type SADP

Figure 1. Two types of self-aligned double pattering

- *Spacer*: the sidewall spacer, which is deposited on the mandrel layout, is formed at the both sides of mandrels.
- *Trim mask*: the second mask in the SADP process flow and for removing away unnecessary segments of metals.

Two types of SADP process are popularly used for the state-of-the-art lithography patterning: SIM-type SADP and SID-type SADP. Figure 1 shows the vertical view of SADP process sequences for SIM (a) and SID (b) type SADP. SIM is an abbreviation of "spacer is metal" where the sidewall spacer itself becomes the final metal patterns. Core layout, which is called as *mandrel* layout and becomes the first mask layout in SADP, is designed based on the space region between metal lines as in (a)-(2). Then, the side-wall spacers are generated based on the core mandrel layout in (a)-(3). After removing mandrels in (a)-(4) and processing the second mask trimming step in (a)-(5), the final dense features are patterned on wafer matched with the design intent in (a)-(6).

The other type of SADP is SID which is an acronym of "spacer is dielectric". The steps are similar to SIM, but, in SID-type SADP the side-wall spacer is just dielectric. Meanwhile, the mandrel layout becomes final metal patterns. The base mandrel layout is chosen from the original layout as shown in Figure 1(b)-(2). Then, the sidewall spacers are generated nearby the mandrel layout in (b)-(3). After removing mandrels, we deposit substrate materials in (b)-(4). Then, the second trimming mask is used for getting the final patterns in (b)-(5)&(6). Since the base mandrel layout is a subset of the original layout and should have enough layout pitch for the 1^{st} lithography patterning, it is usually chosen from the layout coloring [4,5].

Since the width of the sidewall spacer is constant, it is hard to vary the pattern line-width in SIM-type SADP because the sidewall spacer becomes the metal line. Whereas, in SID-type SADP it is hard to control the pattern space because the side wall spacer becomes a space between two Mandrel metal patterns in SID. Since the core mandrel layout in SID-type SADP becomes the final metal pattern, SID-type SADP enables various metal widths. Moreover, as SID-type SADP has fewer process steps than SIM-type SADP, it provides more cost effective metal patterning [5,7].

Let us look at SID-type SADP sequences in a way of top view in Figure 2. The layout coloring is first done to select the base mandrel from the original target in (2). Either color between two colored layouts can be the base mandrel in our approach. Then, extra mandrel layouts are added on the base mandrel to eventually make patterns which are not chosen to the base mandrel. Note that the fist core mask is usually biased and bigger than the design intent for better lithography printability in (3). After decreasing the first mandrel pattern as much

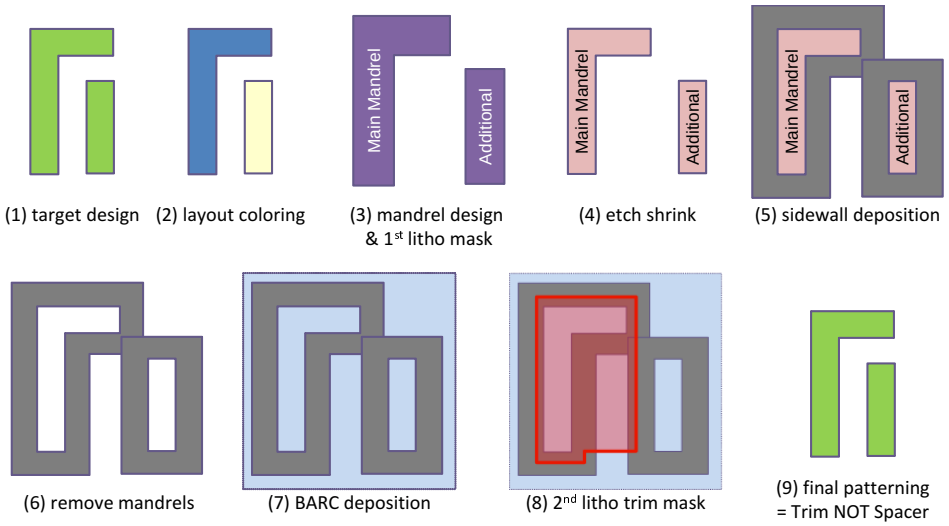


Figure 2. The top view of SID-type SADP process

as the target size in (4), the sidewall spacers are formed around the mandrel as in (5). After removing mandrels in (6) and depositing the substrate material, e.g., BARC in (7), we remove out the unnecessary polygons except the design intent with the trim mask in (8).

Note that since the spacer patterns nearby mandrels will be etched out after the trim mask patterning, the spacer acts like a layout separator among the main mandrel and the secondary metal line. It implies that if the edge of a trim mask layout is on the spacer region, the trim layout can be free from mask overlay variations without any impact on target metal lines. In the other words, we should carefully control the mask overlay if the trim mask edge is on metal lines.

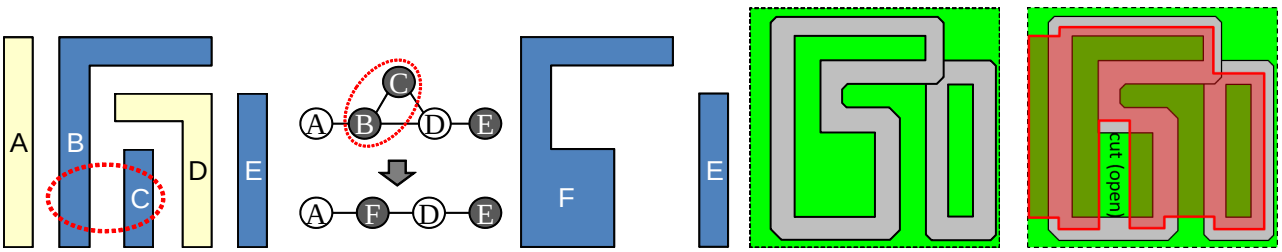
There are many challenges involved with creating a core mandrel mask and a trim mask for complex 2D layouts. In particular, layout coloring and assist mandrel generation are utmost important steps in an SADP mask synthesis process: layout coloring and additional mandrel generation. The manufacturability on both the core mask and trim mask is significantly dependant on layout coloring which, therefore, is one of crucial steps in SADP mask decomposition. The trim mask provides additional flexibility for patterning 2D patterns on wafer. Layout coloring is more highly affects on the lithographic printability of the second trim mask rather than the core mask. We will discuss it in Section 3.1 and 3.2. It requires an intelligently designed mandrel layouts as a good starting point. The assist mandrel will provide the shapes of the secondary metal pattern, and it highly affects the lithographic printability of the fist core mask. Let us see the detail in Section 3.3.

3. MODELING OF MASK DECOMPOSITION FOR SADP

3.1. Grouping and Merging Coloring

Since SADP mask decomposition does not allow stitch insertion, some coloring conflict is usual. As shown in Figure 3, the target design has a native coloring conflict which represents an undecomposable layout even in LELE [1, 8]. To resolve this coloring conflict, we introduce a grouping and merging algorithm [9]. Once two same colored polygons are within the minimum coloring distance d, we make a group for the polygons and merge them into one polygon. By merging the two conflicted polygons, we can make a core mask without any DRC and lithography violations. This merged region between two grouped polygons should be trimmed out at the 2^{nd} trim mask patterning step. Note that since the spacer patterns nearby mandrels will become dielectric after the trim mask patterning, the spacer acts like an overlay-free region. It implies that if the edge of a trim mask layout is on the spacer region, the trim layout can be free from mask overlay variations without any impact on target metal lines. In the other words, we should carefully control the mask overlay if the trim mask edge is on metal lines. Thus, we should note the following issues if a trim mask should cut the merged area:

- The width/space of a trim mask should meet the trim mask width constraint which is usually the same as the minimum target layout width/space or slightly larger.
- Since the edge of a trim mask layout is passing over the main mandrel not the safe spacer region, the overlay error of the trim mask should be carefully controlled.



(a) coloring conflict (b) grouping (c) merging & core (d) spacer generation (e) trim cutting

Figure 3. Grouping and merging coloring

3.2. Trim Mask Friendly Coloring

Since the sidewall spacer can be placed between two abutting metal polygons, it can exactly identify the edge position of different metal lines. It implies that the sidewall spacer prevents abutting metal lines from patterning faults, in particular, bridging fault. Moreover, it can give the trim mask more process tolerance. As shown in Figure 4, a conventional layout coloring might give smaller patterning margin, e.g., narrower trim width or width violation. In addition, the trim mask is prone to mask overlay. Where possible, *the best coloring for SID-type SADP is to assign a different color on polygons in every other layout pitch track.*

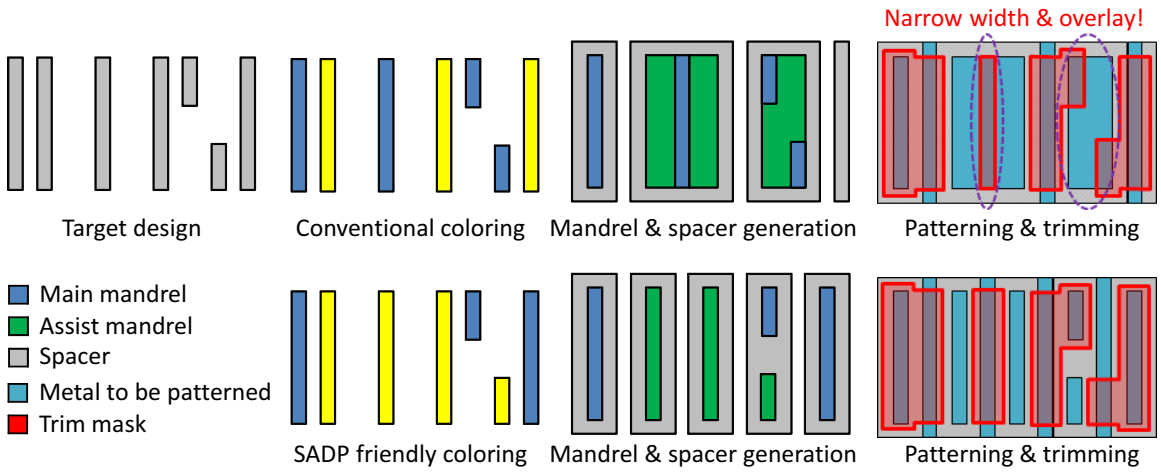


Figure 4. Trim mask friendly coloring

To assign the best coloring on the layout, we insert dummy layouts between two metal lines as shown in Figure 5 [9]. Once we put dummy metals into vacant areas, we assign two-map layout color. After removing the dummy metals, we can get the trim mask friendly layout coloring for SID-type SADP process.

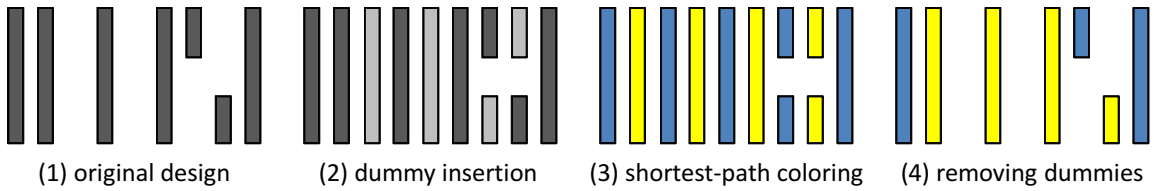


Figure 5. Dummy insertion for trim friendly coloring

3.3. Litho. Friendly Mandrel Layout

Figure 6 illustrates a way to generate assist mandrel patterns in addition to the main mandrel [9]. The goal of the assist mandrel is to make secondary patterns by merging neighboring spacer sidewall spacer of nearby Mandrel. There should be spacer patterns next to every secondary metals. Since Mandrel makes sidewall spacer which also generates secondary metal, in an intuitive way we can make assist mandrel in every neighboring secondary metals as much as the minimum spacer width away. Meanwhile as main mandrel also generates sidewall spacer patterns, we can filter out overlapped assist mandrel which lies on the interacting region of main mandrel within the distance (the minimum spacer width + the mask bias for the 1^{st} pattering).

Figure 7 shows the final core mask layout (main mandrel + assist mandrel) in different ways. We can generate assist mandrel patterns for 2D random layouts with different options, for example *the shorter* assist mandrel, *the longer* assist mandrel, and *the directional* assist mandrel. The shorter assist mandrel approach builds assist mandrel polygons just at the area facing with the secondary metal, secondary metal. This approach induces lots of small island patterns. Some small patterns in the core mask are prone to be collapsed due to photoresist (PR)

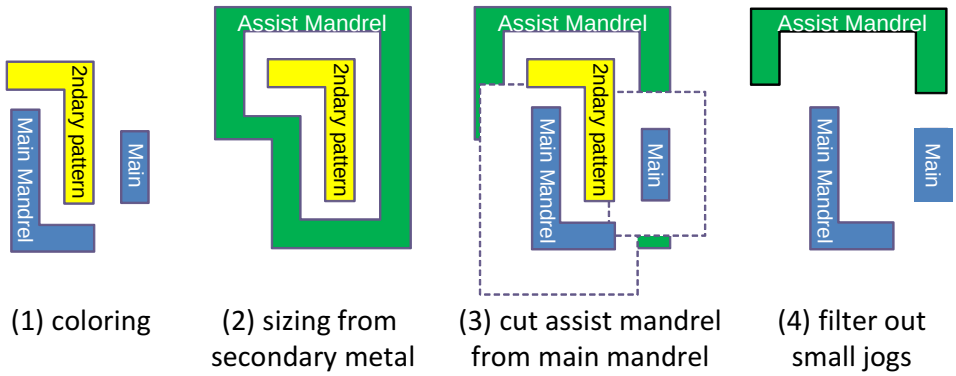
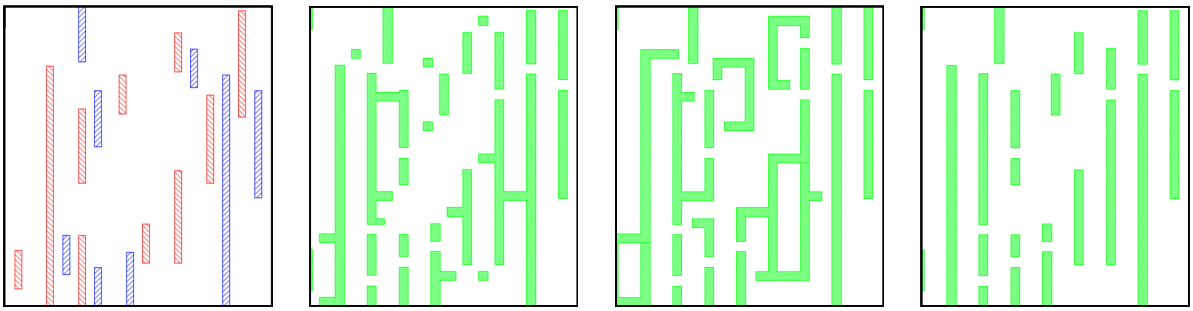


Figure 6. Generation of assist mandrel

tension or moved away due to lithography proximity. Thus, one can also use the longer assist mandrel approach which generate assist mandrel patterns covering all surrounding areas of secondary metal.

Another option is the directional assist mandrel approach which makes assist mandrel by considering lithography illumination. Off-axis illumination (OAI) is a widely used for better lithographic printability. An oblique illumination improves patterning resolution of those features toward the illumination direction [10]. It directly implies that a single directional metal layout is desirable for lithography patterning. Thus, in the directional assist mandrel approach we generate assist mandrel at the area which has the same direction with the metal lines. This approach is similar to the shorter assist mandrel approach at the first stage, yet by removing a small island, which is usually located at the metal line-end, we can achieve directional assist mandrel polygons.

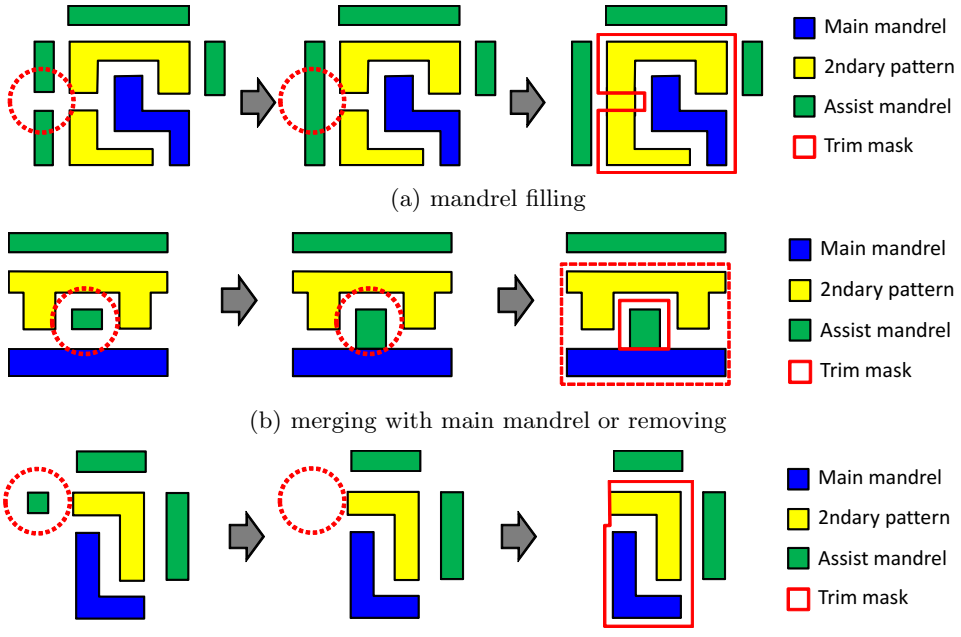


(a) coloring (b) shorter (c) longer (d) directional

Figure 7. Lithography friendly assist mandrel: where blue layout in (a) becomes main mandrel.

3.4. Additional Mandrel Post-processing

If the space among assist mandrels is smaller than a certain constraint, we can fill a space and make a polygon by connecting assist mandrels in order not to violate mask rule in the core mask [9]. Once we connect between two assist mandrels, the corresponding secondary metal might be also connected. Thus, the connected region at secondary metal should be removed at the 2^{nd} trim mask step (Figure 8(a)). In a similar way, if small pieces of assist mandrel are conflicting with main mandrel, we can merge them into main mandrel or remove them. When small assist mandrel is merged into main mandrel, both the merge area and small assist mandrel should be cut at the trim mask, which might be an overlay burden to main mandrel. Meanwhile, when small assist mandrel is removed, secondary metal region might be extended, thus it should be removed, which might give an overlay burden to secondary metal (Figure 8(b)). If a piece of assist mandrel is smaller than a certain constraint, we can remove it (Figure 8(c)).



(a) mandrel filling

(b) merging with main mandrel or removing

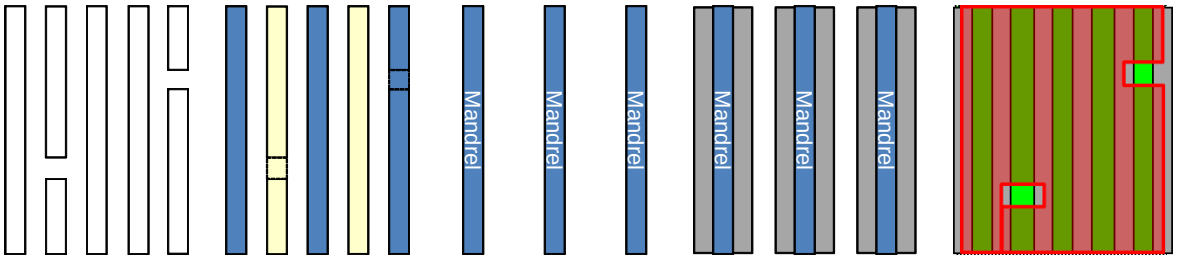
(c) removing

Figure 8. Options of assist mandrel layouts

4. STUDY OF SADP COMPLIANT LAYOUTS

4.1. SADP Compliant Layouts

A random metal layer has various shapes of layouts. When decomposing 2D layout, we happen to meet lots of DRC conflict on both core mask and trim mask. Thus by studying several cases of layouts which seem to be hard to decompose, we can have more flexibility for SADP layout decomposition, SADP-aware routing, and so on.



(a) target design (b) color&group (c) mandrel design (d) sidewall spacer (e) trim mask

Figure 9. Line-end: the space or width of the merged region should be equal or larger than the minimum space or width resolution of the trim mask.

Line-end control: According to a previous research [5], the minimal space of between two line-ends (tip-to-tip) in LELE DPT is twice larger than that of SADP. It is mainly because the tip-to-tip space can be achieved by the cutting (trim) mask. Thus, the minimal space in SADP is highly dependant on the resolution of a isolated pattern on a trim mask. Figure 9 shows a way of a line-end control in SADP process. By using our grouping and merging algorithm, the space between two line-ends can be merged so that the two lines become a united line in (b). Based on the modified layout, mandrel layout can be decided by layout coloring, and assist mandrel patterns are generated if needed in (c). Then, the sidewall spacer patterns are generated nearby the mandrel patterns in (d). Finally, the target patterns on wafer can be printed by eliminating unnecessary patterns using a

trim mask. Since the space CD of the trim mask in (e) can be controlled by trim mask OPC (optical proximity correction) and other RET (resolution enhancement technique) approaches.

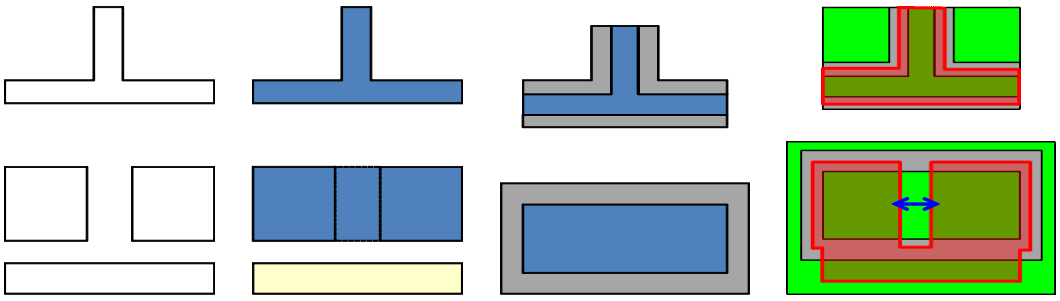


Figure 10. T-shapes: the space or width of the merged region should be equal or larger than the minimum space or width resolution of the trim mask.

T- or X-shapes: Like as LELE DPL, an island type of T- or X-shaped pattern can be easily generated in SADP process because there isn't any coloring conflict when we choose main mandrel layout. However, T- or X-opened area might induce coloring conflict as shown in Figure 10. To resolve layout conflict on mandrel patterns, we can use grouping & merging approaches in (b) where the smallest merged region among several candidates to be merged can be selected [9]. This is because after merging two conflicted polygons into one polygon the trim mask should remove the merged region at the cost of mask overlay. Therefore, shorter trim mask for removing merged region is preferable for smaller overlay impact on the 2^{nd} patterning.

By merging two conflict polygons in (b), mandrel layout can be decided by layout coloring. Then, the sidewall spacer patterns are generated nearby the mandrel patterns in (c). Finally, the target patterns on wafer can be printed by eliminating unnecessary patterns and the merged regions using a trim mask in (d). Note that the space of the merged region should be equal or larger than the minimum space resolution of the trim mask. Therefore, if the merged region is smaller than the trim minimum resolution, we should modify the target design intent by iterating layout design.

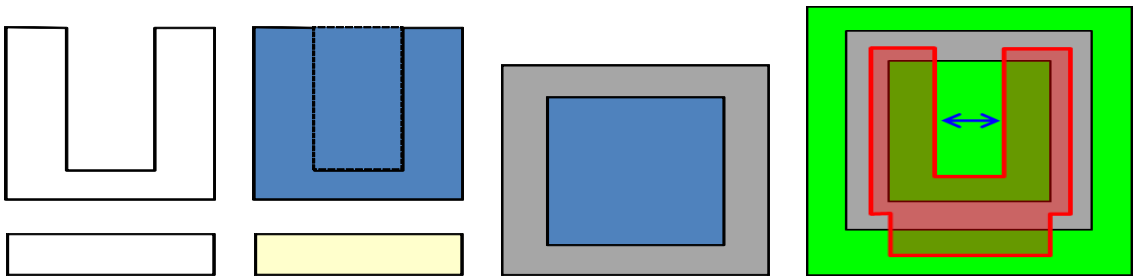
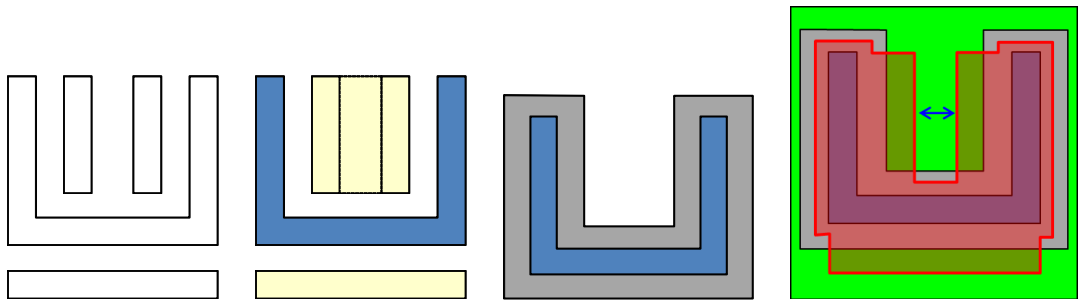


Figure 11. U-bend (short range): the space or width of the merged region should be equal or larger than the minimum space or width resolution of the trim mask.

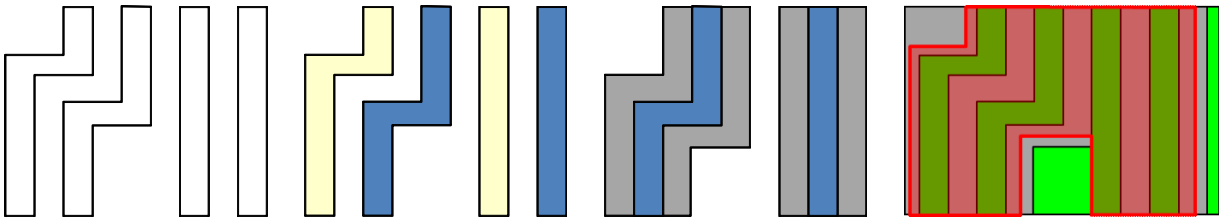
Narrow U-bend: A short ranged U-bend shapes in LELE DPL can be pattered by introducing 'stitch' point [3, 11]. However, in case there is one more line just bellow the U-shape in Figure 11, the layout can't be decomposed due to a type of native conflict in LELE DPL [8]. Meanwhile in SADP a short ranged U-shapes can be generated using grouping & merging algorithm. By using our grouping and merging algorithm, the space between two patterns can be merged into one polygon in (b). Based on the mandrel layout, the sidewall spacer patterns are generated nearby the mandrel patterns in (c). Then, the target patterns on wafer can be printed by eliminating the merged regions using a trim mask in (d). The space of the merged region should be equal or larger than the minimum space resolution of the trim mask. Therefore, if the merged region is smaller than the trim minimum resolution, we should modify the target design intent.



(a) target design (b) color&grouping (c) sidewall spacer (d) trim mask

Figure 12. U-bend (long range): the space or width of the merged region should be equal or larger than the minimum space or width resolution of the trim mask.

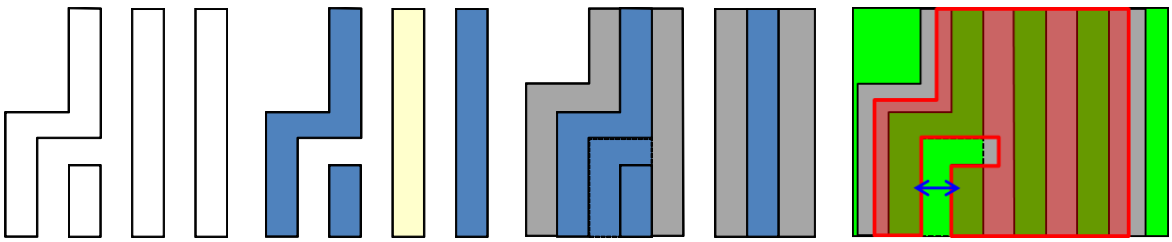
Wide U-bend: A long ranged U-bend shapes can be easily printed since the space of the U-shape is larger than the resolution of the 1^{st} mandrel mask. In case there are some patterns in the space of the U-shape, we can achieve the wafer patterning using grouping & merging approach. In a same fashion, the space of the merged region should be equal or larger than the minimum space resolution of the trim mask.



(a) target design (b) color&grouping (c) sidewall spacer (d) trim mask

Figure 13. Jogged features: the space or width of the merged region should be equal or larger than the minimum space or width resolution of the trim mask.

Jogged features: Even its lithographic printability issue, jogged features are a usual pattern shape for layout routing. If layout patterns don't have any conflicts in layout coloring, SADP decomposition can be easily achieved. As shown in Figure 13, the target design is subject to decompose with two colors without any conflict in (b), which provides robust core mask and trim mask layout in (c) and (d). The jogged layout shape may introduce assist mandrel patterns in order to support the secondary pattern.



(a) target design (b) color&grouping (c) sidewall spacer (d) trim mask

Figure 14. Jogged features (h-type): the space or width of the merged region should be equal or larger than the minimum space or width resolution of the trim mask.

h-type jogged features: h-type features are one of non-compliant layout types because it causes non-colorable and non-trim friendly layout. In Figure 14(a), the small island pattern, jogged features and next straighten line induce odd-cycle coloring conflict. Even our grouping and merging algorithm, the 2^{nd} trim mask may introduce MRC conflict due to smaller width and space. Like as above feature types, the space of the merged region in the

core mask should be equal or larger than the minimum space resolution of the trim mask.

4.2. Layout Retargeting for SADP Compliant

Since the width of a sidewall spacer is usually constant, in order to apply SADP process to 2D random logic, design retargeting may be necessary. A design retarget means to slightly modify the design intent in layout, and it usually induces a slight increase of a metal width in SID-type SADP. Slightly increased (thicker) metal lines are an improvement due to the following reasons: (1) The thicker metal line is better for timing issues, in particular delay. Despite a small increase of coupling capacitance, a resistance decrease is more favorable for metal delay. (2) It is even better for lithography patterning. Thicker metal lines have more tolerance due to lithography process for sub-30nm patterning.

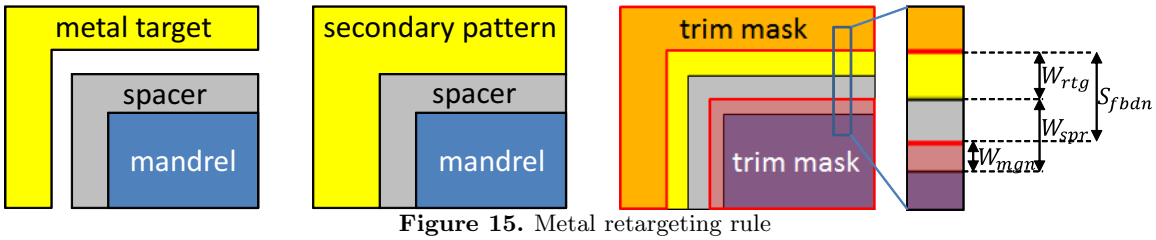


Figure 15. Metal retargeting rule

Therefore, we define a forbidden space for layout retargeting between the two colored layouts, in particular, the main mandrel and the secondary metal. As shown in Figure 15, let S_{fbdn} be the forbidden space for SID-type SADP process, S_{trm} be the minimum allowable space of the trim mask, W_{mgn} be the trim mask overlay margin for the design intent, W_{spr} be the sidewall spacer width, and W_{rtg} be the width of the allowable retargeting. The forbidden space in SID-type SADP is as follows:

$$W_{spr} < S_{fbdn} < S_{trm} \tag{1}$$

Thus, if the S_{trm} is same as the W_{spr}, no forbidden space exists in an SADP mask decomposition. Since, W_{spr} and W_{mgn} are fixed in SADP lithography process, the maximum retargeting width of the design intent, W_{rtg}, is defined as follows:

$$W_{rtg} = S_{fbdn} - (W_{spr} - W_{mgn}) \tag{2}$$

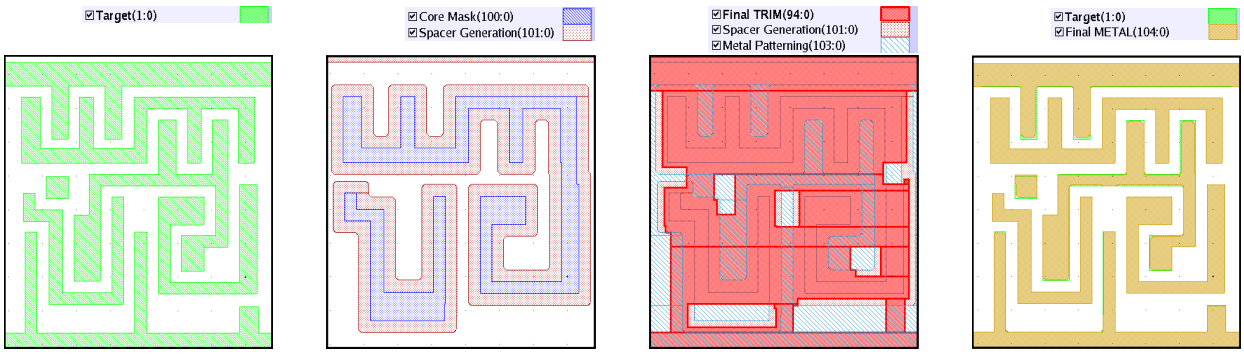
By introducing the maximal allowable retargeting width at the trim mask, we can have more flexibility on layout decomposition and lithography manufacturing in SID SADP.

5. EXPERIMENTAL RESULTS

We implemented a mask decomposition automation for SID-type SADP process and tested with a metal layer of industrial 22nm node standard cells and SRAM logic design. First, the minimum width and space of 22nm node standard cells are all 34nm, the etch bias per edge for mandrels is 8nm that means the minimum width of the core mask for the 1^{st} patterning could be 50nm (34nm+2×8nm). The minimum space of the core mask layout, the minimum width and space of the trim mask layout are all 50nm. The overlay margin of between the trim mask and the design intent is 10nm in our experiments.

Figure 16 shows the results of our SADP decomposition for 22nm node standard cells which are already finished their placement and routing design. As shown in Figure 16(a), the layout has multiple widths and spaces, and moreover the shape of the layout looks arbitrary so that the mask decomposition for SADP process looks challenging. Based on our layout coloring for SADP decomposition, we select the main mandrel by considering the trim mask layout and define the assist mandrel layout in Figure 16(b). After making the core layout with increased without any DRC violations, we shrink the core layout with the following etch step, and than generate the sidewall spacer pattern nearby the mandrel in (b). The trim mask pattering is followed by the BARC deposition in (c), then we can get the final patterning after some etch process in (d). As Figure 16(d) shows, the final metal patterns are slightly thicker than the target design due to the retargeting rule.

We also tested our SADP layout decomposition for Samsung 22nm node SRAM metal layer.In order to test 22nm SRAM design as in Figure 17, we scaled down a previous node design with a 0.5 scaling in the x-direction



(a) target layer (b) mandrel & spacer (c) trim mask (d) final patterns

Figure 16. SADP decomposition for $22nm$ node standard cells

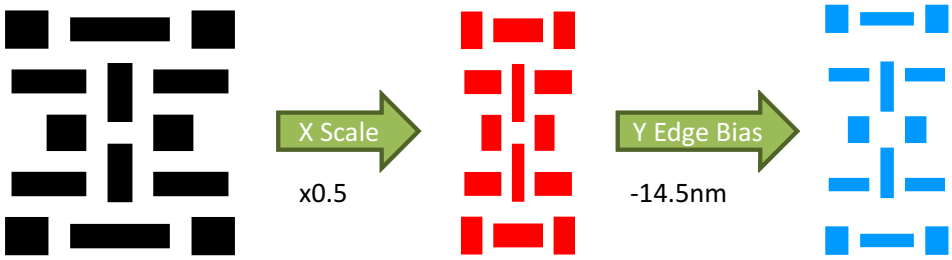


Figure 17. Layout migration

and with -14.5nm biasing in the y-direction. The SRAM layout can be labeled by the different functions of the circuitry as shown in Figure 18 [12]. The SRAM memory array has the most aggressive pitch, followed by the row and column decoders, and finally the random logic. The minimum width and space of the design intent are 31nm and 36nm, respectively. The etch bias per edge for mandrels and the overlay margin of the trim mask are all 4nm. The minimum width and space of the trim mask layout are 44nm and 44nm, respectively. The layout is decomposed across two masks.

Let us see the SADP results of SRAM memory array where a specific polygons are repeating in Figure 19. Based on our layout coloring engine, the layout was assigned into different colors by keeping the core mask design constraints in (b). The coloring engine analyzes the design intent and finds all critical spaces to be in the X direction, meaning that decomposition has to focus on this direction. Since nothing coloring conflicts were in the memory array, the trim mask was also generated without any mask rule violations in (c) and the final patterns was successively matched with the design intent in (d). The estimated final patterning was slightly different from the design intent because we applied metal retargeting for SADP flexibility since the width of sidewall spacer is usually constant.

Figure 20 shows the SADP decomposition on SRAM random logic where layout is irregular and shows more complex than the memory array. Results show the 1^{st} core mask which consists of main mandrel and assist mandrel layouts, and the 2^{nd} trim mask where most edges of the trim mask are placed on sidewall spacer areas. Since we just directly shrunk the previous node design to 22nm design, and the random logic has lots of complex layout shapes, some mask rule conflicts were detected in particular at the trim mask as shown in Figure 21(a). Meanwhile, the layout density of the random logic is relatively lower than the memory array so that designers can have enough room to modify the design target in order to make the design intent SADP compliant. Thus, we could modify and resolve any DRC conflicts using a post-processing step in Figure 21(b).

We also compared various approaches of the mandrel generation and evaluated lithographic printability using an industrial 22nm logic metal layer in Table 1: *Shorter* mandrels, *Longer* mandrels, and *Directional* mandrels. Eight layout blocks which have the same area ($20um \times 20um$) are evaluated. Our optical parameters are wavelength (λ) = 193nm, numerical aperture (NA) = 1.25 immersion lithography, and dipole illumination

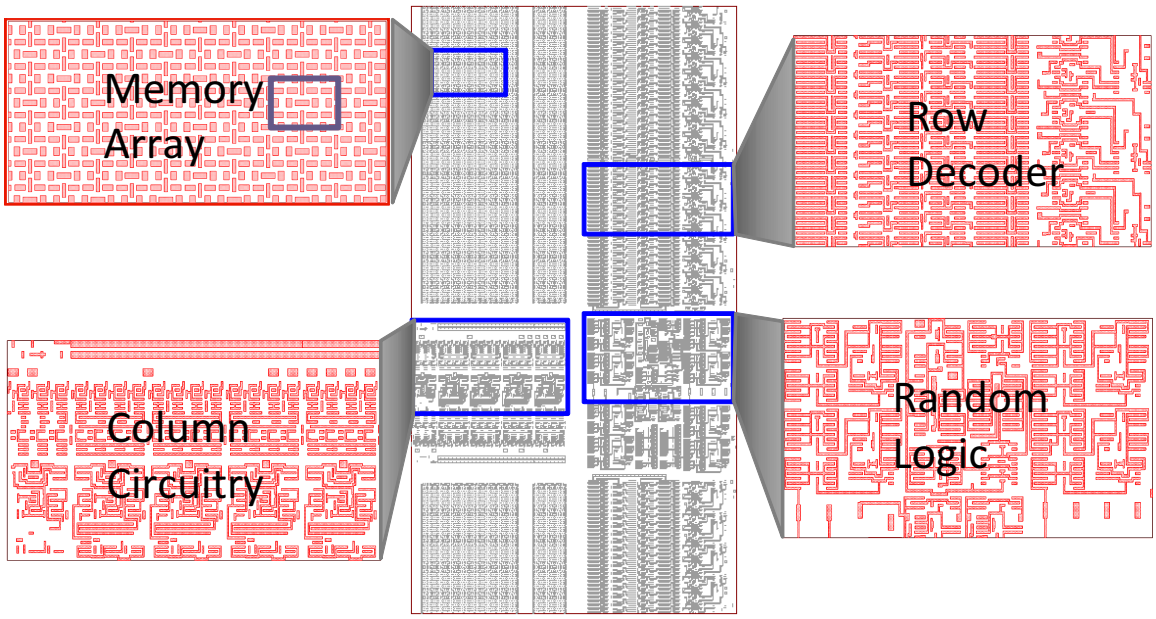
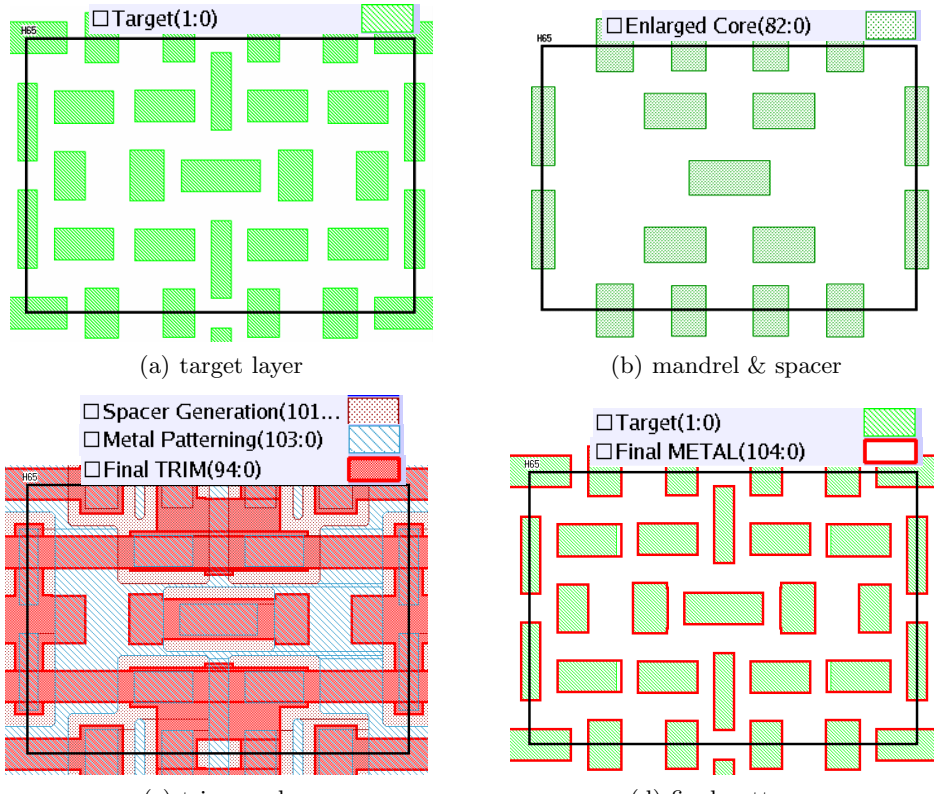


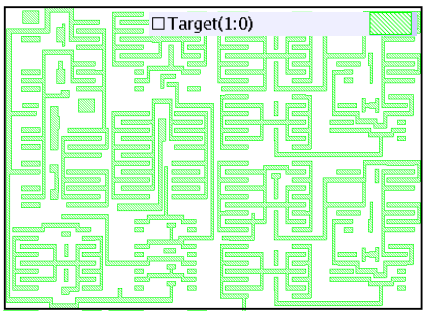
Figure 18. SADP mask decomposition for Samsung SRAM



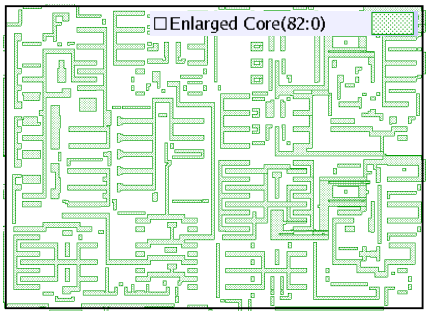
(a) target layer (b) mandrel & spacer

(c) trim mask (d) final patterns

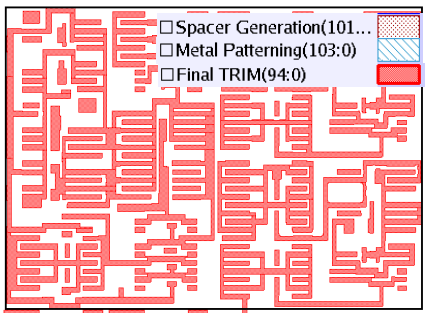
Figure 19. SADP layout decomposition on SRAM cell



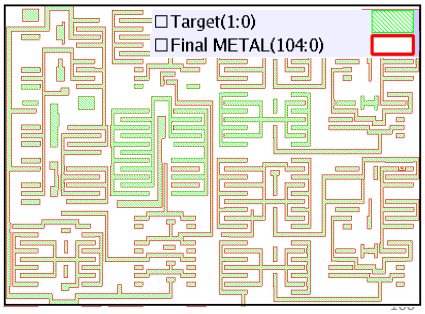
(a) target layer



(b) mandrel & spacer

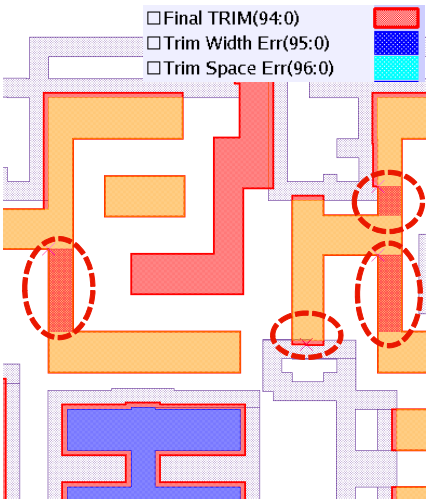


(c) trim mask

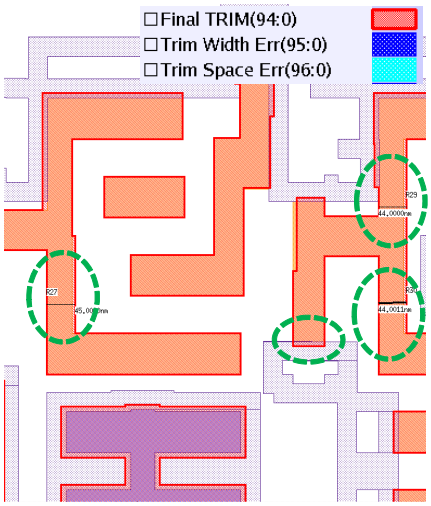


(d) final patterns

Figure 20. SADP layout decomposition on SRAM random logic



(a) pre-processing



(b) post-processing

Figure 21. Trim mask post-processing for SRAM random logic

$\sigma = 0.85/0.55$. Following industrial practice, we first perform full OPC for all mask layers and run lithography simulation with a process variation: focus $= \pm 50nm$. Then, we chose the nominal, the worst, and the best printed images for the given contact layer. For delay and current simulation, we set the nominal S/D resistance on 100Ω as defined in ITRS road-map for $32nm$ CMOS devices [13].

After perform OPC and lithography simulation, we calculate edge placement error (EPE) of the printed image. EPE is a popular metric to evaluate lithography printed image. It means the difference between

Table 1. Comparison of printability at the 1st core mask

Layout	Shorter			Longer			Directional		
	BF[a]	DF[a]		BF[a]	DF[a]		BF[a]	DF[a]	
	$3nm$ EPE[b]	$6nm$ EPE[b]	$Fail$[b]	$3nm$ EPE[b]	$6nm$ EPE[b]	$Fail$[b]	$3nm$ EPE[b]	$6nm$ EPE[b]	$Fail$[b]
Layout1	139	44	20	459	397	0	27	55	0
Layout2	216	54	3	669	593	1	15	52	0
Layout3	137	45	4	547	477	0	9	44	0
Layout4	111	68	0	502	473	0	9	70	0
Layout5	135	61	1	503	411	1	14	58	0
Layout6	138	71	2	536	438	2	15	66	0
Layout7	141	52	9	558	466	2	25	51	0
Layout8	91	39	1	451	401	0	5	40	0
average	139	54.3	5	528	457	0.8	14.9	54.5	0

[a] BF: at the best focus, DF: at the out focus variation
[b] $3nm$: 3nm<EPE, $8nm$: 8nm<EPE, F: patterning fail

resulting printed image and target design of an edge of layout. When we use *Longer* mandrels for the core mask, the patterning fail, in particular, missing of small island pattern, is decreased, yet the number of large EPE at the best focus and the out-focus condition is much larger compared to *Shorter*. Meanwhile when we applied *Directional* mandrels to the core mask, we achieved much smaller EPE variation without failing patterns.

6. CONCLUSION AND ONGOING WORKS

Several methods and options to produce manufacturable mask decompositions for sub-30nm metal random logic layouts with the SID style of SADP are shown. Our approaches for core and trim mask decomposition show the value of intelligent optimization methods in SID-type SADP lithography process. Experimental results with industry standard cell and SRAM designs show that the layout decomposition of SADP for 2D random layout is promising for the future lithography patterning if industries keep trying to reduce a process cost of SADP. For future work, we plan to study SADP-aware routing and the electrical impact of SADP variation.

7. ACKNOWLEDGEMENTS

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