

A Fast Simulation Framework for Full-chip Thermo-mechanical Stress and Reliability Analysis of Through-Silicon-Via based 3D ICs

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Abstract

In this work, we propose an efficient and accurate full-chip thermo-mechanical stress and reliability analysis framework. To the best of our knowledge this is the first such system which enables full-chip stress simulation as compared to existing commercial Finite Element Analysis (FEA) tools which can only simulate very small cross-sections at a time. Our approach is based on the linear superposition principle of stress tensors and the assumption that the stress field around a cylindrical TSV structure is symmetrically distributed. We compare the accuracy and run time of our simulation tool against the commercial FEA tool based on the number of TSVs under consideration. Our experimental results include stress maps produced by varying several parameters such as TSV liner material, size of the TSV landing pads and TSV dimensions. Finally, we also demonstrate our experimental results by simulating a full chip layout and varying the above parameters as well as by varying the chip operating temperature distribution.

I. Introduction

Due to the coefficients of thermal expansion (CTE) mismatch between a TSV fill material such as copper (Cu) and silicon substrate, thermo-mechanical stress is induced during fabrication process and thermal cycling of TSV structures, which can affect device performance [1] or drive crack growth in 3D interconnects [2], [3]. Most previous works focused on modeling the thermo-mechanical stress and reliability of a single TSV in isolation. These simulations are performed using FEA methods which are computationally expensive or infeasible for full-chip analysis. Furthermore, some works used unrealistic TSV structures such as an extremely large landing pad (LP), mainly because the design context is not considered.

Even though there are several works on thermo-mechanical reliability issues induced by TSV stress, this is the first work addressing TSV thermo-mechanical stress and reliability issues on a full-chip scale to the best of our knowledge. In this paper, we propose a TSV thermo-mechanical stress and reliability analysis flow on a full-chip scale. We use von Mises yield criterion as a mechanical reliability metric, and demonstrate the capabilities of our simulation framework by showing the impacts of design parameters such as TSV size, landing pad size and liner thickness size on the mechanical reliability.

The main contributions of this work include the following: (1) Modeling: Compared with existing work, we simulate more detailed and realistic TSV structures and study their impact

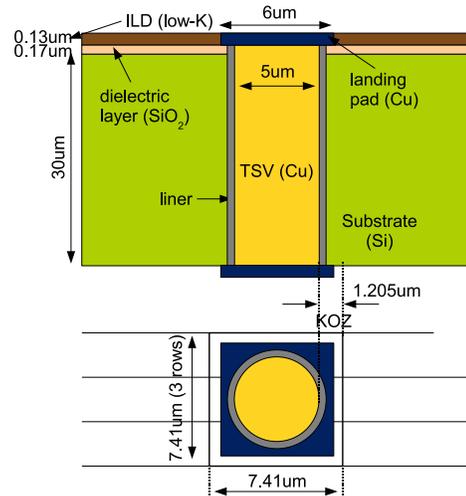


Fig. 1. Baseline TSV structure. TSV cell that occupies 3 standard cell rows with Keep-out-zone of 1.205 μm .

TABLE I. Material properties

Material	CTE (ppm/K)	Young's modulus (GPa)	Poisson's ratio
Cu	17	110	0.35
Si	2.3	130	0.28
SiO ₂	0.5	71	0.16
Low K	20	9.5	0.3
BCB	40	3	0.34

on stress as well as mechanical reliability metric. We also model the impact of chip operating temperature on stress and reliability. (2) Full-chip analysis: We, for the first time, validate the principle of linear superposition of stress tensors against FEA simulations, and apply this methodology to generate a stress map and a reliability metric map on a full-chip scale. We demonstrate the feasibility of our framework by comparing our simulation results versus a commercial FEA based tool ABAQUS in terms of run time and simulation accuracy.

II. Realistic TSV Stress Modeling

The analytical 2D radial stress model, known as *Lamé* stress solution, was employed to address the TSV thermo-mechanical stress effect on device performance in [1]. Even though this closed-form formula is easy to handle, it does not capture the 3D nature of a stress field near a wafer surface around TSVs where devices are located [3]. Moreover, the

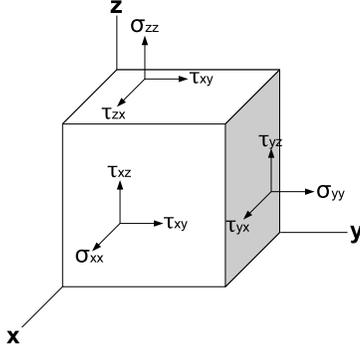


Fig. 2. Cartesian representation of stress tensor components

TSV/substrate interface region near the wafer surface is known to be a highly problematic area for mechanical reliability [3]. In our study, wafer surface means the silicon surface right below substrate(Si)/dielectric layer(SiO₂) interface, where device resides.

Though the authors in [3] proposed a semi-analytic 3D stress model, it is only valid for a TSV with a high aspect ratio. Furthermore, since their model is only applicable to a single TSV in isolation and their TSV structure only includes TSV and silicon substrate, it cannot be directly used to assess mechanical reliability issues in a full-chip scale as well as a TSV which contains a landing pad and a dielectric liner because of the change in boundary conditions.

A. 3D FEA Simulation

Since there is no known analytical stress model for a realistic TSV structure, 3D FEA models for a TSV structure are created to investigate the stress distribution near wafer surface. To realistically examine the thermo-mechanical stress induced by TSVs, our baseline simulation structure of a TSV is based on the fabricated and the published data [4], as shown in Figure 1. Our baseline TSV occupies three standard cell rows in 45 nm technology. We define 1.205 μm from TSV edge as keep-out-zone (KOZ) in which no cell is allowed to be placed. Our baseline TSV diameter, height, landing pad size, and liner thickness are 5 μm, 30 μm, 6 μm, and 125 nm, respectively, unless specified, which are close to the data in [4]. We use SiO₂ as a baseline liner material, and ignore Cu diffusion barrier material such as Ta and Ti in these experiments since this barrier thickness is negligible compared to SiO₂ liner, hence its impact on stress distribution is negligible. Material properties used in our simulations are shown in Table I.

Before discussing the detailed stress modeling results, we introduce the concept of a stress tensor. Figure 2 illustrates the components of the stress tensor in the Cartesian coordinate system. Stress at a point in an object can be defined by the nine-component stress tensor:

$$S = \begin{bmatrix} \sigma_{11} & \tau_{12} & \tau_{13} \\ \tau_{21} & \sigma_{22} & \tau_{23} \\ \tau_{31} & \tau_{32} & \sigma_{33} \end{bmatrix}$$

The first index i indicates that the stress acts on a plane normal to the axis, and the second index j denotes the direction

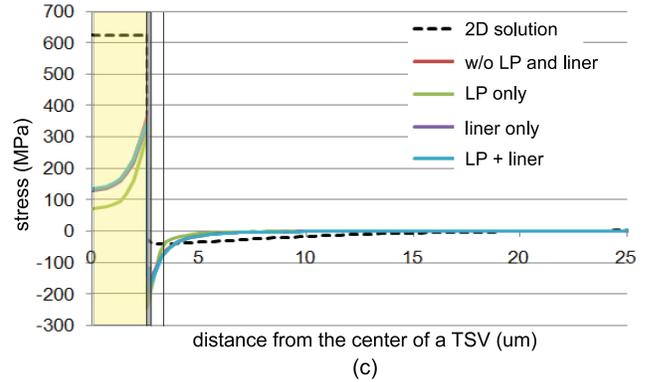
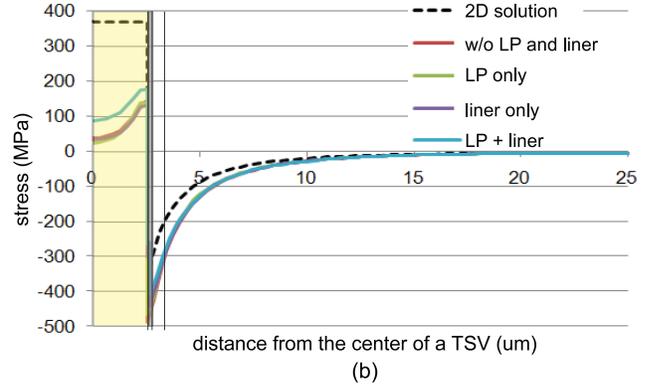
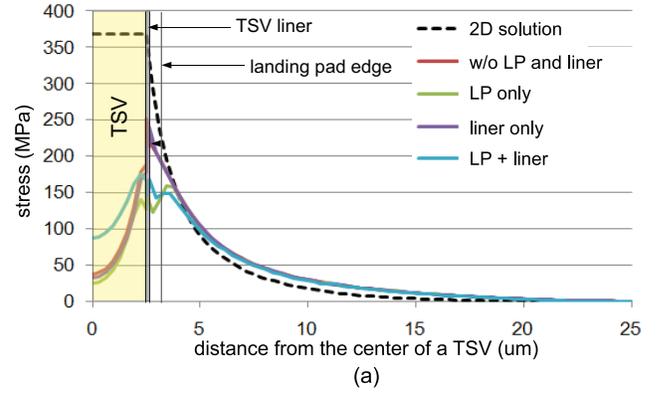


Fig. 3. Effect of TSV structures on normal stress components. (a) σ_{rr} stress. (b) $\sigma_{\theta\theta}$ stress. (c) σ_{zz} stress.

in which the stress acts. If index i and j are same we call this a normal stress, otherwise a shear stress. Since we adopt a cylindrical polar coordinate system in this modeling, index 1, 2, and 3 represent r , θ , and z , respectively.

B. Impact of TSV Liner and Landing Pad

Figure 3 shows FEA simulation results of a normal stress components along an arbitrary radial line from the TSV center at the wafer surface with -250°C of thermal load. That is, we assume TSV structure is annealed at 275°C and cooled down to 25°C to mimic the manufacturing process [3], [5], [6]. We also assume that the entire TSV structure is stress free at the annealing temperature. We first observe the huge discrepancy

between 2D solution and 3D stress results at the TSV edge as well as inside TSV in all normal stress components. It is widely known that most of mechanical reliability failures occur at the interface between different materials. Therefore, 2D solution does not predict mechanical failure mechanism for TSVs correctly. Also, SiO₂ liner, which acts as a stress buffer layer, reduces σ_{rr} stress at the TSV edge by 35 MPa compared with the case without landing pad and liner. The landing pad also helps decrease stress magnitude of σ_{rr} at the TSV edge. The magnitude of $\sigma_{\theta\theta}$ stress and σ_{zz} increases inside TSV, but decreases outside the TSV edge when SiO₂ liner and/or landing pad are introduced.

It is evident from these experiments that modeling stress distribution considering surrounding structures such as a liner and a landing pad is important to analyze the thermo-mechanical stress around TSVs more accurately.

III. Full-Chip Reliability Analysis

FEA simulation involves decomposition of structures into domains of disjoint polygons. These disjoint polygons are used in the formation of the member element functions represented by partial differential equations. They are then assembled and solved by a system of linear equations. FEA simulation of thermo-mechanical stress for multiple TSVs require huge computing resources and time, thus it is not suitable for full-chip analysis. In this section, we present full-chip stress and reliability analysis flow. To enable a full-chip stress analysis, we first explore the principle of linear superposition of stress tensors from individual TSVs. Based on the linear superposition method, we build full-chip stress map. Then from this full-chip stress map, we compute von Mises yield metric to predict mechanical reliability problems in 3D ICs.

A. Linear Superposition Principle

An extremely useful principle in the analysis of linearly elastic structures is that of superposition. The principle states that if the displacements at all points in an elastic body are proportional to the forces producing them, that is the body is linearly elastic, the effect (i.e. stresses and displacements) on such a body of a number of forces acting simultaneously is the sum of the effects of the forces applied separately. We apply this principle to compute the stress at a point by simply adding the individual stress tensors at that point due to each TSV as follows:

$$S = \sum_{i=1}^n S_i \quad (1)$$

where S is the total stress at the point under consideration and S_i is the individual stress tensor at this point due to the i^{th} TSV.

B. Stress Analysis with Multiple TSVs

First, based on the observation that the stress field of a single TSV in isolation is radially symmetrical due to the cylindrical shape of a TSV, we obtain stress distribution around a TSV from a set of stress tensors along an arbitrary radial line from the TSV center in a cylindrical coordinate system. To evaluate a stress tensor at a point affected by multiple TSVs, a conversion of a stress tensor to a Cartesian coordinate

system is required. This is due to the fact that we extract stress tensors from a TSV whose center is the origin in the cylindrical coordinate system; hence we cannot perform a vector sum of stress tensors at a point from each TSV which has a different center location. Then, we compute a stress tensor at the point of interest by adding up stress tensors from TSVs affecting this point. We set a TSV stress influence zone as 25 μm from the center of a TSV, since the magnitude of stress components becomes negligible beyond this distance.

Let the stress tensor in Cartesian and cylindrical coordinate system be S_{xyz} and $S_{r\theta z}$, respectively.

$$S_{xyz} = \begin{bmatrix} \sigma_{xx} & \tau_{xy} & \tau_{xz} \\ \tau_{yx} & \sigma_{yy} & \tau_{yz} \\ \tau_{zx} & \tau_{zy} & \sigma_{zz} \end{bmatrix}, S_{r\theta z} = \begin{bmatrix} \sigma_{rr} & \tau_{r\theta} & \tau_{rz} \\ \tau_{\theta r} & \sigma_{\theta\theta} & \tau_{\theta z} \\ \tau_{zr} & \tau_{z\theta} & \sigma_{zz} \end{bmatrix}$$

The transform matrix Q is the form:

$$Q = \begin{bmatrix} \cos \theta & -\sin \theta & 0 \\ \sin \theta & \cos \theta & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

where, θ is the angle between the x-axis and a line from the TSV center to the simulation point. A stress tensor in a cylindrical coordinate system can be converted to a Cartesian coordinate system using conversion matrices: $S_{xyz} = QS_{r\theta z}Q^T$

C. Mechanical Reliability Analysis

In order to evaluate if computed stresses indicate possible reliability concerns, a critical value for a potential mechanical failure must be chosen. The von Mises yield criterion is known to be one of the most widely used mechanical reliability metric [7]. If the von Mises stress exceeds a yielding strength, material yielding starts. Prior to the yielding strength, the material will deform elastically and will return to its original shape when the applied stress is removed. However, if the von Mises stress exceeds the yield point, some fraction of the deformation will be permanent and non-reversible.

There is a large variation of yield strength of Cu in the literature, from 225 MPa to 600 MPa, and it has been reported to depend upon thickness, grain size, and temperature [7]. We use 600 MPa as a Cu yielding strength in our experiments. The yield strength of silicon is 7000 MPa, which will not be reliability concerns for the von Mises yield criterion.

The von Mises stress is a scalar value at a point that can be computed using components of a stress tensor shown in Equation (2). By evaluating von Mises stress at the interface between a TSV and a liner, where highest von Mises stress occurs, we can predict mechanical failures in TSVs.

Our full-chip stress and reliability analysis flow is shown in figure 4. We first perform a detailed FEA simulation of a single TSV and provide the stress distribution along a radial line from the center of the TSV as input to our simulation engine. We also provide the locations of the TSVs from 3D IC layout along with a thermal map to the simulation engine. If TSV locations are not provided, the tool may generate user-defined regularly distributed TSV placements for analysis. A

$$\sigma_v = \sqrt{\frac{(\sigma_{xx} - \sigma_{yy})^2 + (\sigma_{yy} - \sigma_{zz})^2 + (\sigma_{zz} - \sigma_{xx})^2 + 6(\sigma_{xy}^2 + \sigma_{yz}^2 + \sigma_{zx}^2)}{2}} \quad (2)$$

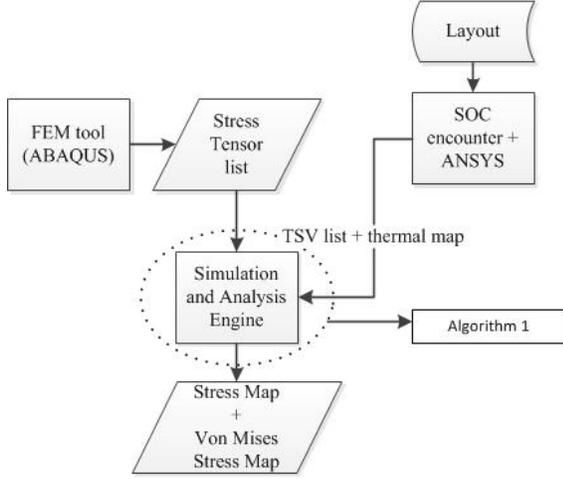


Fig. 4. Simulation Flow

study of the impact of TSV orientations are also available within the tool.

The basic algorithm for generating stress and reliability maps is illustrated in algorithm 1. We first start to find a stress influence zone from each TSV. Then, we associate the points in the influence zone with the affecting TSV. Next, for each simulation point under consideration, we look up the stress tensor from the TSV found in the association step, and use the coordinate conversion matrices to obtain stress tensors in the Cartesian coordinate system. We visit an individual TSV affecting this simulation point and add up their stress contributions. Once we finish the stress computation at a point, we obtain the von Mises stress value using Equation (2). The complexity of this algorithm is $O(n)$, where n is number of simulation points.

IV. Simulation Results

We implement a TSV-aware full-chip stress and reliability analysis flow in JAVA and C++. In the following experiments we observe the impact of several TSV components and TSV orientation on the von Mises reliability metric. Also, we investigate the impact of chip operating temperature on the reliability. Before discussing these simulation results, we first show the efficiency and accuracy of our linear superposition method compared with FEA simulations.

A. Validation of Linear Superposition Method

We validate the linear superposition of stress tensors against FEA simulations by varying the number of TSVs and their arrangement. Table II shows some of our comparisons. First, we observe huge run time reduction in our linear superposition method. Note that we perform FEA simulations using 4 CPUs while only one CPU is used for our linear superposition method. Even though our linear superposition

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input : TSV list  $T$ , stress library, thermal map (optional)
output: stress map, von Mises stress map
if  $T$  is empty then
     $n \leftarrow$  (user specified number of TSVs)
     $l \leftarrow$  (user specified chip length)
     $w \leftarrow$  (user specified chip width)
     $p \leftarrow$  (user specified TSV pitch)
     $P \leftarrow$  GenerateTSVPlacements( $n, l, w, p$ )
end
else
     $P \leftarrow T$ 
end
for each  $T$  in  $P$  do
    for each TSV  $t$  in  $T$  do
         $c \leftarrow$  center of  $t$ 
         $r \leftarrow$  FindStressInfluenceZone( $c$ )
        for each point  $r'$  in  $r$  do
             $r'.TSV \leftarrow t$ 
        end
    end
    for each simulation point  $p$  do
        if  $p.TSV \neq \emptyset$  then
            for each  $t \in p.TSV$  do
                 $d \leftarrow$  distance( $t, p$ )
                 $S_{cyl} \leftarrow$ 
                    FindStressTensor( $d, temperature$ )
                 $\theta \leftarrow$  FindAngle( $line\ tp, x\ axis$ )
                 $Q \leftarrow$  SetConversionMatrix( $\theta$ )
                 $S_{Cart} \leftarrow Q S_{cyl} Q^T$ 
                 $p.S_{Cart} \leftarrow p.S_{Cart} + S_{Cart}$ 
            end
        end
         $vonMises(p) \leftarrow$  ComputeVonMises( $p.S_{Cart}$ )
        if  $vonMises(p) \geq violationThreshold$  then
            incrementViolationCount( $T$ )
        end
    end
end
    
```

Algorithm 1: Full-chip Stress and Reliability Analysis Flow

method performs stress analysis on a 2D plane at the wafer surface, whereas FEA simulation is performed on entire 3D structure, we can perform stress analysis for other planes in a similar way if needed. Also, run time in our linear superposition method shows linear dependency on simulation points, which is directly related to number of TSVs under consideration. Thus, our linear superposition method is highly scalable, hence applicable to full-chip scale stress simulations. Most importantly, error between FEA simulations and the linear superposition method is practically negligible. Results show that our linear superposition method overestimates stress

TABLE II. Comparison between FEA simulations and linear superposition method

# TSV	FEA		linear superposition		max % error	
	# node	run time	# sim' point	run time	inside TSV	outside TSV
1	148K	20m10s	1M	20.83s	1.1	-0.5
2	272K	55m40s	1.2M	26.05s	3.2	-0.8
3	343K	1h24m45s	1.44M	36.73s	5	-1.2
5	521K	1h54m25s	1.68M	55.27s	13.2	-1.9
10	1074K	4h25m55s	2.24M	64.13s	13.7	-2.1

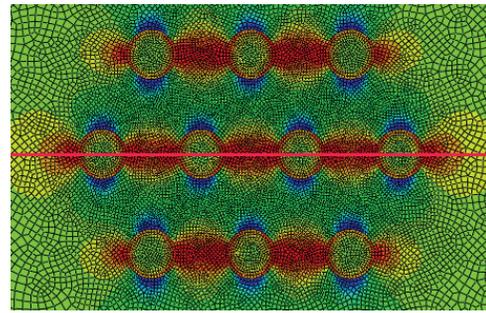
magnitude inside TSV. Even though we use linear elastic model for whole structure, it is possible that due to the difference in material property between TSV and substrate, stress effect induced by nearby TSVs acting on the TSV under consideration could be different between inside and outside TSV. However, though maximum % error inside TSV of 10 TSVs case is as high as 13.7 %, stress magnitude difference between FEA and our method is only 5.1 MPa. Also, since most mechanical problem occurs at the interface between different materials, this error does not pose a serious impact on our reliability analysis. Figure 5 shows the stress map of σ_{xx} component for one of test cases which contains 10 TSVs, and it clearly shows our linear superposition method matches well with the FEA simulation result.

B. Impact of TSV components on Reliability

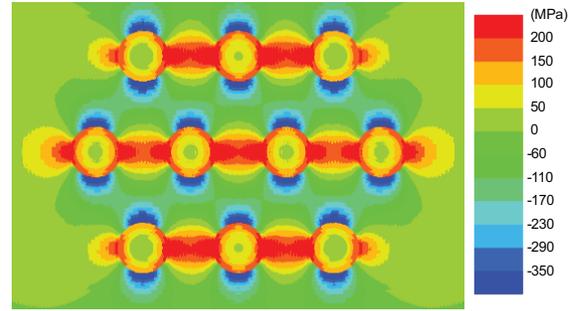
For each of the following studies we studied the impact of a single TSV component at a time by varying the number of TSVs. We ran simulations for 10, 100, 1000 and 10000 TSVs. We first study the effect of liner material on von Mises stress. We choose a TSV pitch of $15 \mu\text{m}$ and liner thickness of 125nm for this study. We identify that the type of liner material has a huge impact on the von Mises stress magnitude, since the liner effectively absorbs thermo-mechanical stress at the TSV/liner interface. Especially, the BCB liner shows significant reduction in the maximum von Mises stress due to the extremely low Young's modulus shown in Table I. Figure 6 (a), (b), and (c) show von Mises stress maps of 100 TSVs with no liner, SiO_2 liner, and BCB liner, respectively, which shows the impact of liner material graphically.

We next compare the maximum von Mises stress with two different landing pad sizes $6 \times 6 \mu\text{m}^2$ and $8 \times 8 \mu\text{m}^2$ respectively. It is observed that increasing the landing pad size does not improve von Mises stress significantly. This is because only the magnitude of σ_{rr} stress component at the TSV/liner interface is reduced due to Cu landing pad, while other stress components such as $\sigma_{\theta\theta}$ and σ_{zz} show increase in stress magnitude shown in Figure 3.

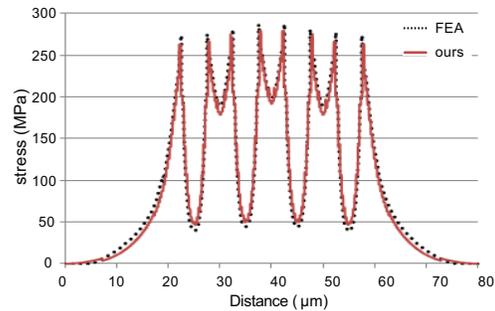
We next choose three different TSV dimensions; the small TSV type corresponding to a landing pad size of $3.5 \times 3.5 \mu\text{m}^2$, diameter of $2.5 \mu\text{m}$, and pitch of $7.5 \mu\text{m}$; the medium TSV type corresponding to a landing pad size of $6 \times 6 \mu\text{m}^2$, diameter of $5 \mu\text{m}$, and pitch of $15 \mu\text{m}$; and the large TSV type corresponding to a landing pad size of $11 \times 11 \mu\text{m}^2$, diameter of $10 \mu\text{m}$, and pitch of $15 \mu\text{m}$. We set the landing pad width to be $1 \mu\text{m}$ larger than the corresponding TSV diameter, and use a 125nm thick SiO_2 liner for all cases for fair comparisons. It is observed that the TSVs with the smaller diameter are



(a)



(b)



(c)

Fig. 5. Sample stress comparison between FEA simulation and linear superposition method. (a) FEA result (σ_{xx}). (b) ours (σ_{xx}). (c) FEA vs. ours (σ_{xx}) along the white line in (a).

benefited because the magnitude of normal stress components decay proportional to $(D/2r)^2$, where D is the TSV diameter and r is the distance from the TSV center.

All of the above results are summarized in Figure 7 with representative 1000 TSVs case. We observe that employing BCB liner and small TSV size improve the mechanical reliability in TSV based 3D ICs.

C. Impact of TSV pitch

We also observe the effect of TSV pitch on von Mises stress. We place TSVs regularly on $1 \times 1 \text{mm}^2$ chip. We use 1600, 2500, 4356, and 10000 TSVs whose pitch are 25, 20, 15, and $10 \mu\text{m}$, respectively. We obtain two data sets; one without landing pad and liner; and one with a landing pad of size $6 \times 6 \mu\text{m}^2$ and BCB liner with thickness 125nm . The von Mises stress reduces with increasing pitch and the layout using TSVs

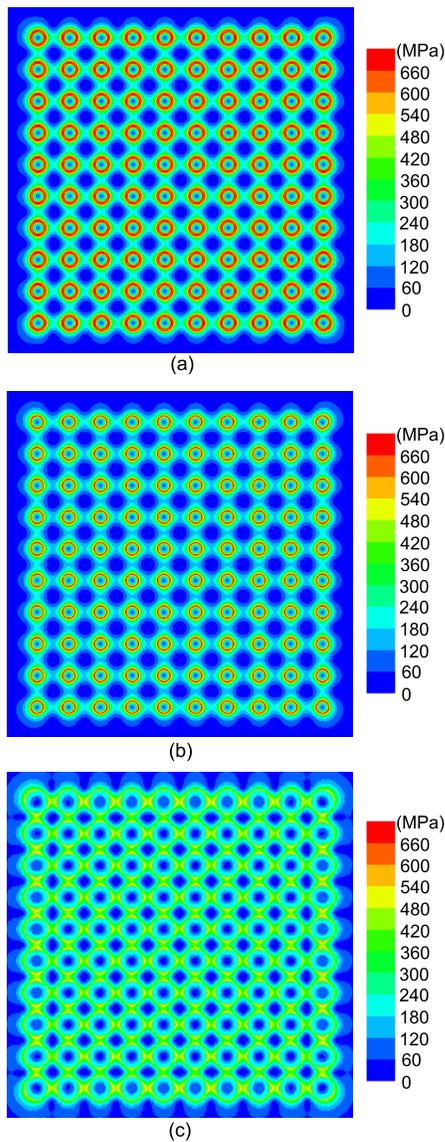


Fig. 6. Von Mises Stress map of regularly placed 100 TSVs with 15 μm pitch. (a) no liner (b) SiO_2 liner (c) BCB liner

with a landing pad and BCB liner shows lower von Mises stress as shown in Figure 8.

D. Impact of relative TSV orientation

We also study the impact of relative orientations of TSVs on reliability. Figure 9 illustrates our simulation structures. We keep TSV1 and TSV3 at fixed locations with 20 μm pitch and rotate TSV2 around TSV1 with a radius of 10 μm , and we monitor maximum von Mises stress in TSV1 shown in Figure 10. We observe that the maximum von Mises stress in TSV1 occurs when the angle between TSV3, TSV1 and TSV2 is 0° shown in Figure 9 (a). This is because of the constructive interference of stress components from all three TSVs. Also, since both TSV2 and TSV3 are in the right side of TSV1, net

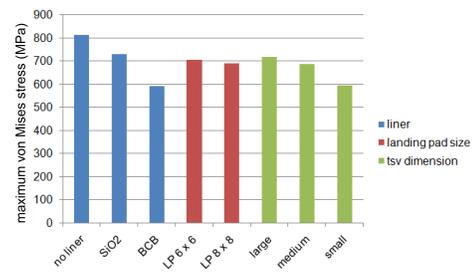


Fig. 7. Impact of liner material, landing pad size, and TSV dimensions on maximum von Mises stress with 1000 TSVs considered

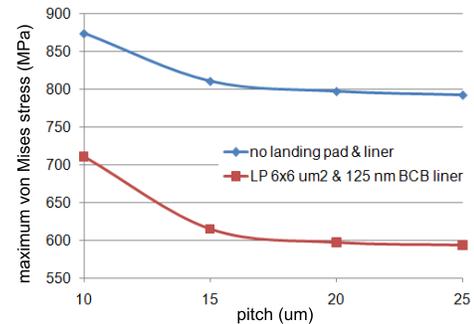


Fig. 8. Impact of TSV pitch on maximum von Mises stress

effect of additive stress is maximum at the right side of TSV1 edge. This is why von Mises stress is higher in the case of 0° than that of 180° . The maximum von Mises stress at TSV1 is observed to be minimum when the angle between TSV3, TSV1 and TSV2 is 90° shown in Figure 9 (c). This is because tensile and compressive stresses of TSV2 and TSV3 at TSV1 are normal to each other and hence destructive interference occurs. These relative TSV orientation study can be potentially applied to mechanical reliability-aware TSV placement optimization.

E. Impact of Chip Operating Temperature

Up to this point, we only consider the residual stress caused by the manufacturing process, i.e. from annealing to cooling process. In this section, we examine the reliability problem during a chip operation phase. We generate a power map using SoC Encounter, and feed this to ANSYS Fluent with in-house add-ons which enables a steady-state thermal analysis for GDSII level 3D ICs shown in Figure 11 (b). Depending on the temperature distribution across the die area, each TSV experiences a different thermal load. Thus, the significance of the mechanical reliability problems of an individual TSV might be different from each other.

We designed a circuit with regularly placed 1472 TSVs whose pitch is 20 μm for this experiment shown in Figure 11 (a). We use a 500 nm thick BCB liner for this experiment. Figure 11 (c) and (d) are close-up shots of von Mises stress map of the hot and the cool spot in this die, respectively. The cool spot experiences higher von Mises stress, since the temperature difference from the stress free temperature, 275°C in our case, is larger in the cool spot than in the hot spot.

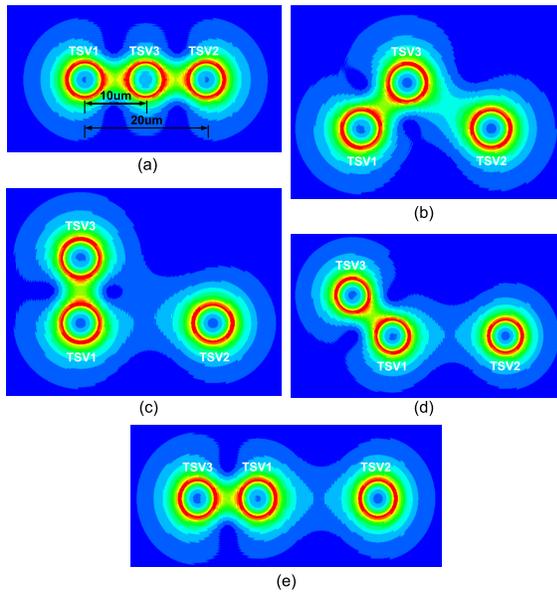


Fig. 9. TSV orientation impact on von Mises stress. TSV1 and TSV2 are located in fixed position with $20 \mu m$ pitch. TSV3 is rotating around TSV1 with $10 \mu m$ pitch. Angle is between TSV1 and TSV3. (a) $\theta = 0^\circ$ (b) $\theta = 45^\circ$ (c) $\theta = 90^\circ$ (d) $\theta = 135^\circ$ (e) $\theta = 180^\circ$

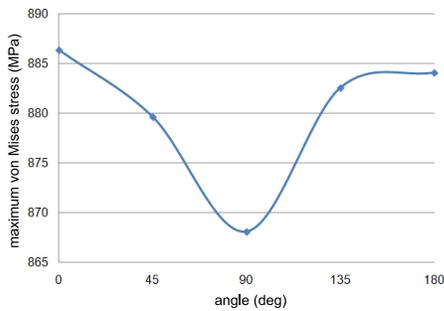


Fig. 10. Impact of TSV orientation on maximum Von Mises stress at TSV1 by rotating TSV3 around TSV1.

However, since the maximum temperature difference across the die is only $20^\circ C$, the impact of an operating temperature to the TSV reliability across the die is not significant. In our test case, the difference of the maximum von Mises stress between two spots is 31.8 MPa . Also, both the hot and the cool spot experiences less maximum von Mises stress compared to the residual stress case, again due to the reduced thermal load. However, the reduction of von Mises stress during a chip operation cannot recover the material yielding failure if it already exists, since this is a non-reversible failure mechanism.

V. Conclusions

In this work, we present a fast and accurate full-chip stress and mechanical reliability analysis flow. We show how TSV structures affect stress field and a mechanical reliability in 3D ICs. This full-chip stress and mechanical reliability analysis capability can be applicable to placement optimization for 3D

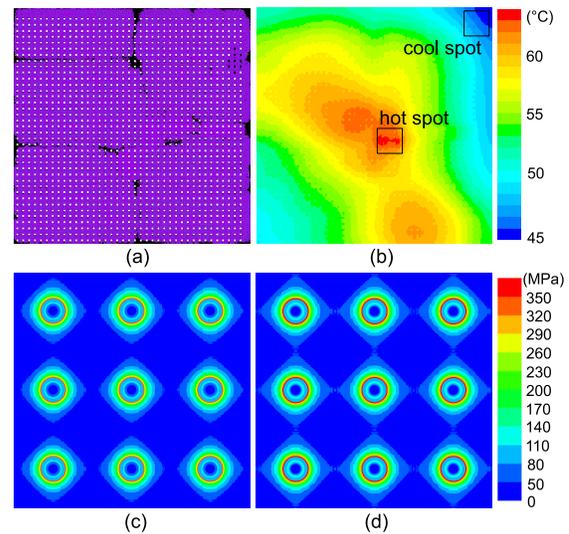


Fig. 11. Impact of operating temperature on von Mises stress. (a) layout of test circuit. TSV landing pads are white rectangles. (b) thermal map. (c) von Mises stress in the hot spot. (d) von Mises stress in the cool spot.

ICs. Our results show that TSV size, liner material, and TSV placement are key design parameters to reduce the mechanical reliability problems in TSV based 3D ICs.

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