TSV Stress-aware Full-Chip Mechanical Reliability Analysis and Optimization for 3D IC

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ABSTRACT

In this work, we propose an efficient and accurate full-chip thermo-mechanical stress and reliability analysis tool and design optimization methodology to alleviate mechanical reliability issues in 3D ICs. First, we analyze detailed thermo-mechanical stress induced by TSVs in conjunction with various associated structures such as landing pad and dielectric liner. Then, we explore and validate the use of the linear superposition principle of stress tensors and demonstrate the accuracy of this method against detailed finite element analysis (FEA) simulations. Next, we apply this linear superposition method to full-chip stress simulation and a reliability metric named the von Mises yield criterion. Finally, we propose a design optimization methodology to mitigate the mechanical reliability problems in 3D ICs. Our experimental results demonstrate the effectiveness of our methodology.

Categories and Subject Descriptors

B.7.2 [**Hardware, Integrated Circuit**]: Design Aids

General Terms

Design

Keywords

3D IC, TSV, stress, mechanical reliability

1. INTRODUCTION

Due to the coefficients of thermal expansion (CTE) mismatch between a TSV fill material such as copper (Cu) and silicon substrate, thermo-mechanical stress is induced during fabrication process and thermal cycling of TSV structures, which can affect device performance [7] or drive crack growth in 3D interconnects [4, 6]. Most previous works focused on modeling the thermo-mechanical stress and reliability of a single TSV in isolation. These simulations are performed using FEA methods which are computationally expensive or infeasible for full-chip analysis. Furthermore, some works used unrealistic TSV structures such as an extremely large landing pad (LP), mainly because the design context is not considered.

Even though there are several works on thermo-mechanical reliability issues induced by TSV stress, this is the first work addressing TSV thermo-mechanical stress and reliability issues on a full-chip scale to the best of our knowledge. In this paper, we propose a TSV thermo-mechanical stress and reliability analysis flow as well as a design optimization methodology to reduce mechanical reliability problems in TSV based 3D ICs. We use von Mises yield criterion as a mechanical reliability metric, and show impacts of design parameters such as TSV size, landing pad size, liner thickness and keep-out-zone (KOZ) size on the mechanical reliability.

The main contributions of this work include the following: (1) Modeling: Compared with existing works, we simulate more detailed and realistic TSV structures and study their impact on stress as well as a mechanical reliability metric. We also model the impact of chip operating temperature on stress and reliability. (2) Full-chip analysis: We, for the first time, validate the principle of linear superposition of stress tensors against FEA simulations, and apply this methodology to generate a stress map and a reliability metric map on a full-chip scale. (3) Design optimization: We present design methods to reduce von Mises stress, which is a mechanical reliability metric, on full-chip 3D IC designs by tuning design parameters such as landing pad size, liner thickness, KOZ size, and TSV placement.

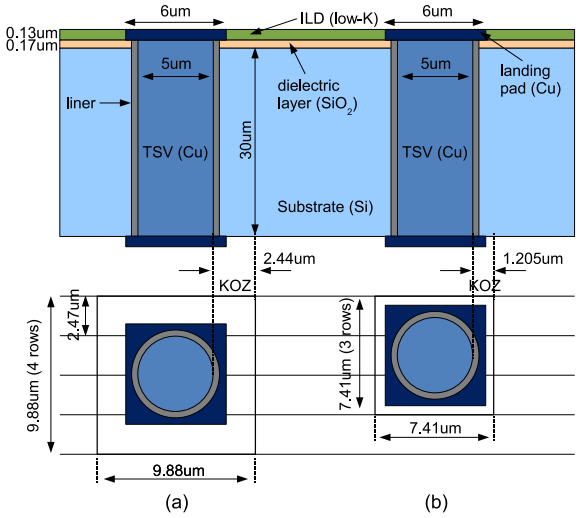

Figure 1: Baseline TSV structure. (a) 4X TSV cell that occupies 4 standard cell rows (KOZ = 2.44 μm). (b) 3X TSV cell (KOZ = 1.205 μm).

2. DETAILED BASELINE MODELING

The analytical 2D radial stress model, known as *Lamé* stress solution, was employed to address the TSV thermo-mechanical stress effect on device performance in [7]. Even though this closed-form formula is easy to handle, it does not capture the 3D nature of a stress field near a wafer surface around TSVs where devices are located [6]. Moreover, the TSV/substrate interface region near the wafer surface is known to be a highly problematic area for mechan-

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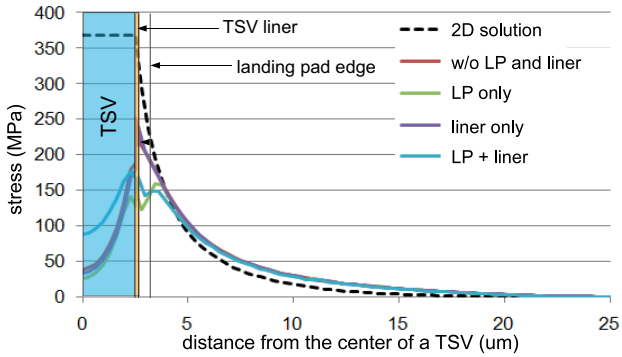

Figure 2: Effect of TSV structures on σ_{rr} stress.

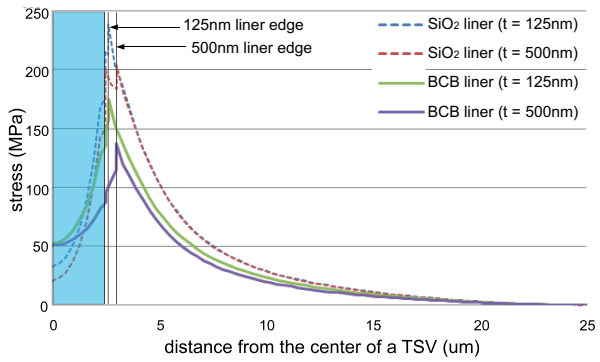

Figure 3: Effect of liner material/thickness on σ_{rr} stress.

ical reliability [6]. In our study, wafer surface means the silicon surface right below substrate (Si)/dielectric layer (SiO_2) interface.

Though the authors in [6] proposed a semi-analytic 3D stress model, it is only valid for a TSV with a high aspect ratio. Furthermore, since their model is only applicable to a single TSV in isolation and their TSV structure only includes TSV and silicon substrate, it cannot be directly used to assess mechanical reliability issues in a full-chip scale as well as a TSV which contains a landing pad and a dielectric liner because of the change in boundary conditions.

2.1 3D FEA Simulation

Since there is no known analytical stress model for a realistic TSV structure, 3D FEA models for a TSV structure are created to investigate the stress distribution near wafer surface. To realistically examine the thermo-mechanical stress induced by TSVs, our baseline simulation structure of a TSV is based on the fabricated and the published data [1], as shown in Figure 1. We construct two TSV cells, i.e. 4X TSV and 3X TSV, which occupy four and three standard cell rows in 45 nm technology. We define 2.44 μm and 1.205 μm from TSV edge as keep-out-zone (KOZ) in which no cell is allowed to be placed for TSV 4X and TSV 3X cells, respectively. Our baseline TSV diameter, height, landing pad size, and liner thickness are 5 μm, 30 μm, 6 μm, and 125 nm, respectively, unless specified, which are close to the data in [1]. We use SiO_2 as a baseline liner material, and ignore Cu diffusion barrier material such as Ta and Ti in these experiments since this barrier thickness is negligible compared to SiO_2 liner, hence its impact on stress distribution is negligible. Material properties used for our experiments are as follows: CTE (ppm/K) for Cu = 17, Si = 2.3, SiO_2 = 0.5, and BCB = 40; Young's modulus (GPa) for Cu = 110, Si = 130, SiO_2 = 71, and BCB = 3. We use the FEA simulation tool ABAQUS to perform experiments, and all materials are assumed to be linear elastic.

Before discussing the detailed stress modeling results, we introduce the concept of a stress tensor. Stress at a point in an object can be defined by the nine-component stress tensor:

$$\sigma = \sigma_{ij} = \begin{bmatrix} \sigma_{11} & \sigma_{12} & \sigma_{13} \\ \sigma_{21} & \sigma_{22} & \sigma_{23} \\ \sigma_{31} & \sigma_{32} & \sigma_{33} \end{bmatrix}$$

The first index i indicates that the stress acts on a plane normal to the axis, and the second index j denotes the direction in which the stress acts. If index i and j are same we call this a normal stress, otherwise a shear stress. Since we adopt a cylindrical coordinate system in this modeling, index 1, 2, and 3 represent r, θ, and z, respectively.

2.2 Impact of TSV Liner and Landing Pad

Figure 2 shows FEA simulation results of a normal stress component σ_{rr} along an arbitrary radial line from the TSV center at the wafer surface with -250°C of thermal load. That is, we assume TSV structure is annealed at 275°C and cooled down to 25°C to mimic the manufacturing process [2, 5, 6]. We also assume that the entire TSV structure is stress free at the annealing temperature. We first observe the huge discrepancy between 2D solution and 3D stress results at the TSV edge. It is widely known that most of mechanical reliability failures occur at the interface between different materials. Therefore, 2D solution does not predict mechanical failure mechanism for TSVs correctly. Also, SiO_2 liner, which acts as a stress buffer layer, reduces σ_{rr} stress at the TSV edge by 35 MPa compared with the case without landing pad and liner. The landing pad also helps decrease stress magnitude at the TSV edge.

We also employ benzocyclobutene (BCB), a polymer dielectric material, as an alternative TSV liner material [5, 6]. Since Young's modulus, which is a measure of the stiffness of an isotropic elastic material, of BCB is much lower than Cu, Si, and SiO_2, this BCB liner can absorb the stress effectively from the CTE mismatch. Figure 3 shows the impact of liner material and thickness on σ_{rr} stress component. As liner thickness increases, stress magnitude at the TSV edge decreases noticeably, especially for the BCB liner case.

It is evident from these experiments that modeling stress distribution considering surrounding structures such as a liner and a landing pad is important to analyze the thermo-mechanical stress around TSVs more accurately. We construct a stress library by varying TSV diameter/height, landing pad size, and liner material/thickness to enable full-chip thermo-mechanical stress and reliability analysis with different TSV structures.

3. FULL-CHIP RELIABILITY ANALYSIS

FEA simulation of thermo-mechanical stress for multiple TSVs require huge computing resources and time, thus it is not suitable for full-chip analysis. In this section, we present full-chip stress and reliability analysis flow. To enable a full-chip stress analysis, we first explore and validate the principle of linear superposition of stress tensors from individual TSVs. Based on the linear superposition method, we build full-chip stress map. Then from this full-chip stress map, we compute von Mises yield metric to predict mechanical reliability problems in 3D ICs.

3.1 Full-chip Analysis with Multiple TSVs

First, based on the observation that the stress field of a single TSV in isolation is radially symmetrical due to the cylindrical shape of a TSV, we obtain stress distribution around a TSV from a set of stress tensors along an arbitrary radial line from the TSV center in a cylindrical coordinate system. To evaluate a stress tensor at a point affected by multiple TSVs, a conversion of a stress tensor to a Cartesian coordinate system is required. This is due to the fact that we extract stress tensors from a TSV whose center is the origin in the cylindrical coordinate system; hence we cannot perform a vector sum of stress tensors at a point from each TSV which has a different center location. Then, we compute a stress tensor at the point of interest by adding up stress tensors from TSVs affecting this point. We set a TSV stress influence zone as 25 μm from the center of a TSV, since the magnitude of stress components becomes

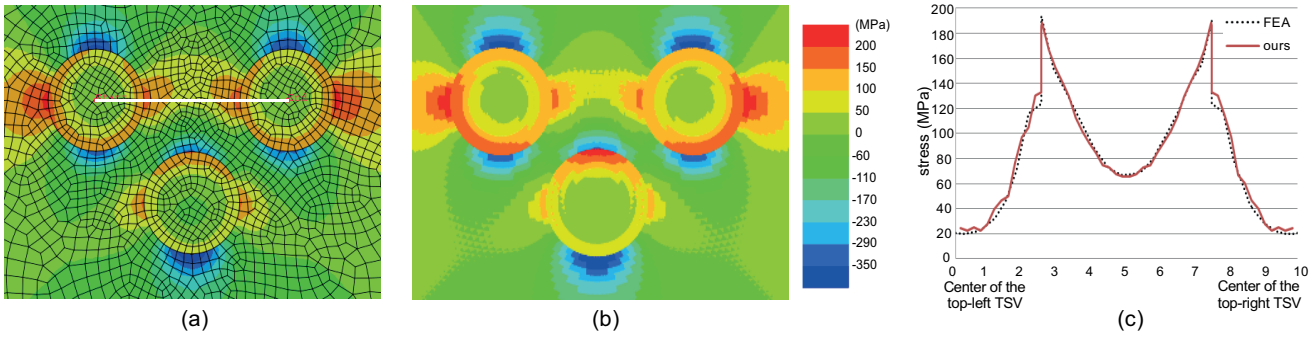

Figure 4: Sample stress comparison between FEA simulation and linear superposition method. (a) FEA result (σ_{xx}). (b) ours (σ_{xx}). (c) FEA vs. ours (σ_{xx}) along the white line in (a).

$$\sigma_v = \sqrt{\frac{(\sigma_{xx}-\sigma_{yy})^2 + (\sigma_{yy}-\sigma_{zz})^2 + (\sigma_{zz}-\sigma_{xx})^2 + 6(\sigma_{xy}^2+\sigma_{yz}^2+\sigma_{zx}^2)}{2}} \quad (1)$$

negligible beyond this distance.

Let the stress tensor in Cartesian and cylindrical coordinate system be S_{xyz} and $S_{r\theta z}$, respectively.

$$S_{xyz} = \begin{bmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \sigma_{zz} \end{bmatrix}, S_{r\theta z} = \begin{bmatrix} \sigma_{rr} & \sigma_{r\theta} & \sigma_{rz} \\ \sigma_{\theta r} & \sigma_{\theta\theta} & \sigma_{\theta z} \\ \sigma_{zr} & \sigma_{z\theta} & \sigma_{zz} \end{bmatrix}$$

The transform matrix Q is the form:

$$Q = \begin{bmatrix} \cos\theta & -\sin\theta & 0 \\ \sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

where, θ is the angle between the x-axis and a line from the TSV center to the simulation point. A stress tensor in a cylindrical coordinate system can be converted to a Cartesian coordinate system using conversion matrices: $S_{xyz} = QS_{r\theta z}Q^T$.

We validate the linear superposition of stress tensors against FEA simulations by varying the number of TSVs and their arrangement. We observe that % error between the linear superposition method and FEA simulations is less than 5 % down to the TSV pitch of 7 μm. As we further decrease TSV pitch, due to strong TSV-to-TSV interaction % error starts to increase. However, since the minimum TSV pitch achievable in the current process is around 10 μm [1], this linear superposition method is valid in a practical sense. Figure 4 shows one of test cases which contains three TSVs, and it clearly shows our linear superposition method matches well with the FEA simulation result. Even though we only show σ_{xx} component due to space limit, other stress tensor components also match well with FEA simulation results.

3.2 Mechanical Reliability Analysis

In order to evaluate if computed stresses indicate possible reliability concerns, a critical value for a potential mechanical failure must be chosen. The von Mises yield criterion is known to be one of the most widely used mechanical reliability metric [8]. If the von Mises stress exceeds a yielding strength, material yielding starts. Prior to the yielding strength, the material will deform elastically and will return to its original shape when the applied stress is removed. However, if the von Mises stress exceeds the yield point, some fraction of the deformation will be permanent and non-reversible.

There is a large variation of yield strength of Cu in the literature, from 225 MPa to 600 MPa, and it has been reported to depend upon thickness, grain size, and temperature [8]. We use 600 MPa as a Cu yielding strength in our experiments. The yield strength of silicon is 7000 MPa, which will not be reliability concerns for the von Mises yield criterion.

input : TSV list T, stress library, thermal map (optional)
output: stress map, von Mises stress map
for *each TSV* t *in* T **do**
  $c \longleftarrow$ center of t
  $r \longleftarrow$ FindStressInfluenceZone(c)
  for *each point* r' *in* r **do**
    $r'.TSV \longleftarrow t$
  end
end
for *each simulation point* p **do**
  if $p.TSV \neq \emptyset$ **then**
    for *each* $t \in p.TSV$ **do**
      $d \longleftarrow distance(t, p)$
      $S_{cyl} \longleftarrow$ FindStressTensor($d, temperature$)
      $\theta \longleftarrow$ FindAngle($line\ tp, x\ axis$)
      $Q \longleftarrow$ SetConversionMatrix(θ)
      $S_{Cart} \longleftarrow QS_{cyl}Q^T$
      $p.S_{Cart} \longleftarrow p.S_{Cart} + S_{Cart}$
    end
  end
  $vonMises(p) \longleftarrow$ ComputeVonMises($p.S_{cart}$)
end

Algorithm 1: Full Chip Stress and Reliability Analysis Flow

The von Mises stress is a scalar value at a point that can be computed using components of a stress tensor shown in Equation (1). By evaluating von Mises stress at the interface between a TSV and a liner, where highest von Mises stress occurs, we can predict mechanical failures in TSVs.

Our full-chip stress and reliability analysis flow is shown in Algorithm 1. We first start to find a stress influence zone from each TSV. Then, we associate the points in the influence zone with the affecting TSV. Next, for each simulation point under consideration, we look up the stress tensor from the TSV found in the association step, and use the coordinate conversion matrices to obtain stress tensors in the Cartesian coordinate system. We visit an individual TSV affecting this simulation point and add up their stress contributions. Once we finish the stress computation at a point, we obtain the von Mises stress value using Equation (1). The complexity of this algorithm is $O(n)$, where n is number of simulation points.

4. FULL-CHIP SIMULATION RESULTS

We implement a TSV-aware full-chip stress and reliability analysis flow in JAVA and C++. Four variations of an industrial circuit,

Table 1: Benchmark circuits

circuit	TSV placement	TSV cell size ($\mu m \times \mu m$)	wirelength (mm)	area ($\mu m \times \mu m$)
Irreg3X	Irregular	7.41×7.41	9060	960×960
Reg3X	Regular	7.41×7.41	9547	960×960
Irreg4X	Irregular	9.88×9.88	8884	1000×1000
Reg4X	Regular	9.88×9.88	9648	1000×1000

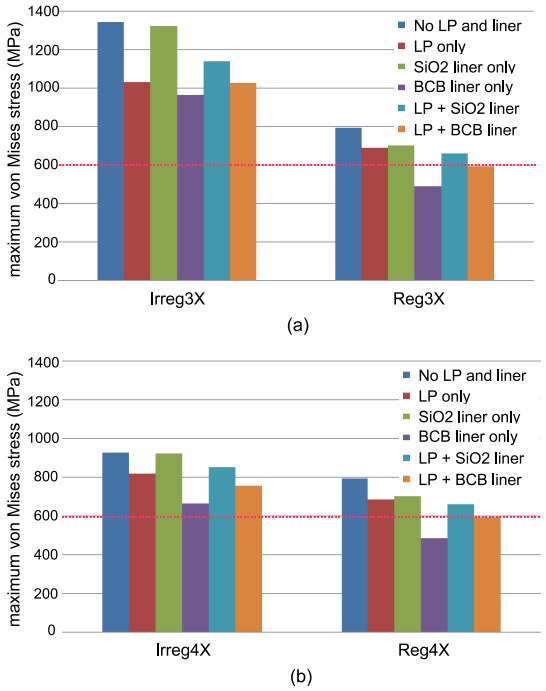

Figure 5: Impact of TSV structure, TSV placement style, and KOZ size on the maximum von Mises stress. (a) designs with 3X TSV cell (KOZ = 1.205 μm). (b) 4X TSV cell (KOZ = 2.44 μm).

with changes in TSV placement style and TSV cell size, are used for our analysis, which are listed in Table 1. The number of TSVs and gates are 1472 and 370K, respectively, for all cases. These circuits are synthesized using Synopsys Design Compiler with the physical library of 45 nm technology, and designed using Cadence SoC Encounter to two-die stacked 3D ICs.

In the regular TSV placement scheme, we pre-place TSVs uniformly on each die, and then place cells, while TSVs and cells are placed simultaneously in the irregular TSV placement scheme. The irregular TSV placement shows better wirelength than the regular case [3]. We use a gate-level 3D IC design methodology for these circuits as a baseline, and compare these with block-level designs in section 4.6.

Even though we simulate 25M points for all test cases, it takes less than 10 minutes since this requires a linear time computation proportional to the number of simulation points on the grid, while a typical FEA simulation for a single TSV structure takes from several minutes to hours depending on the mesh structure. We also validate our analysis results against FEA simulations by comparing a small section of a design which contains a small group of TSVs, which shows less than 2% error in terms of the maximum stress value. The proposed full-chip stress and reliability analysis based on linear superposition of stress tensors is fast and accurate enough to be used for iterative optimization purpose.

4.1 Overall Comparison

In this section, we discuss the impact of TSV structure, TSV placement style, and KOZ size on the thermo-mechanical stress and the mechanical reliability in 3D ICs. We perform full-chip stress and reliability analysis on our benchmark circuits based on our stress modeling results with different TSV structures.

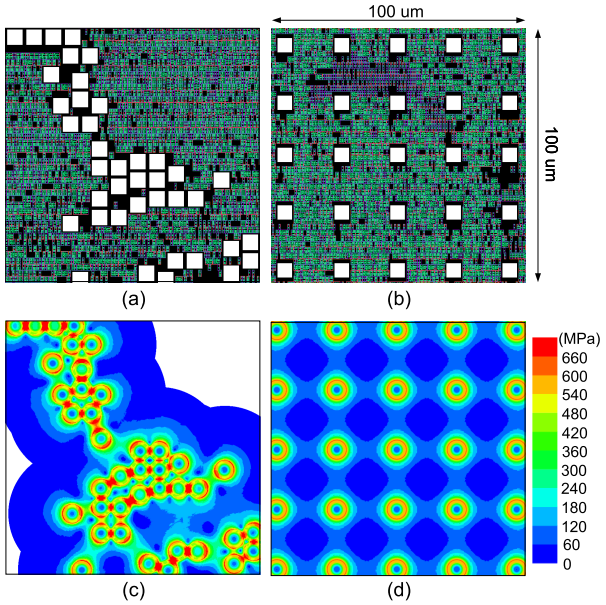

Figure 6: Close-up shots of layouts and von Mises stress maps. (a) Irreg3X. (b) Reg3X. (c) Von Mises stress map of Irreg3X. (d) Von Mises stress map of Reg3X.

Table 2: Impact of TSV size on the maximum von Mises stress. The numbers in parentheses are % reduction compared to TSV large case.

TSV placement	max von Mises stress (MPa)		
	TSV large	TSV medium	TSV small
Irregular	1241.87	1141.9 (8% ↓)	924.16 (26% ↓)
Regular	754.9	659.37 (12% ↓)	456.47 (40% ↓)

Figure 5 shows the maximum von Mises stress in our benchmark circuits. We first observe that designs with irregular TSV placement show worse maximum von Mises stress than those with the regular TSV placement. This is mainly because TSVs can be placed closely in case of the irregular TSV placement scheme to minimize wirelength. Figure 6 shows the part of von Mises stress maps of Irreg3X and Reg3X circuits, and we see that most of TSVs in the Irreg3X circuit exceed Cu yielding strength (600 MPa). Second, as the KOZ size becomes larger stress level reduces significantly for the irregular TSV placement case. By enlarging KOZ size, interference from nearby TSVs is reduced. However, for the regular TSV placement case, since TSV pitch of Reg3X (23.5 μm) and Reg4X (25 μm) is similar and also interference from nearby TSVs is negligible at this distance, there is no noticeable difference in maximum von Mises stress. Third, these results show the importance of using an accurate TSV stress model to assess the mechanical reliability of 3D ICs. There are significant differences in the von Mises stress depending on the existence of structures surrounding a TSV, such as a landing pad or a liner. It is possible that we might overestimate the reliability problems by using a simple TSV stress model not considering a landing pad or a liner. However, most of these test cases violate the von Mises yield criterion for Cu TSV. Section 4.4 shows how TSV liners help reduce the violations.

4.2 Impact of TSV Size

To investigate the effect of the TSV size, we use three different sizes of TSV with a same aspect ratio of 6; TSV small ($H/D = 15/2.5\ \mu m$), TSV medium ($H/D = 30/5\ \mu m$), and TSV large ($H/D = 60/10\ \mu m$), where H/D is TSV height/diameter. Also,

Table 3: Impact of a landing pad size on von Mises criterion. The numbers in parentheses are % reduction compared to LP $6 \times 6\ \mu m^2$ case.

circuit	LP $6 \times 6\ \mu m^2$		LP $8 \times 8\ \mu m^2$	
	max von Mises stress (MPa)	# violating TSVs	max von Mises stress (MPa)	# violating TSVs
Irreg4X	852.83	1472	827.06 (3% ↓)	1472 (0% ↓)
Reg4X	659.84	1472	612.45 (7% ↓)	1472 (0% ↓)

Table 4: Impact of liner thickness on the number of TSVs violating von Mises criterion. The numbers in parentheses are % reduction compared to the 125 nm thick liner case.

circuit	liner material	# violating TSVs		
		125 nm	250 nm	500 nm
Irreg3X	SiO_2	1467	1433 (2% ↓)	1297 (11% ↓)
	BCB	1407	1172 (17% ↓)	357 (75% ↓)
Reg3X	SiO_2	1472	0 (100% ↓)	0 (100% ↓)
	BCB	0	0 (-)	0 (-)
Irreg4X	SiO_2	1472	1272 (14% ↓)	97 (93% ↓)
	BCB	1044	535 (49% ↓)	0 (100% ↓)
Reg4X	SiO_2	1472	0 (100% ↓)	0 (100% ↓)
	BCB	0	0 (-)	0 (-)

to suppress the effect of KOZ size, we use 2X TSV cell (KOZ 1.22 μm) for TSV small, 3X TSV cell (KOZ 1.202 μm) for TSV medium, and 5X TSV cell (KOZ 1.175 μm) for TSV large. Additionally, we set the landing pad width is 1 μm larger than the corresponding TSV diameter, and use a 125 nm thick SiO_2 liner for all cases for fair comparisons. Table 2 shows the maximum von Mises stress. For both irregular and regular TSV placement schemes benefit from smaller TSV diameter significantly. This is mainly because the magnitude of normal stress components decay proportional to $(D/2r)^2$, where r is the distance from the TSV center.

4.3 Impact of Landing Pad Size

In this section, we explore the impact of landing pad size, which is normally determined by considering TSV alignment, on reliability issues. Designs with 4X TSV cells with 125 nm thick SiO_2 liner are used. We compare the maximum von Mises stress and the number of violating TSVs with two different landing pad size shown in Table 3. These results show that the regular TSV placement benefits more von Mises stress reduction from the larger landing pad size. This is because the stress reduction in a single TSV directly translates to the overall stress magnitude decrease in a full-chip scale for the regular TSV placement case. However, increasing the landing pad size does not improve von Mises stress significantly. Also we see that all TSVs do not satisfy von Mises criterion for every test case. This is because only the magnitude of σ_{rr} stress component at the wafer surface is reduced due to Cu landing pad, while other stress components hardly changes with a larger landing pad size.

4.4 Impact of Liner Thickness

In this section, we examine the impact of liner thickness on von Mises stress. We use designs with both 3X TSV cells and 4X TSV cells, and set the landing pad size $6 \times 6\ \mu m^2$ and $8 \times 8\ \mu m^2$, respectively. Figure 7 shows the maximum von Mises stress results with liner thickness of 125 nm, 250 nm, and 500 nm. We observe that liner thickness has a huge impact on the von Mises stress magnitude, since the thicker liner effectively absorbs thermo-mechanical stress at the TSV/liner interface. Especially, the BCB liner shows significant reduction in the maximum von Mises stress compared with SiO_2 liner due to extremely low Young's modulus shown in Section 2.1. For example, 500 nm thick BCB liner reduces the maximum von Mises stress by 29% for the Irreg3X and satisfies the von Mises yield criterion for all circuits with a regular TSV placement.

Table 4 shows the number of TSVs violating von Mises criterion.

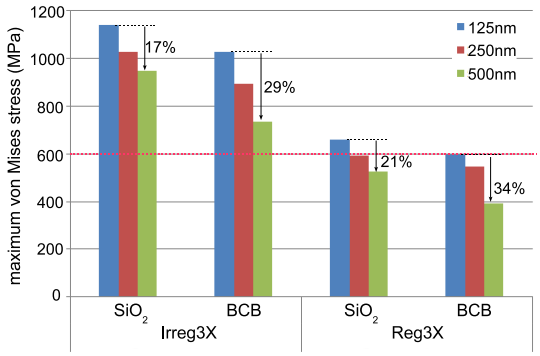

Figure 7: Impact of liner thickness on the maximum von Mises stress of circuits with 3X TSV cell.

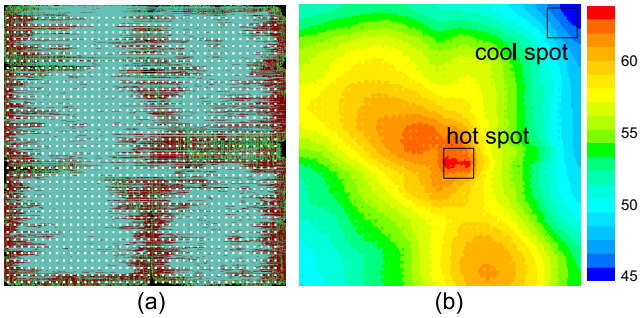

Figure 8: Impact of temperature (°C) during a chip operation on von Mises stress. (a) layout of Reg3X. TSV landing pads are white rectangles. (b) thermal map.

Even though there are still many TSVs not satisfying von Mises criterion for the Irreg3X circuit, it is possible to reduce von Mises stress if we place TSVs carefully considering this reliability metric during a placement stage.

4.5 Impact of Chip Operation Temperature

Up to this point, we only consider the residual stress caused by the manufacturing process. In this section, we examine the reliability problem during the chip operation phase. Our full-chip thermal simulation flow is as follows. We first generate a power map using SoC Encounter, and then feed this to ANSYS Fluent with in-house add-ons which enable a steady-state thermal analysis for GDSII level 3D ICs shown in Figure 8(b). Depending on the temperature distribution across the die area, each TSV experiences a different thermal load. Thus, the significance of mechanical reliability problems of an individual TSV might be different from each other. To support temperature dependent stress analysis, we build stress library with wide range of thermal load.

We use the Reg3X circuit for this experiment since TSVs in the regular TSV placement scheme show uniform von Mises stress distribution, which enables us to observe the impact of an operating temperature across the die easily. We use a 500 nm thick BCB liner for this experiment. The cool spot experiences higher von Mises stress, since the temperature difference from the stress free temperature, 275°C in our case, is larger in the cool spot than in the hot spot. However, since the maximum temperature difference across the die is only 20°C, the impact of an operating temperature on the TSV reliability across the die is not significant. In our test case, the difference of the maximum von Mises stress between two spots is 31.8 MPa. Also, both the hot and the cool spot experience less maximum von Mises stress compared to the residual stress case, again due to the reduced thermal load. However, the reduction of von Mises stress during a chip operation cannot recover the material yielding failure if it already exists, since this is a

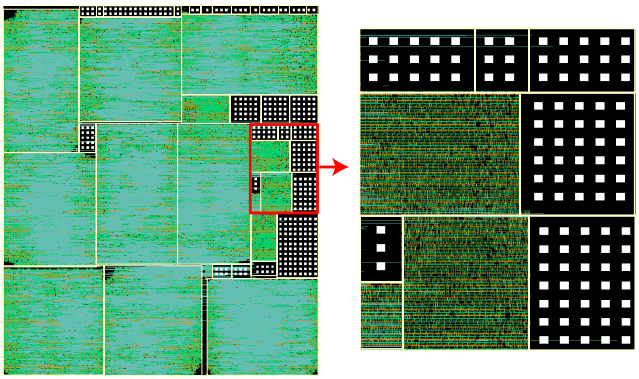

Figure 9: Layout of block-level design (TSV pitch = 15 μm). White rectangles are TSV landing pads. (a) full-chip layout. (b) close-up shot of the red box in (a).

Table 5: Comparison between gate-level and block-level design

level	TSV pitch (μm)	# TSV	wirelenth (mm)	area ($\mu m \times \mu m$)	max stress (MPa)
Gate	irregular	1472	9060	960×960	734.12
	23.5	1472	9547	960×960	391.8
Block	15	368	8259	950×1130	419.28
	10	394	8028	1080×1000	525.92
	7.5	333	7933	980×1090	722.72

non-reversible failure mechanism.

4.6 Reliability of Block-Level 3D Design

Even though the gate-level 3D design has the potential of highest optimization, the block-level design is attractive in the sense that we can reuse highly optimized 2D IP blocks. In this section, we study the reliability issues in block-level 3D designs. 3D block-level designs are generated using an in-house 3D floorplanner which treats a group of TSVs as a block shown in Figure 9. We use a 500 nm thick BCB liner for this experiment. We vary the TSV pitch inside TSV blocks to examine its impact on layout quality as well as reliability issues. Table 5 shows that block-level designs use less number of TSVs, show shorter wirelength, and occupy more area than gate-level designs. Experimental results show that we can control the von Mises stress with area overhead in block-level design, since the TSV pitch in block-level design is controllable. Another benefit of block-level design is that we can localize the thermo-mechanical reliability problems only nearby TSV blocks.

4.7 Impact of TSV Re-placement

In this section, we manually optimize TSV locations to show the potential benefit of TSV reliability aware layout optimization while minimizing the change in layout. We use the Irreg3X circuit which shows worst von Mises stress, and employ 500 nm thick BCB liner for this experiment. Our related study on the maximum von Mises stress vs. TSV-to-TSV pitch shows that 10 μm pitch is a reasonable choice to reduce von Mises stress considering some safety margin. We reposition densely placed TSVs to nearby white spaces if available to reduce the von Mises stress. Figure 10 shows the part of the Irreg3X circuit layout with re-placed TSVs. Table 6 shows the distribution of von Mises stress higher than 420 MPa across the die before and after the TSV re-placement, and we see the reduction in high von Mises stress region after TSV re-placement. With small perturbations of TSV locations, we could reduce the von Mises stress level and decrease the number of violating TSVs from 357 to 293, which is 18 % improvement with only 0.23 % wirelength increase. This small test case shows the possibility of a layout optimization without degrading performance too much.

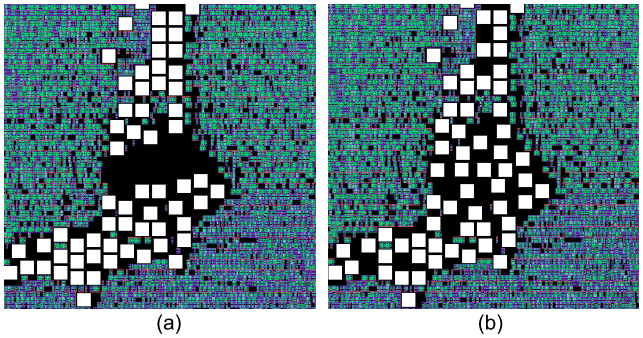

Figure 10: TSV re-placement to reduce von Mises stress. TSV landing pads are white rectangles. (a) original layout. (b) after TSV re-placement.

Table 6: Von Mises stress distribution after TSV replacement

	von Mises stress (MPa)				
	420-480	480-540	540-600	600-660	660-
original	0.21%	0.101%	0.043%	0.012%	0.002%
replacement	0.225%	0.093%	0.037%	0.010%	0.0%

5. CONCLUSIONS

In this work, we show how TSV structures affect stress field and a mechanical reliability in 3D ICs. We also present an accurate and fast full-chip stress and mechanical reliability analysis flow, which can be applicable to placement optimization for 3D ICs. Our results show that KOZ size, TSV size, liner material/thickness, and TSV placement are key design parameters to reduce the mechanical reliability problems in TSV based 3D ICs.

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