Electromigration Modeling and Full-chip Reliability Analysis for BEOL Interconnect in TSV-based 3D ICs

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***Abstract*—Electromigration (EM) is a critical problem for interconnect reliability of modern integrated circuits (ICs), especially as the feature size becomes smaller. In three-dimensional (3D) IC technology, the EM problem becomes more severe due to drastic dimension mismatches between metal wires, through silicon vias (TSVs), and landing pads. Meanwhile, the thermo-mechanical stress due to the TSV can also cause reduction in the failure time of wires. However, there is very little study on EM issues that consider TSVs in 3D ICs. In this paper, we show the impact of TSV stress on EM failure time of metal wires in 3D ICs. We model the impact of TSV on stress variation in wires. We then perform detailed modeling of the impact of stress on EM failure time of metal wires. Based on our analysis, we build a detailed library to predict the failure time of a given wire based on current density, temperature and stress. We then propose a method to perform fast full-chip simulation, to determine the various EM related hot-spots in the design. We also propose a simple routing-blockage scheme to reduce the EM related failures near the TSVs, and see its impact on various metrics.**

I. Introduction

Electromigration involves the mass transport of atoms in solid state metals. The mass transport of atoms can lead to creation of hill-locks or voids in the conductor. Current density is usually considered as the major cause for mass transport of atoms. However, other factors like stress gradients, and temperature can also play a significant role as shown in the work [1] [2], [3], and [4]. The reduction of feature sizes in modern ICs has aggravated the problem of electromigration. Thus, considering EM while designing modern ICs is important for reliability aspects.

3D ICs consist of through silicon vias (TSVs) that are fabricated using a complex manufacturing process. The TSV itself is primarily made up of copper, and the material surrounding it is made up of silicon. Both these materials have widely varying mechanical properties. During manufacturing, the 3D IC undergoes thermal cycling that causes thermo-mechanical stress in the region surrounding the TSVs. Thus, it becomes important to asses the mechanical reliability of 3D ICs. The thermo-mechanical stress generated around the TSVs, is largely due to the significant mismatch in the coefficient of thermal expansion (CTE) of copper ($17.7ppm/^oC$) used for TSVs, and the surrounding silicon ($3.05ppm/^oC$). The thermo-mechanical stress induced by the TSVs can impact reliability in several ways. TSV-induced stress can affect the silicon region surrounding it. The change in the stress of the silicon can change carrier mobility, and can thus impact performance of devices near TSVs [5], [6]. TSV-induced stress can also impact the dielectric layers, and the metal wires around the TSV [6]. In this paper, we focus on the electromigration reliability impact of the TSVs on the nearby metal wires.

Previous works in [1], [2], [3], and [4] show that the failure time (T_f) of a wire is dependent on multiple factors; including current density, temperature, and stress gradients. Thus, to determine EM reliability of a chip we need to consider all the three factors. This work, to our best knowledge, is the first detailed study of full-chip EM analysis for 3D ICs, considering the impact of TSV-induced stress on interconnects. Metal-2 (M2) wires are the closest wires above the TSV structure. Thus, M2 wires are more prone to the TSV-induced stress. In this work, we show experimental results for M2 wires near a TSV. However, our method can be extended for analyzing any metal layer. The major contributions of this paper are as follows: 1) We propose an electromigration (EM) failure time model for wires near TSVs in 3D ICs as shown in Figure 1. Our model is an extension of the work done in [7]. While the basic equations remain the same, our model considers the impact of the additional TSV-induced stress on the failure time of metal wires. The TSV-induced stress is obtained by performing finite-element-method (FEM) based simulations. 2) We propose an effective way of building libraries for thermo-mechanical stress, and failure time (T_f). We also propose a method to perform fast full-chip 3D IC analysis. 3) As an application of our full-chip EM analysis, we demonstrate the impact of routing blockages on enhancing the reliability 3D ICs.

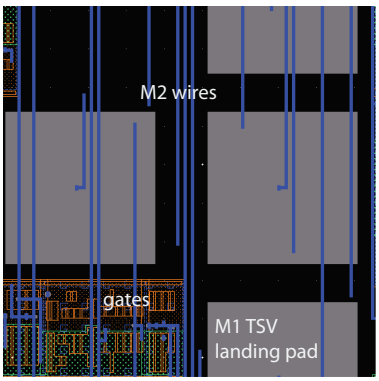

Fig. 1. Typical layout of 3D IC, where TSV landing pads in M1, gates, and M2 are shown. M2 wires going over or running nearby are under the risk of EM-related failure due to TSV-induced stress.

II. Preliminaries

In this section, we discuss some concepts behind the electromigration modeling of interconnects. In classical electromigration studies, Black [1] proposed an empirical equation to relate the mean time to failure of metal interconnects, to current density and temperature. However, a lot of experimental work and modeling has shown that Black's equation is not accurate enough to predict the failure in metal interconnects [7]. Black's equation considers only current density as the driving force responsible for EM failure. However, failure in the interconnect may be caused due to several interacting forces. These forces include current density, temperature gradient, mechanical-stress gradient, and atom concentration gradient. The migration of atoms caused by each of these forces can be categorized as follows

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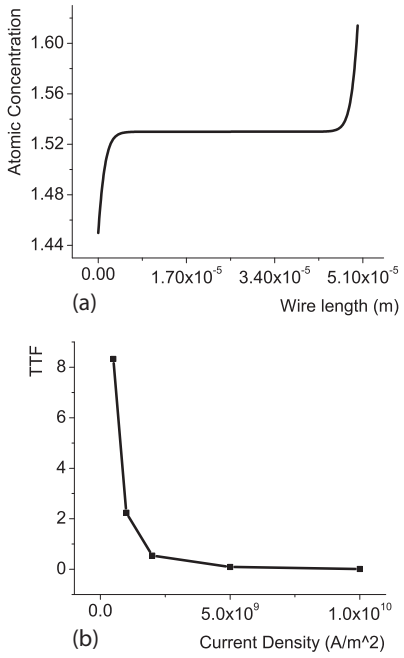


Fig. 2. (a) Change in concentration along a wire due to current. (b) Impact of current density on failure time of a metal wire.

([7]): 1) current-induced migration (CM) caused by moving electrons of current, 2) stress-induced migration (SM) caused by thermo-mechanical stress gradient, 3) temperature-induced migration (TM) caused by temperature gradient, and 4) atomic migration (AM) caused by atomic concentration gradient. In this paper, we use the term electromigration (EM) to describe the mass transport of atoms caused by all the above forces. To specifically describe the failure in metal interconnects, which is caused by current density, we use the term CM. The variation of atomic concentration in a metal structure may be represented by the following equations:

$$\frac{\partial c}{\partial t} + \nabla \cdot \Gamma = 0 \tag{1}$$

$$\Gamma = -D\nabla c + \frac{Dcje\rho Z}{kT} + \frac{Dc\Omega}{kT} \cdot (\nabla(\sigma_m)) + \frac{DcQ^*}{kT} \cdot \frac{\nabla(T)}{T} \tag{2}$$

where $D = Do\ exp(-E_a/kT)$. The variables used in the above equations along with their typical values are discussed in greater detail in Table I. The atomic flux terms J_e, J_s, J_t, and J_a that are caused by CM, SM, TM, and AM respectively, can be represented by the following equations:

$$J_e = \frac{Dcje\rho Z}{kT} \tag{3}$$

$$J_s = \frac{Dc\Omega}{kT} \cdot (\nabla(\sigma_m)) \tag{4}$$

$$J_t = \frac{DcQ^*}{kT} \cdot \frac{\nabla(T)}{T} \tag{5}$$

$$J_a = -D\nabla c \tag{6}$$

The contributions due to each of the above terms can be different, and the combined effect of the different forces can determine where and when the failure occurs in a metal interconnect.

A. Understanding the EM phenomenon

In modern integrated circuits (ICs), creation of back-end-of-line (BEOL) structures, including wires and vias is a complicated process involving many steps. A typical copper interconnect has diffusion barrier layers at the end of the wire [8]. The barrier layers, which are at the end of the interconnect, act as a blocking boundary that prevents the transport of copper atoms across them. Atoms in the metal interconnect would accumulate or deplete, only when, the divergence of atomic flux caused by different forces is not zero. Let us consider a small subsection in the middle of the interconnect. To simplify our understanding, we assume that only current is flowing across the interconnect. The number of atoms that enter or leave the small subsection of the interconnect is the same. Thus, the middle of the interconnect experiences no change in atomic concentration. However, the ends of the interconnect act as a blocking boundary. Thus, atoms tend to accumulate or deplete at the end of the interconnect. Other factors, such as stress gradients or temperature gradients also behave similarly.

TABLE I
NOMENCLATURE AND PARAMETER VALUES

Parameter	Representation	Value
c	Atomic Concentration	-
Do	Initial diffusivity	1e-8
Ea	Activation energy	1.3e-19
k	Boltzmans constant	1.38e-23
T	Temperature (K)	-
j	Current density (A/m2)	-
Z	Effective charge	4
e	Electron charge	1.6e-19
Ω	Atomic volume	1.6e-29
σ_m	Hydrostatic stress	-
Q	Heat of transport	-0.0867eV
ρ	Resistivity	1.68e-8

III. EM ANALYSIS OF A METAL WIRE

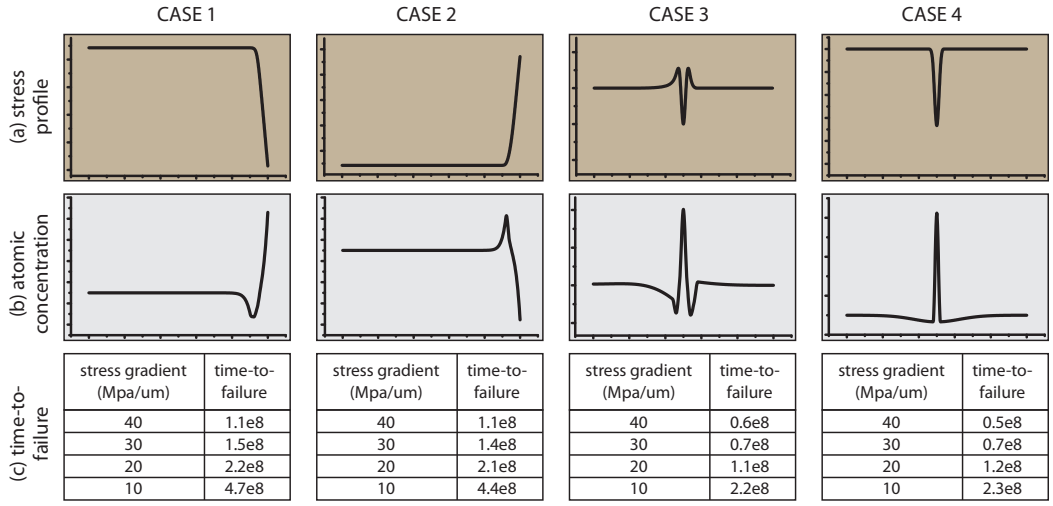
In this section, we discuss how different forces can affect the failure time (T_f) of a metal wire. We perform the analysis using a finite-element-method (FEM) based model in COMSOL multi-physics. We build a one-dimensional (1D) model of a thin metal wire using the equations described in Section II. To measure the degradation caused by EM, we use a time-metric to measure how long it takes for the atomic concentration variation to reach a certain threshold. In this paper, we use 5% deviation of the atomic concentration ([7]) as the threshold.

A. Atomic migration caused by current

To model the effect of atom migration caused by current, we assume the wire is subjected to a certain current load. The variation in the atomic concentration along the wire is shown in Figure 2(a). We see that the atomic concentration changes towards the end of the wire. As discussed in Section II-A, the end of the wire acts as blocking boundary, thus, causes accumulation or depletion of atoms at the end of the wire. The relationship between T_f, and current density is shown in Figure 2(b). We observe that as the current density increases, the failure time (T_f) of the wire decreases.

B. Atomic migration caused by stress

In this section, we observe the impact of stress gradient on T_f of a metal wire. We consider four different stress profiles as shown in Figure 3(a). We will show later, that these four stress profiles are critical in analyzing the full-chip reliability of three-dimensional (3D) ICs. As shown in Equation 4, the atomic flux caused by stress is proportional to the magnitude of the hydrostatic stress gradient. The change in the atomic concentration corresponding to each profile is shown in Figure 3(b). The relation between T_f, and the magnitude



stress gradient (Mpa/um)	time-to-failure
40	1.1e8
30	1.5e8
20	2.2e8
10	4.7e8

stress gradient (Mpa/um)	time-to-failure
40	1.1e8
30	1.4e8
20	2.1e8
10	4.4e8

stress gradient (Mpa/um)	time-to-failure
40	0.6e8
30	0.7e8
20	1.1e8
10	2.2e8

stress gradient (Mpa/um)	time-to-failure
40	0.5e8
30	0.7e8
20	1.2e8
10	2.3e8

Fig. 3. (a) Four different stress profiles acting on a wire. (b) Change in atomic concentration due to stress gradients. (c) Impact on time-to-failure due to increasing stress gradient.

of the stress slope is shown in Figure 3(c). As the magnitude of the stress gradient increases T_f decreases.

C. Atomic migration caused by temperature

In an integrated circuit, the temperature profile seen by a wire is dependent upon the power map of the IC, the thermal resistance, and the self heating of the wire. The actual temperature gradient of an interconnect in a 3D IC can be hard to predict. Temperature gradient impacts mass transport of atoms in two ways. First, it changes diffusivity D ($= Do\ exp(-E_a/kT)$) that can lead to faster migration of atoms. Second, the temperature migration force TM ($=\frac{DcQ^*}{kT} \cdot \frac{\nabla(T)}{T}$) can also cause migration of atoms.

D. Overall Effect

To build an accurate model for electromigration all three forces that are CM, SM, and TM should be considered simultaneously. AM typically acts as a resistive force opposing the other forces. Thus, AM is not considered as a driving force. The different forces can either aid or oppose each other to cause the migration of atoms. However, it should be noted that SM can act on metal wire even when the integrated circuit is off, whereas, CM and TM occur only when the integrated circuit is operating. We assume that when the IC is turned off, there are no temperature gradients in the IC that may cause atomic migration because of temperature. In Figure 4, we show an example of how atomic concentration along a wire can change because of current, stress, and temperature. We observe, that the combined effect on the wire can be obtained by the superposition of the individual effect of each of the forces. Also, if we compare Figure 4(c) with Figure 2, we see a difference in the atomic concentration variation. The difference occurs because in Figure 4(c) the diffusivity D also changes with temperature, whereas, in Figure 2 the temperature is constant across the wire.

IV. EM-aware Reliability Modeling

Based on our discussion in Section II, we observe that stress-induced migration (SM) can significantly impact the reliability of a metal interconnect. In 3D integrated circuits, through silicon vias (TSVs) can cause significant stress gradients along a metal wire that can impact the reliability of the metal wire. To predict the failure time for a wire requires complex modeling that may be solved by performing FEM-based simulations. However, even for a single wire, running a FEM tool needs significant run-time and resources. Thus, it is impractical for full-chip analysis. In this section, we propose a way to generate a set of libraries. The libraries can be used to perform full-chip reliability analysis without running the FEM solver.

Our approach can be divided into two parts. First, we perform stress modeling. During stress modeling, we see the impact of a single TSV on a given wire. We then extend our analysis to consider multiple TSVs for full-chip analysis. We generate a TSV-induced stress library. The TSV-induced stress library is used to determine the stress gradients on a metal wire caused by nearby TSVs. Second, we generate a failure time (T_f) library based on the TSV-induced stress library. The goal of the failure time library is to quickly determine the wires that are likely to fail because of current, stress, and temperature. We discuss the details of our library generation in the following sections.

A. TSV-induced stress library

To generate the stress library, we perform thermo-mechanical stress simulations of a 3D structure consisting of TSV, landing pad, dielectric layers, and nearby metal wire. The structure is simulated using an industrial tool called ANSYS. The entire 3D structure is subjected to a thermal ramp from 300^oC to 25^oC. The 3D structure we simulate is discussed in [6]. The stress of a metal wire (caused by a TSV) depends on the relative location, and the distance between the TSV and the metal wire. We show that based on evaluating four important cases we can build an effective stress library. The four cases of a horizontal wire location with respect to a TSV are shown in Figure 5.

- *Case1*: Horizontal wire goes over the TSV, and overlaps with the area occupied by the TSV.
- *Case2*: Horizontal wire ends near the TSV, and lies along the tangential direction from the TSV.
- *Case3*: Horizontal wire ends near the TSV, and lies along the normal direction from the TSV.
- *Case4*: Horizontal wire goes above the TSV, without having intersection with TSV.

To generate an effective TSV-induced stress library, we show that the above four cases are sufficient. For any given horizontal wire, the wire may or may not extend on both sides of the TSV. If the

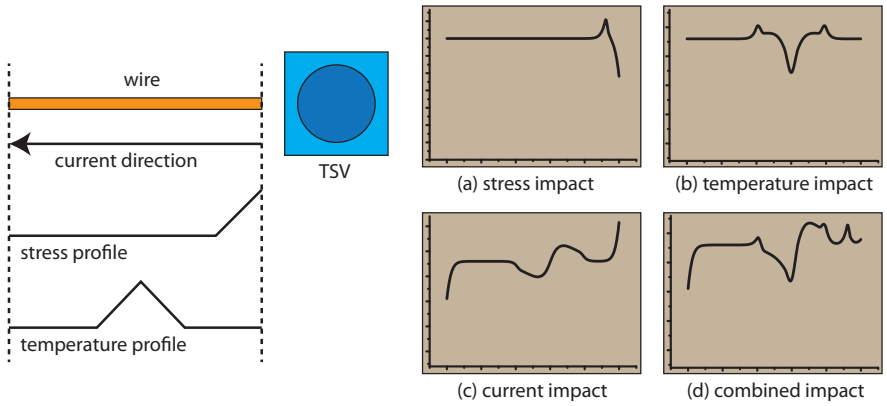


Fig. 4. A single wire subject to current, stress profile and temperature profile. (a) Change in atomic concentration due to stress gradient. (b) Change in atomic concentration due to temperature gradient. (c) Change in atomic concentration due to current. (d) Change in atomic concentration due to combined effect of all three forces.

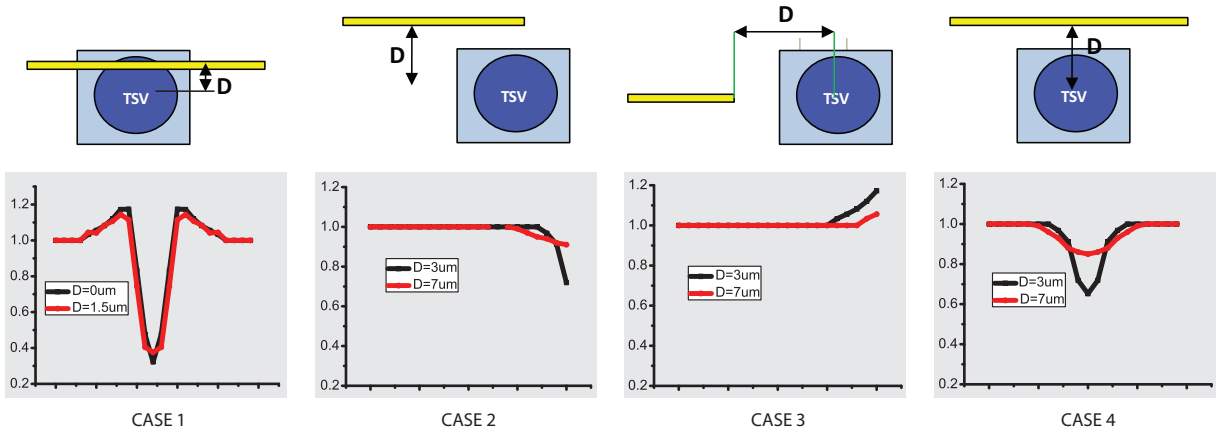


Fig. 5. 4 different cases of a horizontal wire location with respect to a TSV. The top row shows the top view of these cases, where we show a thin horizontal wire, circular TSV and its landing pad. The bottom row shows the stress profile on the wire. It also shows the impact of TSV stress based on the distance D between the wire and TSV.

wire extends on both sides of the TSV, then, we can consider the following two possibilities: 1) the wire goes over the copper TSV and is covered by *case*1, 2) the wire may run parallel to the TSV without going over it. *Case*4 is symmetric with respect to an x-axis going through the TSV center. Thus, it is sufficient to capture all the cases of wire running parallel to the TSV without going over it.

If the wire does not extend beyond the TSV, then, we can consider one of its end points to lie within any quadrant with respect to the TSV center. Again, because of symmetry, cases for other quadrants can be covered if we cover one quadrant. *Case*2 and *case*3 cover the extreme points when the end point of the wire may lie in the second quadrant. We see that our four cases are sufficient to cover all possibilities. By changing the location of the wire w.r.t. the TSV center, an effective library to determine TSV-induced stress can be built. Results for vertical wires can be obtained using symmetry. In Figure 5, we also show how stress gradient decreases as the distance between the wire and the TSV center increases.

In the above discussion, we showed how to determine the TSV-induced stress on a wire because of a TSV. However, to perform full-chip reliability analysis we need to consider multiple TSVs. To consider multiple TSVs, we propose a superposition based method similar to the one discussed in [5]. At any given point on the wire, we first determine all the nearby TSVs that can influence the stress at the given point. Based on a critical distance D_{crit}, we consider only those TSVs whose centers lie at a distance that is less than D_{crit}. We then use the superposition method to consider the effective stress at the given point. In Figure 6, we compare the effectiveness of the two methods. We observe that both methods give similar results.

We briefly discuss the effect of nearby metallization on the stress of a wire. The structure we simulate is shown in Figure 7. The stress results for wire b is also shown in Figure 7. In the simulations we consider two cases: 1) wires a and c are present (multiple wire) during simulation, and 2) when wires a and c are absent (single wire) during simulation. We observe, that the nearby metal wires have little effect on the stress gradients caused by the TSV. To perform a quick first-level analysis, we ignore the effect of nearby metallization.

B. Time-to-failure library

In this section, we show how we can effectively build a library to determine failure time T_f of wires. In Section IV-A, we analyzed that the four cases, which are shown in Figure 5, are sufficient to build a TSV-induced stress library. In this section, we show that the same four cases are also sufficient to determine failure time of wires. To simplify the analysis, we consider two distinct regions of the wire defined as follows:

- Center region of the wire. The center region of the wire can be

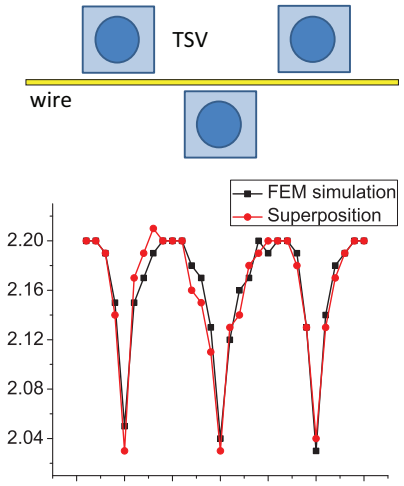


Fig. 6. Comparison between superposition-based stress calculation and FEM-based stress calculation.

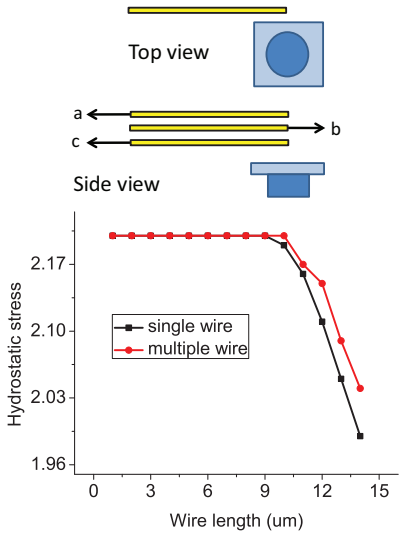


Fig. 7. Impact of nearby metallization. We plot the stress profile of wire 'b' for two cases: 1) when wires 'a' and 'c' are present during simulation (multiple wire), and 2) when wires 'a' and 'c' are absent during simulation.

considered as the region that is far away from the end points of the wire. Multiple TSVs near the center of the wire can cause stress gradients in the wire. In Figure 8(a), we show a case where multiple TSVs may affect a horizontal wire. In this region the horizontal wire is either running parallel to the TSV (*case*4) or goes over it (*case*1). In both cases, the wire experiences a V-shaped stress profile. The stress profile caused by the TSVs is also shown in Figure 8(a). Thus, building a failure time (T_f) library based on *case*1 or *case*4 can predict failure in the center region of the wire.

- End region of the wire. The end region of the wire can be considered as the region that is at the end of the wire. Based on the location of the TSVs nearby, the stress gradient experienced by the wire may be positive or negative. As shown in Figure 8(b), TSV A causes a positive stress gradient, whereas, TSV B causes a negative stress gradient. The TSV that is closer to the wire dominates the stress profile on the wire. We observe that by

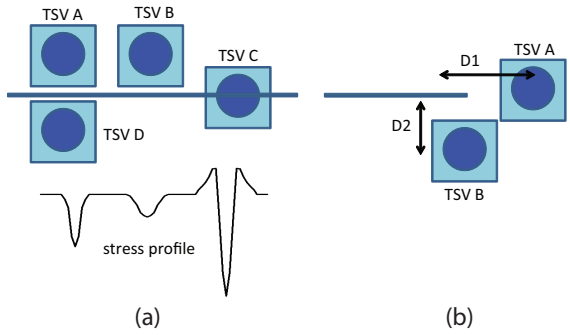


Fig. 8. Stress profile on a wire due to multiple TSVs. (a) When the TSVs are located in regions far away from the end points of a wire. (b) The end point may experience positive or negative stress gradient based on how far it is from TSV A (D1) or from TSV B (D2).

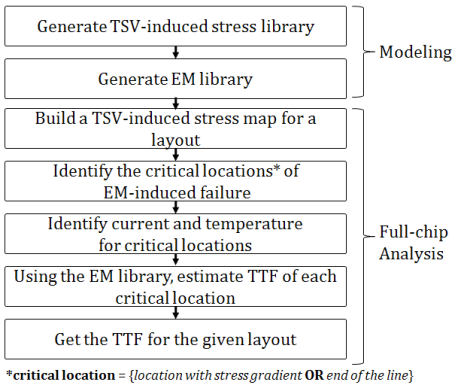


Fig. 9. Generating libraries and estimate the EM time-to-failure for a full-chip layout based on the libraries.

building a failure time (T_f) library based on *case*2, and *case*3; we can predict the failure at the end of the wire.

Vertical wires can be analyzed similarly due to symmetry. As discussed in Section II, stress gradients can cause migration of atoms even when the chip is not operating. However, current and temperature cause the migration of atoms only when the chip is on. To do a complete analysis we build 3 different kinds of libraries. The different libraries built are discussed as follows:

- Current-stress-temperature (CST) library. In the CST library, we assume that all three forces that are current, stress, and temperature, act on the wire.
- Current-temperature (CT) library. In the CT library, we assume that only current and temperature act on the wire. We ignore the effect of stress.
- Stress-temperature (ST) library. In the ST library, we assume that only stress and temperature act on the wire. We ignore the effect of current.

In all three libraries, that are CST, CT, and ST library, we ignore the effect of temperature gradient. However, we consider the effect of temperature on diffusivity D. We ignore the effect of temperature gradient because the possible number of temperature gradient profiles on a chip could be very large. Thus, making it impossible to build an efficient library. At every region of the wire, we assume the temperature of the region is the average temperature surrounding it.

V. Full-chip analysis and application

In this section, we propose a method to estimate EM reliability of a full-chip with TSVs. As shown in Figure 9, after TSV-induced stress and time to failure library are generated, analysis of the full-chip layout is done. Reliability analysis for a given layout is achieved through the following four steps:

1) **Build a TSV-induced stress map:** Using the stress library that is generated in Section IV, it is possible to build a stress map for the entire layout of the chip. The stress map is determined based on the location of TSVs and the wires. Variation in stress along the wire can be determined by using the stress library.
2) **Identify the critical locations of EM-induced failure:** Once we get the stress map, we can determine the stress gradients affecting the wire. As EM-induced failure occurs typically only at the end of the wire or at a high-stress gradient region, we need to look only at critical locations to determine EM reliability. Thus, we define the following: *Critical location of EM-induced failure is the location with high stress gradient (this typically occurs when wire goes over a copper filled TSV) OR the end of the line.*
3) **Identify the current density and temperature of each critical location:** For the current density analysis, we first obtain the layout for all dies in design exchange format (DEF). For 3D nets (nets that have pins in multiple dies), based on the TSV locations we determine the set of wires in each die that form the 3D net. We then use the method discussed in [9] to determine average current density in each wire.
   The steady-state temperature of a point $\mathbf{p} = (x, y, z)$ inside a 3D structure can be obtained by solving the heat equation
   $$\nabla \cdot (k(\mathbf{p})\nabla T(\mathbf{p})) + S_{\mathrm{h}}(\mathbf{p}) = 0 \quad (7)$$
   where k is thermal conductivity in W/m·K, T is temperature in K, and S_{h} is volumetric heat source in W/m^3. This model can be implemented by meshing analyzed structure of a 3D IC. To perform the thermal analysis we obtain the layout of all dies in a 3D IC in GDSII format from Cadence SoC Encounter. We then perform static power analysis to determine the power dissipation of each cell. The layout and logic cell power dissipation information is then used by our analyzer. Once all the information is known, the data is fed into the ANSYS FLUENT tool to perform thermal analysis.
4) **Estimate failure time for each critical location:** The metric to measure the reliability is defined as 5% deviation of atomic concentration in our work. Using the EM library, we get the failure time for each critical location based on the mechanical stress, current density and temperature. Total reliability for a given layout, is determined by the number of wire segments that have failure time (T_f) smaller than a given threshold value T_F^{thresh}. Once we determine failure time at each critical location, the total number of critical wires can be determined easily.

A. Routing Blockages to increase Reliability

From our discussion in Section IV, we observe that TSV induced stress can impact the time-to-failure of nearby wires. To improve the EM reliability of wires, we add routing blockages over the TSV. The routing blockages ensure that no metal wires go near a TSV location. As shown later in our results, adding routing blockages can greatly help in reducing the number of wires that may have EM problems. We show that even with such a simple scheme we can achieve increased reliability.

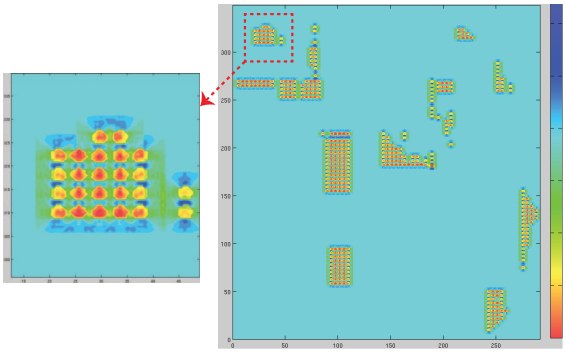


Fig. 10. Variation of hydrostatic stress for vertical wires on a given die.

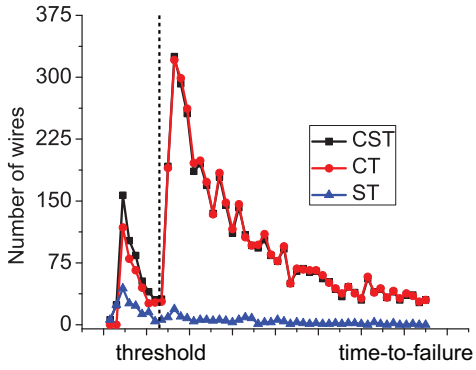


Fig. 13. Wire distribution in according to failure time. The vertical line divides the critical region from the non-critical region.

VI. Experimental Results

All our experiments are performed on Linux 2.4 GHz processor and our algorithm implemented in C++. In our experiments we consider the size of the TSV to be $4\mu m$ in diameter. We perform our experiments on a 4 die 3D stack. We also analyze the impact of TSV on M2 wires near the TSV. Our method however can be applied to analyzing all wires in a given design.

We discuss some of the simulation times needed to analyze stress and model T_f for a given wire. To perform FEM-based simulation for a single TSV and wire structure can take about 40-50 minutes on a single processor in ANSYS. In addition, to model T_f of a wire based on the results of stress simulation can take about 2-3 minutes in COMSOL. Such simulation times make it impractical to use FEM based solvers to analyze thousands of wires in a 3D IC layout.

A. Full chip results

In Figure 10, we plot the result of how hydrostatic stress would vary for vertical wires on a given die. The result would be different for horizontal wires, however, it can be computed easily using symmetry. We observe that variation in stress, which causes stress gradients, occurs in regions that are close to the TSVs. To see the impact of different libraries, i.e. CST, CT, and ST library, we perform full chip analysis for different circuits as discussed in Section V. The results are shown in Figure 11 and Table II. In Figure 11 (d) we plot the failure map when we consider current, stress, and temperature. The effect of ST library, and CT library is shown in Figure 11 (e), (f) respectively. We observe that ST library effects regions that are close to the actual TSV location. Detailed results are shown in Table II. We show the number of TSVs, total wire-length, and number of critical

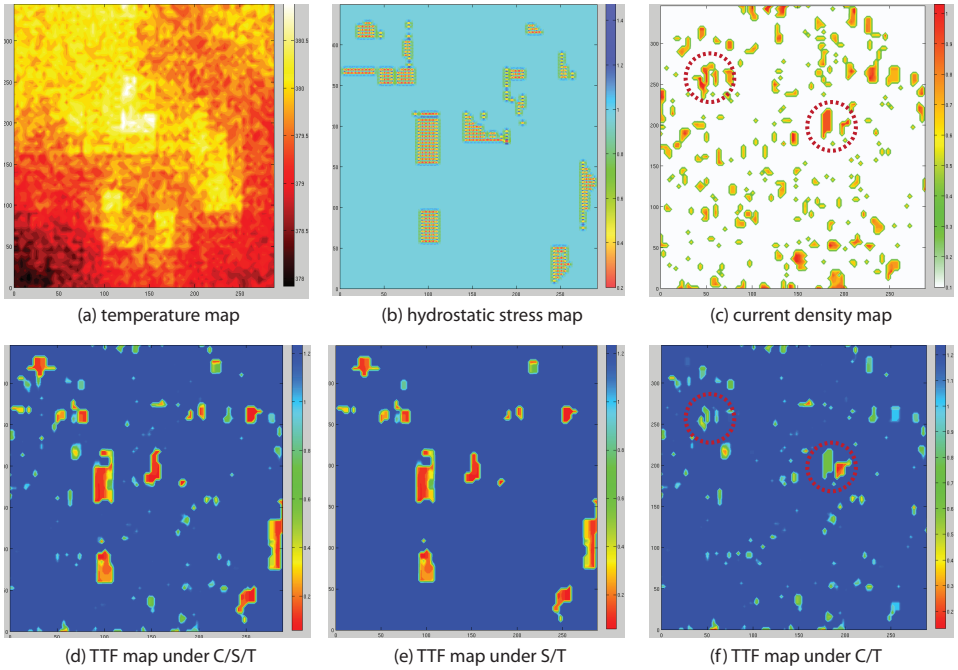


Fig. 11. (a) Temperature map. (b) Map of variation of hydrostatic stress for vertical wires. (c) Map of current density. (d) Map of critical wires when considering current,stress, and temperature. (e) Map of critical wires when considering stress, and temperature. (f) Map of critical wires when considering current, and temperature. Circled regions in (c) and (f) show that high current density region correspond to critical locations.

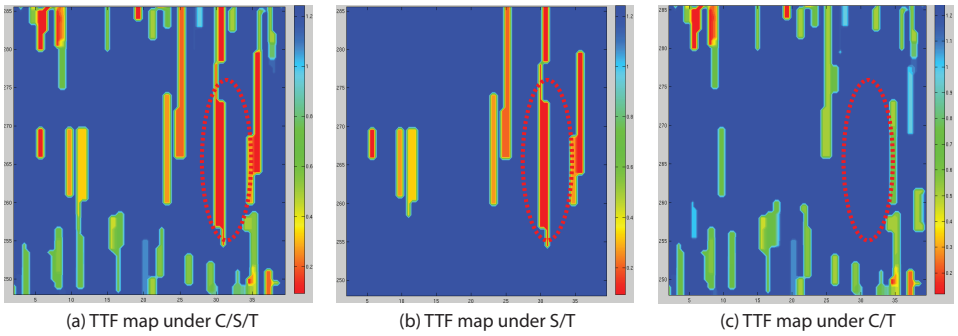


Fig. 12. Zoom in image of the layout shown in Figure 11. (a) Map of critical wires when considering current,stress, and temperature. (b) Map of critical wires when considering stress, and temperature. (c) Map of critical wires when considering current, and temperature. Highlighted regions shows a failure hot-spot that occurs due to TSV induced stress.

TABLE II
COMPARISON BETWEEN CST, CT, AND ST LIBRARIES. EM_f IS THE NUMBER OF CRITICAL WIRES.

			EM_f		
ckt	# TSV	Total wirelength (um)	CST	CT	ST
ckt1	934	3.33×10^5	503	418	150
ckt2	1034	3.95×10^5	384	294	123
ckt3	1107	7.95×10^5	497	436	98
ckt4	1336	2.19×10^6	713	628	138

TABLE III
IMPACT OF ROUTING BLOCKAGES ON EM RELIABILITY OF 3D IC. WE COMPARE THE NUMBER OF EM FAILURES EM_f AND IMPACT ON TOTAL WIRE-LENGTH WL (μm).

		No Routing Blockage		Routing Blockage	
ckt	# Gate	EM_f	WL	EM_f	WL
ckt1	14864	503	3.33×10^5	435	3.34×10^5
ckt2	19895	384	3.95×10^5	224	3.96×10^5
ckt3	29706	497	7.15×10^5	378	7.17×10^5
ckt4	103991	713	2.19×10^6	587	2.22×10^6

wires found using each type of library. In Figure 12, we show a zoom-in image of the layout. We can see that all critical regions obtained by the ST library include regions that overlap with the TSVs.

In Figure 13, we show how failure time T_f varies for wires in given circuit based on the CST, CT, and ST library. We observe that the ST library affects a small number of wires that are in the critical region. As the failure time increases the number of wires in the CST and CT library tend to converge.

B. *Effect of routing blockage*

To improve the EM-reliability of M2 wires in 3D ICs, we add routing blockages as discussed in Section V-A over the TSV. We perform our experiments on four different benchmarks. The results

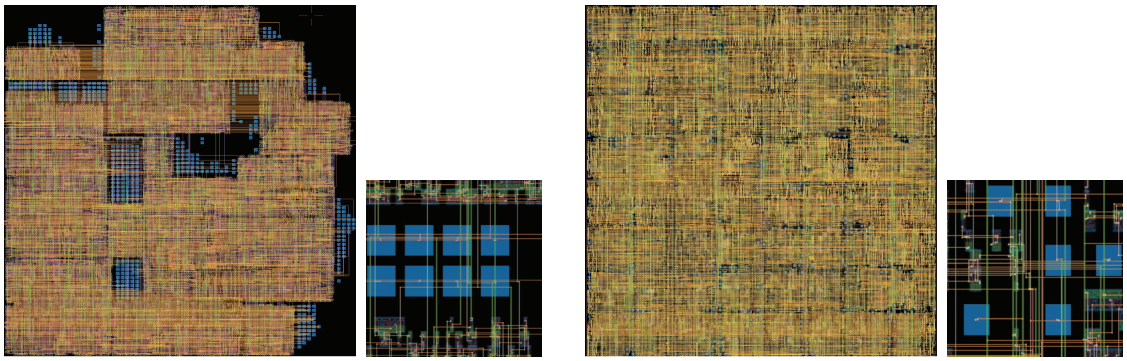


Fig. 14. GDSII layout shots of our block-level vs gate-level designs.

TABLE IV
GATE VERSUS BLOCK-LEVEL 3D ICS. WE COMPARE NUMBER OF TSVS, WIRE-LENGTH, AREA, AND NUMBER OF CRITICAL WIRES (EM_f) FOR BOTH DESIGN STYLES.

type	ckt	# TSV	Wirelength (um)	Area (um^2)	# EM_f
gate-level	ckt1	847	12.65×10^5	133280	384
	ckt2	1715	3.33×10^6	284387	673
block-level	ckt1	1214	12.43×10^5	90000	315
	ckt2	1478	3.41×10^6	253724	598

are shown in Table III. We compare the number of wires likely to fail EM_f and the wire-length. As seen in Table III, adding routing blockages reduces the number of wires that may fail. Due to routing blockages there are zero M2 wires that go over the TSV, in addition there are fewer wires that get affected by TSV induced stress thus increasing the reliability. The impact on total wire-length is less than 1%.

C. Gate-level versus block-level

In this section, we compare two design techniques to generate 3D ICs. We compare gate-level, and block-level 3D ICs. The block-level designs are built using our own 3D-floorplanning tool, whereas, gate-level designs are built using [10]. The results are shown in Table IV. We use the CST library for all analysis. We observe that even though gate-level design use a fewer number of TSVs they tend to have more wires that fail. We believe this occurs because gate-level designs have more wires that go over or near the TSVs, as compared to block-level designs that have fewer wires that go near the TSVs. Figure 14 shows an example layout obtained for block-level and gate-level designs.

VII. OBSERVATION AND FINDINGS

The major observations of this paper can be summarized as follows:

1) The TSV-induced stress gradients can impact the reliability of the wires.
2) EM reliability of wires is affected by current, stress gradients, and temperature. To accurately model reliability of wires in 3D ICs all three forces need to be considered.
3) We proposed an effective way to build stress and reliability libraries. Our method builds on four simple cases, and by using symmetry can be extended to perform quick full-chip reliability analysis.
4) TSV-induced stress can cause failure in metal wires even when the chip is turned off. We build libraries three libraries, i.e., CST, ST, and CT library. Based on these libraries we show the importance of current and stress gradients in 3D integrated circuits.
5) We show that by avoiding routing near the TSV locations we can reduce the impact of failure caused by TSV-induced stress gradients.

VIII. CONCLUSION

In this paper we show that TSVs in 3D IC can impact the stress gradients in metal wires near them. The change in stress in metal wires can lead to stress gradients that can impact the failure time of the metal wires. We showed how we can build an effective library to determine stress on wires due to TSVs. In addition, we proposed a method to perform fast full-chip EM analysis for 3D ICs while considering the effect of TSV stress. For future work, we would focus on determining different techniques that would help avoid or reduce the impact of TSV stress on electromigration reliability.

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