Full-Chip Through-Silicon-Via Interfacial Crack Analysis and Optimization for 3D IC

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***Abstract*—In this work, we propose an efficient and accurate full-chip through-silicon-via (TSV) interfacial crack analysis flow and design optimization methodology to alleviate TSV interfacial crack problems in 3D ICs. First, we analyze TSV interfacial crack at TSV/dielectric liner interface caused by TSV-induced thermo-mechanical stress. Then, we explore the impact of TSV placement in conjunction with various associated structures such as landing pad and dielectric liner on TSV interfacial crack. Next, we present a full-chip TSV interfacial crack analysis methodology based on design of experiments (DOE) and response surface method (RSM). Finally, we propose a design optimization methodology to mitigate the mechanical reliability problems in 3D ICs.**

I. Introduction

Due to the coefficients of thermal expansion (CTE) mismatch between a TSV fill material such as copper (Cu) and silicon (Si) substrate, thermo-mechanical stress is induced during fabrication process and thermal cycling of TSV structures. This stress can affect device performance [1] and drive crack growth in 3D interconnects [2]–[4]. Most previous works focused on modeling the thermo-mechanical stress and reliability of a single TSV in isolation. These simulations are performed using finite element analysis (FEA) method which is computationally expensive or infeasible for full-chip analysis. Furthermore, some works used unrealistic TSV structures such as an extremely large landing pad (LP), mainly because the design context is not considered.

Even though there are several works on thermo-mechanical reliability issues induced by TSV stress, this is the first work addressing TSV interfacial crack in a full-chip scale to the best of our knowledge. In this paper, we propose a fast and efficient full-chip TSV interfacial crack analysis flow based on DOE and RSM. We use energy release rate (ERR) as a mechanical reliability metric, and show the impact of TSV placement style on ERR.

The main contributions of this work include the following: (1) Modeling: Compared with existing work, we simulate more detailed and realistic TSV structures and study their impact on TSV interfacial crack. (2) Full-chip analysis: We employ DOE and RSM to generate ERR models of TSV interfacial crack for full-chip analysis. We validate our methodology against FEA simulations. (3) Design optimization: We present design methods to reduce ERR for TSV based 3D IC designs.

II. Preliminaries

A. TSV Interfacial Crack

TSVs pose a significant challenge to thermo-mechanical reliability of 3D ICs. In particular, CTE mismatch between the conducting metal in TSV and silicon substrate can generate thermal stress inside and around TSVs. Such stress can induce cohesive crack in the silicon substrate [5] and drive interfacial crack between TSV and dielectric liner [2]–[4].

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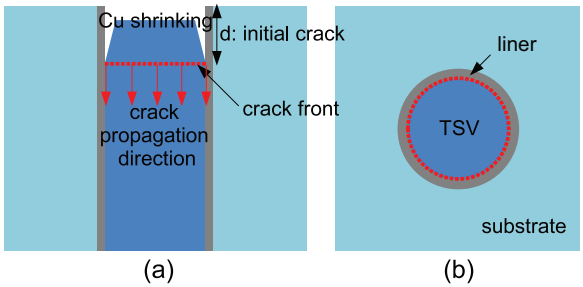

Fig. 1. TSV interfacial crack structure under negative thermal load. (a) Side view with initial crack length of d. (b) Top view.

It is widely known that most of the mechanical reliability failures occur at the interface between different materials. Thus, in this work, we focus on TSV interfacial crack at the TSV/dielectric liner interface. This TSV interfacial crack can cause not only mechanical reliability problems, but functional failures due to leakage.

However, it is hard to obtain realistic crack structures and crack growth behavior models after crack initiation without measurement data. Even with the same initial crack, every crack can grow in a different manner depending on the surrounding environment. Therefore, we adopt a crack structure well studied from previous works [3], [4]. Figure 1 shows our TSV interfacial crack structure. This crack initiates around the circumference of the TSV near the wafer surface and grows vertically downward. In our study, wafer surface means the dielectric layer surface right below dielectric layer (SiO_2)/ILD (low K) interface shown in Figure 2. Also, we assume that crack front propagates uniformly to simplify crack modeling.

B. Energy Release Rate

Energy release rate (ERR) is defined as the energy dissipated during fracture, i.e., crack, per newly created fracture surface area. In other words, ERR is the measure of the amount of energy available for fracture. If high energy is available around crack front, then there is a high chance of crack growth.

However, even with an initial crack, if ERR of the crack under consideration is lower than a threshold value, crack does not grow further and stays in a stable state. The debonding energy between different materials is this threshold, and its value is material and fabrication process specific. For example, debonding energy of Cu/SiO_2 interface ranges from 0.7 to 10 J/m^2 depending on fabrication process [2].

Since loading in our simulation structure is solely due to thermal expansion from fabrication process with no work done by external loads, ERR can be determined as the rate of change in strain energy with crack extension [2]. In TSV based 3D ICs, this strain energy is mostly generated from the thermo-mechanical stress induced by

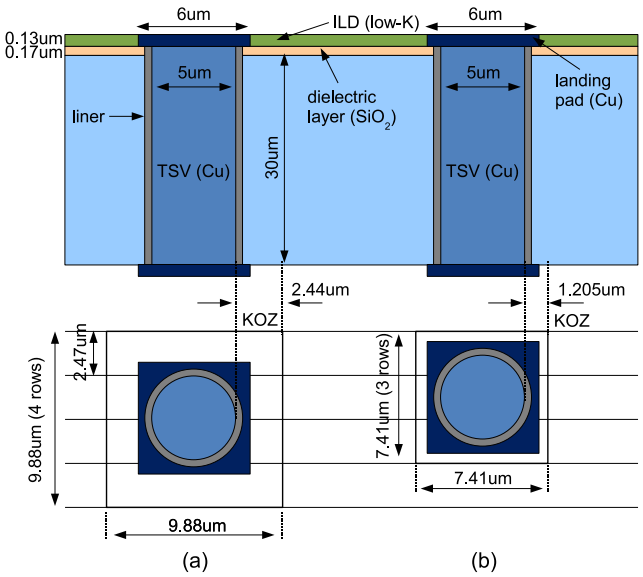

Fig. 2. Baseline TSV structure. (a) TSV_A cell occupying four standard cell rows (KOZ = 2.44 μm). (b) TSV_B cell (KOZ = 1.205 μm).

TSVs. Based on this, two 3D FEA models are created for strain energy analysis, one with a crack length of d, and another with a crack length of $d + \Delta d$. We obtain ERR for TSV interfacial crack using forward difference approach as follows:

$$ERR = -\frac{\partial U}{\partial A} = -\frac{U_{d+\Delta d} - U_d}{2\pi r_{TSV} \cdot \Delta d}$$

where, U is a strain energy, A is area, d is an initial crack length, Δd is a crack increment, and r_{TSV} is TSV radius. In this work, we set d as 1 μm and vary Δd from 0.1 to 0.5 μm to capture crack initiation from the wafer surface as well as near surface thermal stress impact [4].

III. TSV Interfacial Crack Modeling

To the best of our knowledge, there is no work on TSV interfacial crack considering nearby TSVs. The work in [5] investigated cohesive crack in Si substrate with straight and zigzag TSV lines containing five TSVs, and showed that the zigzag type is a better choice to mitigate crack driving force than the straight line. However, this work was performed based on a 2D stress model. Thus, it does not capture the 3D nature of a stress field near a wafer surface around TSVs where devices are located [4]. Also, they did not consider dielectric liner and landing pad in TSV structures, which are essential components for TSV.

Although authors in [4] proposed a semi-analytic ERR model for TSV interfacial crack, it is only valid for an infinitely long TSV. Also, their model is only applicable to a single TSV in isolation and their TSV structure includes only TSV and silicon substrate. Thus, it cannot be directly used to assess TSV interfacial crack considering multiple TSVs as well as a TSV which contains a landing pad and a dielectric liner because of the change in boundary conditions.

Before discussing detailed crack modeling, we introduce two terminologies: (1) **Victim TSV**: TSV with an interfacial crack. (2) **Aggressor TSV**: TSV located nearby a victim TSV and affecting crack growth of the victim TSV.

A. 3D FEA Simulation

Since there is no known analytical ERR model for a realistic TSV structure, 3D FEA models for a TSV interfacial crack analysis are created to investigate the impact of aggressor TSVs on interfacial crack of a victim TSV. To realistically examine the interfacial crack, our baseline simulation structure of a TSV is based on the fabricated and the published data [6], as shown in Figure 2.

We construct two TSV cells, i.e., TSV_A and TSV_B, which occupy four and three standard cell rows in 45 nm technology. We define 2.44 μm and 1.205 μm from TSV edge as keep-out-zone (KOZ) in which no cell is allowed to be placed for TSV_A and TSV_B cells, respectively. Our baseline TSV diameter, height, landing pad width, and liner thickness are 5 μm, 30 μm, 6 μm, and 125 nm, respectively, unless specified, which are close to the data in [6]. We use SiO_2 as a baseline liner material, and ignore Cu diffusion barrier material such as Ta and Ti in these experiments. In general, this barrier thickness is negligible compared with SiO_2 liner, hence its impact on stress distribution is negligible.

Material properties used for our experiments are as follows: CTE (ppm/K) for Cu = 17, Si = 2.3, SiO_2 = 0.5, and BCB = 40; Young's modulus (GPa) for Cu = 110, Si = 130, SiO_2 = 71, and BCB = 3. We use the FEA simulation tool ABAQUS to perform experiments. We apply ΔT = -250°C of thermal load for entire simulation structures. That is, we assume TSV structure is annealed at 275°C and cooled down to 25°C to represent the manufacturing process [4], [5], [7]. We also assume that the entire TSV structure is stress free at the annealing temperature.

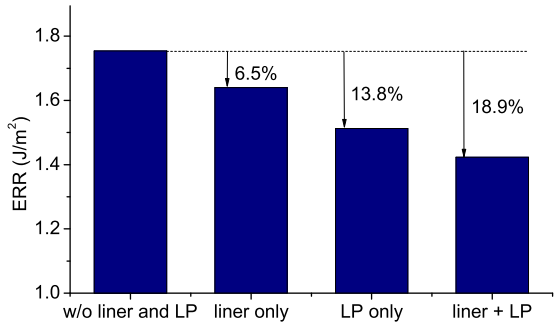

Fig. 3. Impact of TSV surrounding structures on ERR.

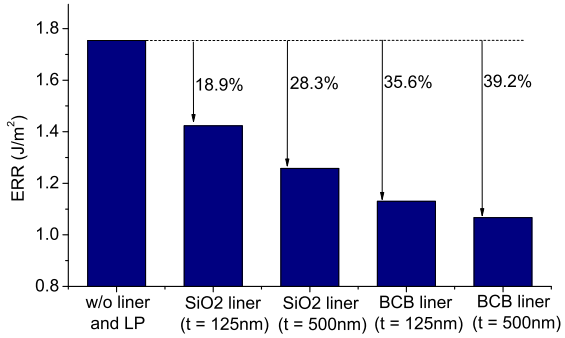

Fig. 4. Impact of TSV liner on ERR. Landing pad width of 6 μm is used with each liner case.

B. Impact of TSV Liner and Landing Pad

We first explore the impact of surrounding structures such as a liner and a landing pad. For this experiment, we use simulation structures without aggressor TSVs. Figure 3 shows ERR of a victim TSV with four different configurations. First, we observe that 125 nm thick SiO_2 liner, which acts as a stress buffer layer, reduces ERR by 6.5 % compared with the case without landing pad and liner.

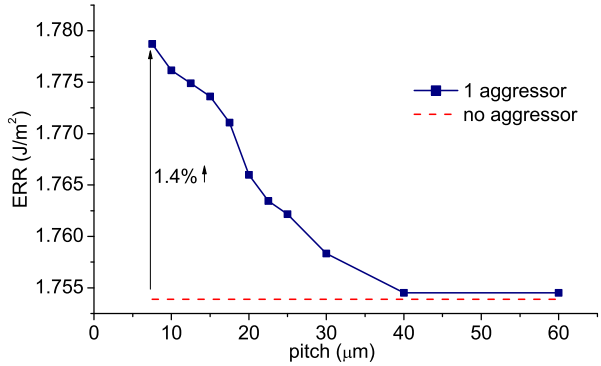

Fig. 5. Impact of TSV pitch on ERR.

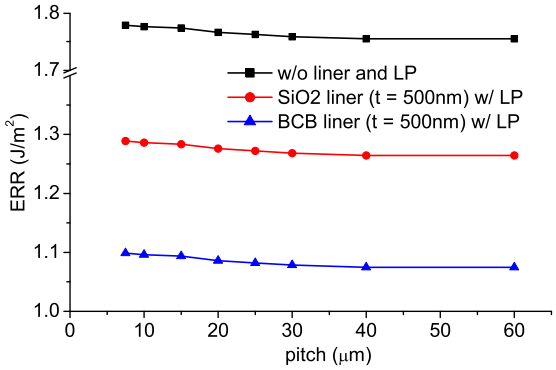

Fig. 6. Impact of TSV pitch with liner and landing pad (6 μm) on ERR.

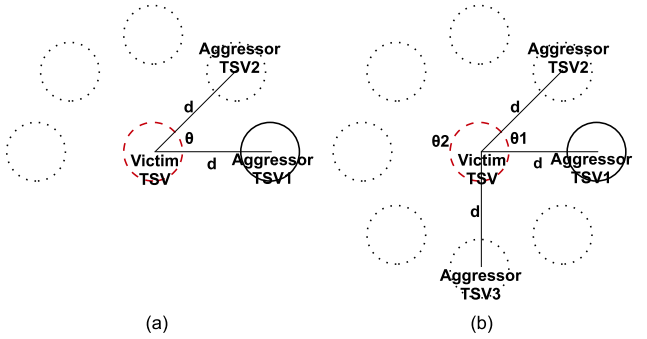

Fig. 7. Simulation structure for angular dependency. Distance from victim to all aggressors is d. (a) Two aggressor TSVs. Aggressor 1 is fixed and aggressor 2 rotates. (b) Three aggressor TSVs. Aggressor 1 is fixed and aggressor 2 and 3 rotate.

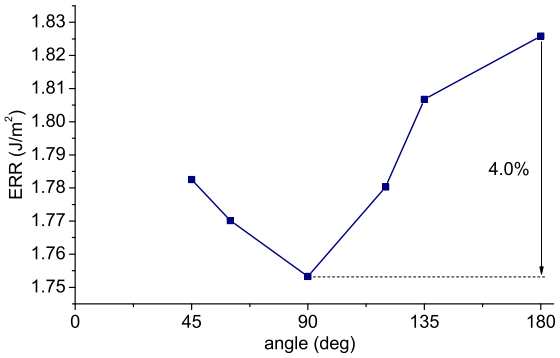

Fig. 8. Impact of angle between victim and two aggressor TSVs on ERR.

The landing pad also helps decrease ERR by preventing TSV/liner interface from separating. Finally, when both SiO_2 liner and landing pad are considered, ERR decreases by 18.9 %.

We also employ benzocyclobutene (BCB), a polymer dielectric material, as an alternative TSV liner material [4], [5]. Since Young's modulus, which is a measure of the stiffness of an isotropic elastic material, of BCB is much lower than Cu, Si, and SiO_2, this BCB liner can absorb the stress effectively caused by the CTE mismatch. Figure 4 shows the impact of liner material and thickness on ERR. For this experiment, we set landing pad width as 6 μm for all cases. As liner thickness increases, ERR decreases noticeably for both liner materials. Also, BCB liner outperforms SiO_2 on reducing ERR.

We examine the impact of landing pad size on TSV interfacial crack as well. We use four landing pad widths; 6, 8, 10, and 12 μm. We observe that ERR is lower with landing pad than ERR without landing pad case for all landing pad sizes. We also see that for landing pad width up to 10 μm, ERR increases and then saturates. This is because the magnitude of all normal stress components at TSV/liner interface underneath landing pad increases due to increased Cu volume with enlarged landing pad area, which is an additional CTE mismatch source. Thus, for TSV interfacial crack, larger landing pad size is not beneficial.

C. Impact of Pitch and Angle among TSVs

In this section, we investigate the impact of TSV pitch on TSV interfacial crack. With fixed victim TSV location, we vary TSV pitch between a victim and an aggressor from 7.5 μm to 60 μm. As Figure 5 shows, ERR decreases monotonically as the pitch increases and approaches to the level when there is no aggressor at around 40 μm pitch. However, when only one aggressor is considered, ERR increase at the minimum pitch compared with the maximum pitch is only 1.4 %, which is negligible. Figure 6 shows ERR curve with two 500 nm thick liner materials and 6 μm wide landing pad. The magnitude of ERR decreases when we use a liner and a landing pad, but overall ERR trend remains similar.

As we introduce additional TSVs, both distance and angle between TSVs become important to TSV interfacial crack. Stress at a point can be computed by adding individual stress tensors induced by each TSV at this point. Depending on relative angle between TSVs, even with the same pitch, stress at the point can be either added up or canceled out. Since this stress directly affects strain energy of a TSV structure, ERR value also varies over different angles.

Now we perform experiments with two aggressors which are located at 10 μm distance from the victim TSV. Then, we vary angle among three TSVs from 45° to 180° to explore impact of angle on ERR of the victim TSV shown in Figure 7(a). As Figure 8 shows, ERR is minimum when three TSVs form 90° angle, and increases as angle approaches to either 45° or 180°. If we plot σ_{xx} stress component in Cartesian coordinate system, TSV structure with negative thermal load creates tensile stress along the x-axis and compressive stress along the y-axis. Thus, if a victim and aggressors form 90°, tensile and compressive stress from each aggressor TSV cancels out at the victim TSV location, that is why we see lowest ERR at 90°.

D. Relative Importance of Pitch over Angle

In this section, we explore the combined effect of TSV pitch and angle. We first use two aggressor TSVs, and change both pitch and angle. We also employ DOE, which will be discussed in detail in Section IV, to produce simulation points shown in Figure 9. Figure 10

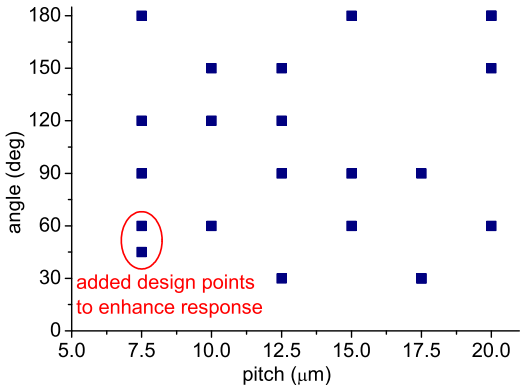

Fig. 9. DOE based simulation points of two aggressor TSVs.

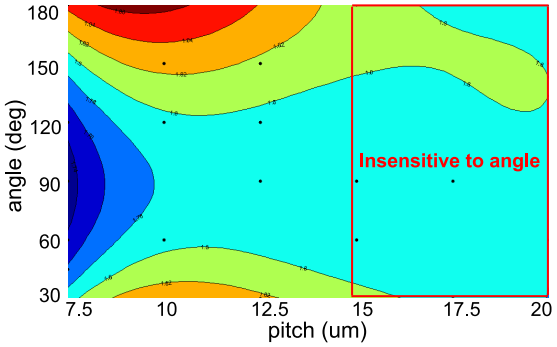

Fig. 10. ERR contour map of pitch and angle.

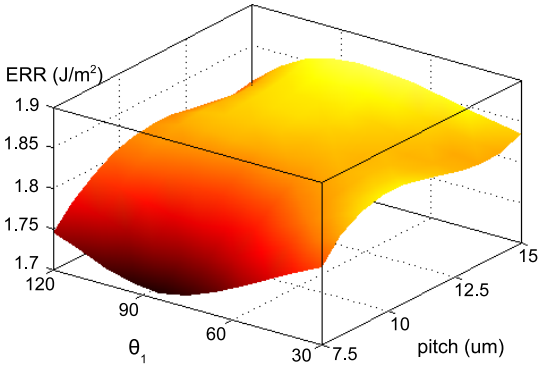

Fig. 11. ERR surface map of pitch and θ_1 in three aggressor TSVs case.

shows an ERR contour map for different pitch and angle. We observe high angular dependency in a small pitch region. However, as the pitch exceeds 15 μm, impact of angle is almost negligible.

To further investigate the relative importance between pitch and angle, we now use three aggressor TSVs shown in Figure 7(b). As Figure 11 shows, angular dependency is dominant for small pitches. However, as the pitch increases, even though there are still some fluctuations along angle axis, angular dependency of ERR is not significant. We also perform simulations with more aggressors up to eight aggressors. We find that angular dependency is almost not noticeable beyond 10 μm pitch, and the number of aggressor TSVs as well as TSV pitch mostly determine the ERR value of the victim TSV.

IV. DOE and RSM based Full-Chip TSV Interfacial Crack Modeling

FEA simulation of TSV interfacial crack with multiple TSVs requires huge computing resources and time. In our simulations, depending on the number of TSVs and mesh structure, single FEA simulation takes about 1 to 12 hours using four CPUs. Thus, it is not feasible for full-chip analysis.

Meanwhile, DOE has been used for many science and engineering applications. Recently, DOE was even used for co-optimization of power network, thermal TSV, and micro-fluidic channel in 3D ICs [8]. It has been proven to be an effective technique when analysis is desired for complex systems with multiple input factors. It provides a well-organized way of performing experiments so that we can use the experimental results to find meaningful relations between input factors and responses of the system. In this section, we present a design of experiments (DOE) and response surface method (RSM) based full-chip TSV interfacial crack analysis flow.

In general, TSV placement style is largely divided into two categories: (1) Regular TSV placement. (2) Irregular TSV placement. In the regular TSV placement scheme, we pre-place TSVs uniformly on each die, and then place cells. In this case, the pitch between TSVs is the most critical factor to predict ERR of a victim TSV. On the other hand, TSVs and cells are placed simultaneously in the irregular TSV placement scheme. The irregular TSV placement shows better wirelength than the regular case [9]. However, in this irregular TSV placement case, possible positions of aggressor TSVs around a victim TSV are innumerable. Thus, it is infeasible to examine all possible TSV arrangements to assess ERR of a victim TSV.

In the following sections, we discuss DOE and RSM based full-chip TSV interfacial crack modeling for both regular and irregular TSV placement styles, and validate our model against FEA simulations. We use *Model-Based Calibration Toolbox* in MATLAB to design experiments and obtain response surface model.

A. Designing Experiments

To use DOE and RSM, we first need to define design knobs (=input factors) and metrics (=responses). We use ERR as our metric to assess TSV interfacial crack in a full-chip scale. However, input factors are different for regular and irregular TSV placement style.

Figure 12 shows two possible regular TSV placement of 5×5 TSV block with a same pitch. In the array type, TSVs are aligned both in horizontal and vertical direction, whereas in the staggered type, TSVs in every other row are shifted by half pitch. For both of these regular TSV placement schemes, the most important factor that determines ERR of a victim TSV is the pitch and the position of the victim TSV inside the block such as center, side, or corner shown in Figure 12. We set TSV pitch as the only input factor and find ERR models for aforementioned critical victim TSV locations separately for regular TSV placement scheme.

Unlike the regular TSV placement style, there are countless possible combinations of TSV placement in irregular TSV placement. However, simulating all these possibilities is impossible. In Section III-D, we identified that relative angle between victim and aggressor TSV is important only when the pitch is small. Also, as shown in Figure 5 and Figure 6, gradient of ERR along pitch is not steep. From these observations, we simplify ERR model for the irregular TSV placement as follows: If the distance between a victim and aggressors is less than 10 μm, we consider both the number of aggressors and angle between them. If the distance exceeds 10 μm, we only count the number of aggressors at each distance bin with 5 μm interval shown in Figure 16. In this way, we remove distance

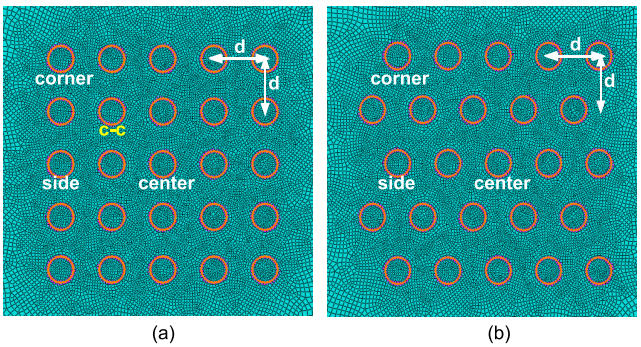

Fig. 12. Top view of meshed simulation structures for 5×5 TSV block. Orange circles are TSVs. (a) Array type. (b) Staggered type.

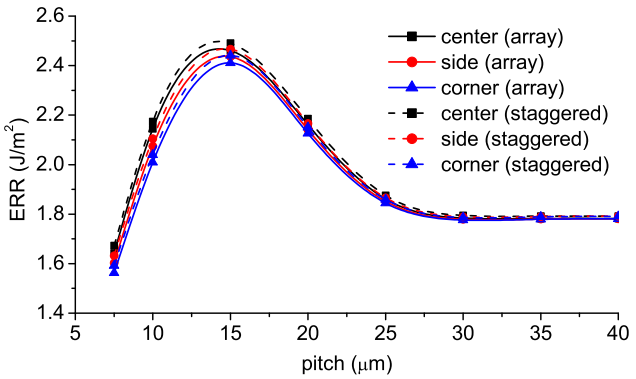

Fig. 13. ERR vs. pitch for array and staggered type.

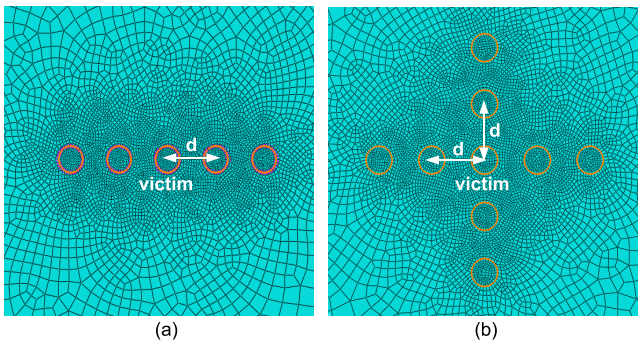

Fig. 14. Top view of meshed simulation structures for (a) line style, (b) cross style.

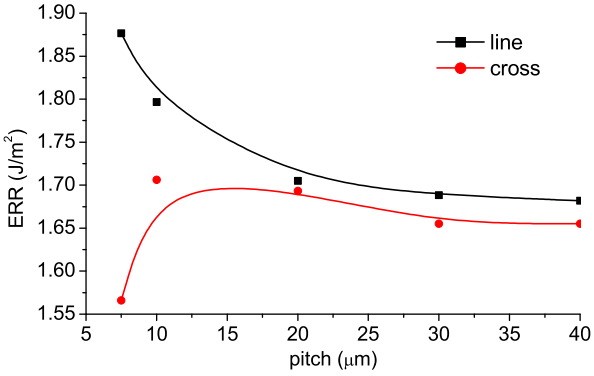

Fig. 15. ERR vs. pitch for line and cross type.

from input factors, and use number of aggressors at each bin and angle of nearest aggressors to design experiments.

We generate design points using Stratified Latin Hypercube from space filling design styles. Based on the design points, we create FEA simulation structures and obtain ERR data from each simulation. With these ERR values, we build the response surface and obtain the analytical ERR model for full-chip TSV interfacial crack analysis.

B. ERR Model for Regular TSV Placement

First, we monitor ERR values of victim TSVs in center, side, and corner location shown in Figure 12. As Figure 13 shows, ERR is highest at the center, and decreases as victim TSV location moves to side. The lowest ERR occurs at corner due to decreased number of aggressors surrounding the victim TSV. We also observe that ERR of the victim TSVs in array type is always lower than the counterpart in staggered type, even though the difference is not significant. This is because large numbers of nearby aggressors are forming 90° angle in array type, hence reduces stress magnitude at the victim TSV location.

Interestingly and counterintuitively, ERR is minimum in the smallest pitch, and increases up to 15 μm, then decreases and finally saturates at around 30 μm pitch. To verify why minimum ERR occurs at the smallest pitch, we build two simulation structures shown in Figure 14. In line style, the victim TSV is only affected by constructive stress interference from aggressors, whereas the victim TSV experiences both destructive and constructive stress interference from aggressors in cross style. As Figure 15 shows, even though there are four more aggressors in cross structure, ERR is always higher in line style for simulated pitches. Most importantly, ERR is minimum at the smallest pitch in cross structure due to highest destructive stress interference. This observation indicates that it is always better to build TSV blocks in array type rather than in line style with a given number of TSVs to help suppress TSV interfacial crack growth. We also observe that ERR difference among three victim TSV locations, i.e., center, side, and corner, is higher in smaller pitches. This is again due to higher stress interference in smaller pitches, which results in larger stress magnitude difference among different victim TSV locations.

We decide to use array type for regular TSV placement ERR model, which shows lowest ERR. We generate 8 design points for regular TSV placement and build RSM model based on FEA simulation results. RSM model can be expressed as a multivariate polynomial equation. In our case, ERR model of regular TSV placement is expressed as a 4^{th} order polynomial with one variable (=pitch) as follows:

$$ERR_{reg} = c_1 + c_2 \cdot d + c_3 \cdot d^2 + c_4 \cdot d^3 + c_5 \cdot d^4$$

where, d is pitch and c_1 - c_5 are TSV dimension dependent coefficients. We build ERR models for center, side, and corner locations separately. We observe that ERR of an intermediate point such as c-c shown in Figure 12(a) can be obtained by averaging ERR values of victim TSVs in center and corner locations with a negligible error. We also generate ERR models for different TSV array blocks, such as 3×3 and 7×7 array.

C. ERR Model for Irregular TSV Placement

As we discussed, there are innumerable scenarios for irregular TSV placement. We reduce the number of input factors by distance binning and considering angular dependency within 10 μm distance range from victim TSV shown in Figure 16. In addition, number of aggressors at each distance bin cannot be arbitrarily large. Also,

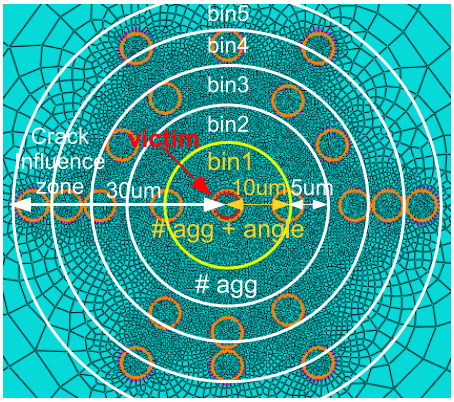

Fig. 16. Top view of meshed simulation structure for irregular TSV placement with 21 aggressor TSVs.

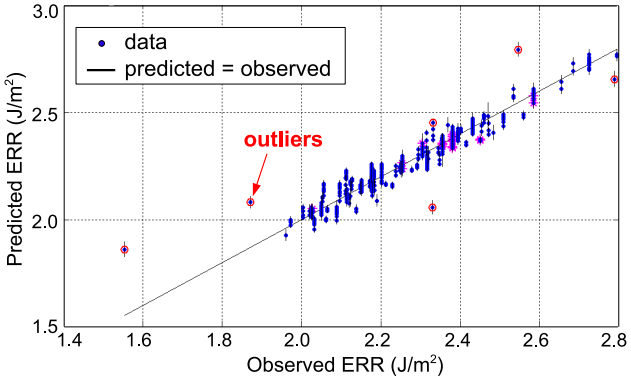

Fig. 17. Predicted ERR using DOE and RSM vs. observed ERR.

as the pitch becomes smaller, possible number of aggressors at that bin is also smaller due to reduced bin area. We generate 50 design points with this constraint. Since we use 13 input factors, 8 for angle (8 aggressors are maximum possible number that can be placed in the bin 1) and 5 for number of aggressors at each distance bin, 50 design points are not enough to obtain high quality RSM model. However, based on the observation that if we rotate entire simulation structure by same angle θ around victim TSV, ERR will remain same since relative positions of TSVs are unchanged, we generate 885 data points from 50 simulations for better response surface fitting.

Figure 17 shows predicted ERR (RSM model) and data points. There are 6 outliers which occur when there are no aggressors at bin 1, hence 8 input factors for angle are not exercised, which causes deviation from the predicted model. This ERR model can be enhanced by simulating more design points on this particular case. However, the proportion of the case with no aggressors at bin1 is less than 6 % (87 out of 1472 TSVs) in the worst case in our benchmark circuits. Also, since the ERR model fits well with data points in general, we use the model without further simulations. ERR model of irregular TSV placement is expressed as a 2^{nd} order polynomial with 13 variables. The details of our ERR model is not shown due to space limit.

D. Quality of ERR Model

The goodness-of-fit of a model can be tested with statistics such as coefficient of determination (R^2), root mean square error (RMSE), and prediction error sum of squares RMSE (PRESS RMSE), which is

TABLE I
QUALITY OF ERR MODEL

Placement type	R^2	RMSE	PRESS RMSE
Regular	0.993	0.034	0.086
Irregular	0.956	0.044	0.098

TABLE II
VALIDATION OF ERR MODEL. SIMULATION CASE SHOWS PITCH FOR REGULAR TSV PLACEMENT AND NUMBER OF AGGRESSORS FOR IRREGULAR TSV PLACEMENT.

Placement type	Simulation case	ERR (model)	ERR (simulation)	Validation RMSE
Regular	9 μm	1.996	1.985	0.033
	12.5 μm	2.401	2.371	
	17.5 μm	2.355	2.335	
	22.5 μm	2.015	1.988	
	27.5 μm	1.789	1.778	
Irregular	10 agg	1.901	1.971	0.055
	21 agg	2.229	2.324	
	28 agg	2.320	2.305	
	36 agg	2.394	2.371	
	43 agg	2.572	2.547	

evaluated by excluding one data point at a time, building a new RSM model, and computing RMSE [8]. Table I shows that R^2 values of our ERR models are close to 1, and both RMSE and PRESS RMSE is less than 0.1. Considering the fact that ERR values from our simulations range from 1.5 to 3.0 in general, quality of fitting is acceptable.

Even though our models match well with simulation data, it is essential to validate whether our ERR models predict unseen data points correctly. We design five new simulation structures to validate ERR models for both regular and irregular TSV placement cases. Table II shows predicted ERR from our model and ERR from simulations. Since regular TSV placement type uses only one input factor, i.e., pitch, validation RMSE is lower than irregular TSV placement case and closer to model RMSE value. Validation RMSE of irregular TSV placement type is also acceptable compared with model RMSE value.

E. Full-chip Analysis Flow

In this section, we briefly summarize our full-chip TSV interfacial crack analysis flow. We assume that each TSV can be a candidate for victim TSV. Thus, while we visit each TSV, we set this TSV as a victim TSV and other TSVs within influence zone as aggressors. In our simulation, we use 30 μm as a crack influence zone, since at around this pitch ERR saturates shown in Figure 13. Then, we find angle and distance between aggressor and victim TSV, and insert aggressor into corresponding distance bin for irregular TSV placement or find pitch for regular TSV placement. Once we prepare this information, we compute ERR using analytical models based on DOE and RSM.

V. FULL-CHIP SIMULATION RESULTS

We implement a full-chip TSV interfacial crack analysis flow in C++. Four variations of a gate-level 3D circuit, with changes in TSV placement style and TSV cell size, are used for our analysis, which are listed in Table III. The number of TSVs and gates are 1472 and 370K, respectively, for all cases to compare impact of placement style on ERR fairly. These circuits are synthesized using Synopsys Design Compiler with the physical library of 45 nm technology, and designed using Cadence SoC Encounter to two-die stacked 3D ICs.

A. Impact of KOZ

We first investigate the impact of KOZ size on ERR of both regular and irregular TSV placement style. Figure 18 shows histogram of

TABLE III
BENCHMARK CIRCUITS

circuit	TSV placement	TSV cell size ($\mu m \times \mu m$)	wirelength (mm)	area ($\mu m \times \mu m$)	pitch (μm)
Irreg_A	Irregular	9.88×9.88	8884	1000×1000	-
Reg_A	Regular	9.88×9.88	9648	1000×1000	25
Irreg_B	Irregular	7.41×7.41	9060	960×960	-
Reg_B	Regular	7.41×7.41	9547	960×960	22

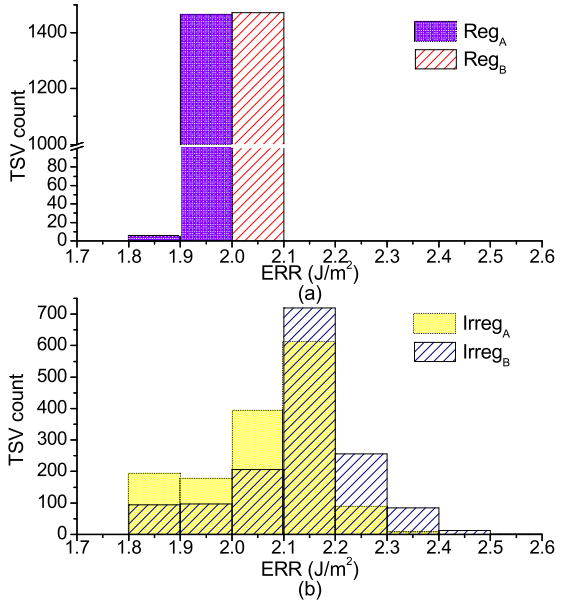

Fig. 18. Impact of keep-out-zone on ERR. TSV_A cell (KOZ = 2.44 μm) and TSV_B cell (KOZ = 1.205 μm) (a) Regular TSV placement. (b) Irregular TSV placement.

number of TSVs for observed ERR ranges. We first observe that ERR values are highly concentrated in a small range in the case of regular TSV placement. Even though there is a difference of ERR between center and corner locations in TSV array for example, that is negligible in the pitch of 22 μm (Reg_B) and 25 μm (Reg_A). Also, KOZ size impact on ERR is not significant for this regular TSV placement case, since both TSV pitches are already close to crack influence zone (30 μm), and their difference is only 3 μm.

On the other hand, irregular TSV placement case shows larger variations of ERR and large number of TSVs experience higher ERR than regular TSV placement case. This is mainly because TSVs can be placed either densely or sparsely to minimize wirelength in the case of irregular TSV placement scheme. Thus, ERR of victim TSV can vary noticeably depending on the placement of nearby aggressor TSVs. Furthermore, since there are regions where group of TSVs are closely placed as shown in Figure 19(a), higher ERR values are observed in irregular TSV placement style. We also see that the KOZ size affects ERR values significantly in irregular TSV placement. This is because number of aggressors at each distance bin decreases due to increased KOZ size, hence reduces stress magnitude at victim TSV.

B. Impact of Liner

We identify that ERR is highly dependent on the liner material and its thickness in Section III-B. In this section, we investigate the impact of liner on ERR in a full-chip scale. We use 6×6 μm^2 landing pad for all cases. Figure 20(a) shows that ERR values of both irregular and regular TSV placement schemes reduce significantly with use of liner. We also observe that liner thickness has a huge impact on the

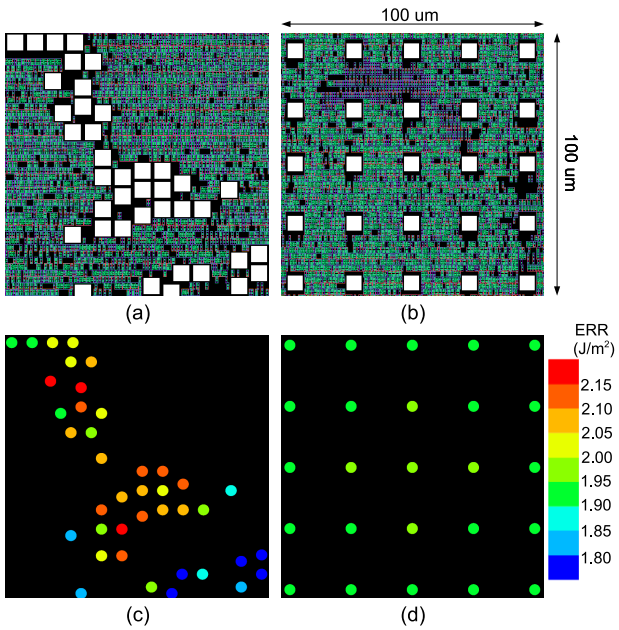

Fig. 19. Close-up shots of layouts and ERR maps. (a) Irreg_B. (b) Reg_B. (c) ERR map of Irreg_B. (d) ERR map of Reg_B.

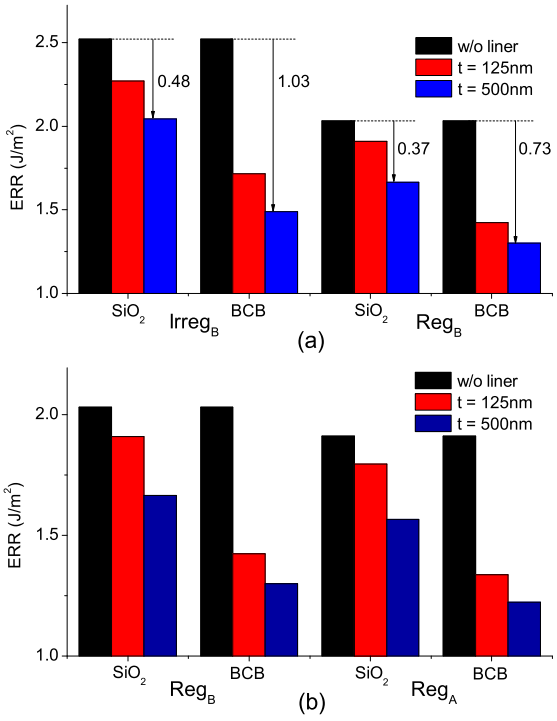

Fig. 20. Impact of liner material and thickness on maximum ERR. (a) Irreg_B vs. Reg_B. (b) Reg_B vs. Reg_A.

maximum ERR magnitude, since the thicker liner effectively absorbs thermo-mechanical stress at the TSV/liner interface. Especially, the BCB liner shows significant reduction in the maximum ERR compared with SiO_2 liner due to extremely low Young's modulus shown in III-A. Furthermore, we see that ERR decrease is higher in irregular TSV placement case compared with regular TSV placement since

TABLE IV
COMPARISON BETWEEN GATE-LEVEL AND BLOCK-LEVEL DESIGN

level	TSV pitch (μm)	# TSV	WL (mm)	area ($\mu m \times \mu m$)	max ERR (J/m^2)	std' dev'
Gate	irregular	1472	9060	960×960	1.489	0.081
	22	1472	9547	960×960	1.300	0.003
Block	7.5	333	7933	980×1090	1.232	0.129
	10	394	8028	1080×1000	1.500	0.160
	15	368	8259	950×1130	1.805	0.270

stress buffer effect of liner is more effective where aggressor TSVs are close to victim TSV.

Figure 20(b) shows that differences of ERR values between Reg_B and Reg_A circuits are not significant with different liner material and its thickness. This is again because pitch difference between Reg_B and Reg_A circuits is negligible and pitch itself is already close to crack influence zone range.

C. Reliability of Block-Level 3D Design

Even though the gate-level 3D design has the potential of highest optimization, the block-level design is attractive in the sense that we can reuse highly optimized 2D IP blocks. In this section, we examine TSV interfacial crack in block-level 3D designs. 3D block-level designs are generated using an in-house 3D floorplanner which treats a group of TSVs as a block shown in Figure 21. We use 500 nm thick BCB liner and 6×6 μm^2 landing pad for all cases. We vary the TSV pitch inside TSV blocks to examine its impact on layout quality as well as reliability issues. Note that the pitch inside TSV block is smaller than regular TSV placement case, in general.

Table IV shows that block-level designs use less number of TSVs, show shorter wirelength, and occupy more area than gate-level designs. Experimental results show that the block-level design with 7.5 μm pitch shows smallest ERR among all cases. This is observed in Figure 13 due to strong TSV-to-TSV stress interference in small pitches. However, it comes with larger variation of ERR across TSVs compared with both irregular and regular TSV placement cases. This is mainly due to the small TSV pitch and different types of TSV blocks used in block-level design such as the line type shown in top-right part of Figure 21(a). Also, it is possible that decreased TSV pitch could worsen signal integrity due to high TSV-to-TSV coupling. Therefore, TSV pitch in block-level designs should be carefully determined considering both mechanical and electrical issues.

D. Summary and Key Findings

In this section, we summarize our work and briefly discuss key findings.

1) We present an efficient full-chip TSV interfacial crack analysis flow based on DOE and RSM. Note that our full-chip TSV interfacial crack analysis methodology is general enough to be applied to other types of crack structures.
2) TSV interfacial crack is affected by TSV placement style, KOZ size, and TSV surrounding structures such as a liner and a landing pad.
3) Irregular TSV placement suffers from higher ERR and larger ERR variation compared with regular TSV placement, hence hard to control TSV interfacial crack problems across a chip.
4) It is recommended to use array type TSV blocks wherever possible for regular TSV placement and block-level design to benefit from ERR reduction by highest destructive stress interference. In addition, TSV pitch inside TSV blocks should be carefully determined by considering both mechanical and electrical issues.

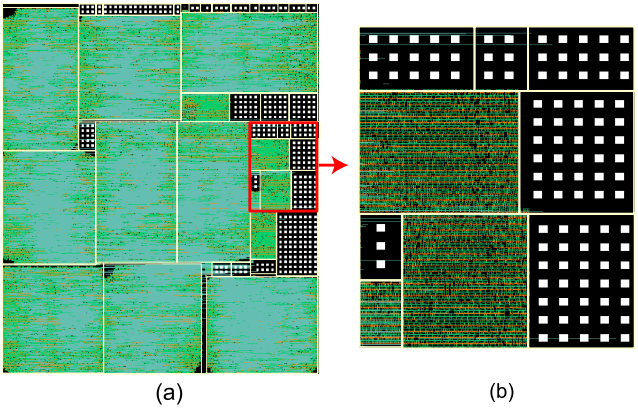

Fig. 21. Layout of block-level design (TSV pitch = 15 μm). White rectangles are TSV landing pads. (a) full-chip layout. (b) close-up shot of the red box in (a).

5) Larger KOZ relieves TSV interfacial crack due to increased spacing among TSVs and decreased number of aggressors affecting victim TSV inside crack influence zone. However, since it comes with larger footprint area, a careful design of KOZ is required.
6) Liner material and thickness are key design knobs to alleviate TSV interfacial crack problem by reducing stress magnitude at TSV/liner interface.

VI. CONCLUSIONS

In this work, we show how TSV placement as well as TSV surrounding structures such as a liner and a landing pad affect TSV interfacial crack in 3D ICs. We also present a DOE and RSM based accurate and fast full-chip TSV interfacial crack analysis flow, which can be applicable to placement optimization for 3D ICs. Our results show that KOZ size, liner material/thickness, and TSV placement are key design parameters to reduce the TSV interfacial crack problems in TSV based 3D ICs.

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