Implications of triple patterning for 14nm node design and patterning

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ABSTRACT

The upcoming 14nm logic node will require lithographic patterning of complex layout patterns with minimum pitches of approximately 44nm to 50nm. This requirement is technically feasible by reusing existing 20nm litho-etch-litho-etch (LELE) double patterning (DPT) methods with very strong restricted design rules. However, early indications are that the cost-effective design and patterning of these layouts will require lithographic methods with additional resolution, especially in two-dimensional configurations. If EUV lithography reaches maturity too late, the 14nm logic node will need other lithographic techniques and the corresponding physical design rules and EDA methodologies to be available. Triple patterning technology (TPT) is a strong option for 14nm node logic on both hole and line-space pattern layers. In this paper we study major implications of a 14nm logic TPT lithographic solution upon physical design, design rules, mask synthesis/EDA algorithms and their process interactions.

Keywords: lithographic design rules, double patterning (DPT), triple patterning (TPT)

1. Introduction and 14nm node background

According to the latest ITRS roadmap [1] (see Figure 1), at the 20nm logic node (with features at a minimum half-pitch of ~32nm) double patterning with 193nm water immersion will be used with NA of 1.35 to perform patterning in high volume manufacturing (HVM) starting in late 2012. The 14nm logic node will have features at a minimum half-pitch of ~22-25nm, and the first industry HVM for these nodes will likely start in 2015. Several pitch splitting optical lithography options have been considered for the patterning of the 14nm device node including litho-etch-litho-etch double patterning (LELE DPT), litho-etch-litho-etch-litho-etch triple patterning (LELELE TPT), and self-aligned spacer double patterning (SADP). Another option is to lower the wavelength by an order of magnitude with EUV systems to use a λ of 13.5nm with an NA of 0.25-0.33. Unfortunately, EUV throughput, mask defectivity and resist performance are not yet ready for manufacturing or integration development. Therefore, the industry is currently mainly focusing on 193nm immersion lithography patterning methods for 14nm logic node development.

In this paper, we first provide background information and analysis of major 193nm immersion lithography options for backend layer patterning of the 14nm logic node. We then discuss the many process requirements and issues for potential TPT patterning of this node. Next we look in more detail at different

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EDA/mask synthesis requirements and algorithms at the 14nm node. Finally, we summarize this work, provide our current conclusions on TPT methods, and recommend future work to perform.

2. Introduction to 14nm node patterning options

Double patterning is a major option chosen by foundries for the 20nm logic node [2]. DPT methods decompose the original design intent into two individual masking layers (i.e., colors), where each of them can be patterned reusing existing 193nm 1.35NA lithography from the 28nm logic node, see Figure 2. Minimum CDs of ~45nm are patterned in resist then shrunk down to ~32nm after etch. As the minimum pitch patterned by single exposure at the 28nm node is ~90nm, DPT can easily pattern a minimum pitch of 64nm for 1D structures. However, not all existing layouts can be shrunk to the 20nm node and maintain DPT compliance (i.e., the polygons can be decomposed into 2 colors, each color meeting minimum spacing rules which are ~2X the smallest space allowed between different colors). Often this is due to 2D layout configurations containing odd cycles which require 3 colors for decomposition [3, 4].

For 1D features, a DPT process can reuse 28nm lithography and achieve a 45nm minimum pitch which would likely be sufficient for the 14nm node. However, for 2D layout configurations, a DPT process for 14nm has major limitations, see Figure 3. Minimum CDs of ~45nm are patterned in resist then shrunk down to ~22nm after etch. The problem is that the space between line-ends grows during this etch shrink and due to 2D effects, it may grow by 2X of the ~23m shrink seen by 1D features. Therefore each color must meet minimum spacing rules which are ~4X the smallest space allowed between different colors. This is a major limitation for area minimization during design.

Another major option for 14nm metal patterning is Spacer is Dielectric (SID) SADP [5, 6, 7], see Figure 4. In this method, a double patterning style coloring is first done to choose features for a mandrel (sacrificial) mask patterned with single exposure. Single CD spacer features are then created around the perimeters of the mandrel patterns and the sacrificial mandrels are removed. The spacer features will become dielectric material on the wafer. Next a 2nd lithography step is performed to pattern a (generally complex) trim mask which adds additional dielectric material in other areas where metal is undesired. The SID SADP method has several advantages vs. LELE DPT including lower sensitivity to overlay errors and smaller allowed 2D space, but it also has challenges including process cost, trim mask complexity and more restricted layout design.

A third option for 14nm backend patterning is TPT [8]. There are many possible TPT methods, e.g., [9], but in this paper we will restrict discussions to LELELE TPT. This method is an extension of DPT to allow 3 colors (i.e., 3 masks) to be used in layout decomposition, see Figure 5. However, as noted above, the advantages of TPT for enabling design shrinks are not for 1D features, but for 2D features such as line-ends or via patterning. For example, Figure 6 shows how TPT can be used to substantially reduce the area required to pattern dense via arrays.

3. TPT process needs and issues

There are several process considerations for the use of TPT which will affect the adoption of this technology. As the design intent for a device layer will be split into 3 advanced masks to transfer the pattern lithographically, the process complexity and cost are increased substantially. Each of the 3 mask exposures will be done using a ~28nm lithography-etch (LE) process, and the filmstack must have multiple hardmask layers for etch transfers. The final wafer pattern will be the superposition of the individual etched patterns from the 3 LE steps. Therefore CD and overlay control for each LE step will be critical in order to ensure that the spacing between features patterned with different LE steps is sufficient. The maximum error allowed for layer-layer overlay control may need to be as small as 3-3.5nm, a very difficult challenge especially considering the complexity of aligning 3 LE steps. As the CD control should generally be within +/-10% of the final etched ~22nm CD, the CD control required for each LE step must

be far better than is needed for ~45nm etched CDs from the 28nm node. This will require substantial improvements in lithography, OPC and RET processes. Achieving good pattern density balance across the 3 lithography steps is important for fine etch control, and is then a requirement for TPT decomposition.

TPT also requires that 3 expensive masks must be manufactured for each TPT device layer, each with significantly improved mask CD control and mask pattern registration. Achieving good pattern density balance across the 3 masks is also expected to be a consideration in mask CD and registration control. Therefore, the total cost of the masks needed for a 14nm TPT layer may be greater than 3X the mask cost of patterning a corresponding single exposure 28nm layer. However, one potential future mask cost enhancement for TPT patterning may come from the faster multi-beam mask writing tools being developed.

4. TPT EDA/mask synthesis options & issues

All pitch splitting methods have limitations on the structures which are compliant for decomposition. Figure 7 shows a comparison of common metal routing structures and their compliance with DPT, SID SADP and TPT. It is clear that TPT can decompose more layout configurations than DPT and SID SADP and this helps to shrink design area. However, it can be seen that TPT cannot decompose every common layout. Figure 8 shows examples of the types of layouts which cannot be decomposed by TPT. In this figure, the colored circles are nodes in a graph, they represent polygons (or portions of polygons) colored during TPT decomposition. Nodes connected by solid lines must be colored with different colors in order to be compliant (i.e., these polygons are at a smaller space than can be resolved with a single LE step). Figures which are not TPT compliant are seen to contain multiple overlapping odd cycles (i.e., triangular shaped connections of nodes) in different forms.

Pitch splitting compliance errors can often be avoided by design modifications, but there are obviously limits to how much a layout can be modified and still achieve good area scaling. Figure 9 shows an example of how an SRAM metal1 layer scaling is limited for DPT and TPT coloring. TPT is seen to provide greater area scaling than DPT but is different in how layout scaling is limited. DPT scaling is mainly limited by scaling the cell horizontally while TPT is limited by both horizontal and vertical scaling.

A considerable challenge for TPT EDA/mask synthesis methods is the inherent complexity of finding a TPT compliant solution. Solving general 3 color graph problems is known to not be solvable in polynomial time, that is, it is an NP-complete problem computationally. Therefore, the graph coloring solution time can increase exponentially with the number of nodes in the network. A pictorially example of the increase in complexity of finding a TPT solution vs. finding a DPT solution is shown in Figure 10. For a square configuration of nodes, there are only two possible coloring solutions which may need to be searched to find the optimum. For the same square configuration however, there are 18 possible solutions. Overall there are 3^{N} possible TPT solutions to search for a coloring graph with N nodes. As a graph with only 30 nodes will have $> 10^{14}$ possible solutions, obviously it is not possible to evaluate them all.

Figure 12 shows a list of different TPT methods that were evaluated for this work. The “poor man’s TPT” method is a reuse of 2 color DPT with the additional step of attempting to remove DPT conflicts by moving polygons at conflict to the 3rd mask color, see Figure 12. This has the advantage of good run time and has sufficient quality for layers with few conflicts. However, this method does not provide good color balance and it does not guarantee finding compliant solutions, even if they exist, for very dense layers like metal1, see Figure 13.

The ILP and SDP methods were compared for TPT run time and decomposition quality. The decomposition quality of ILP and SDP was comparable [10], see Figure 14. Occasionally SDP had an additional conflict compared to ILP. It is not expected that this is a fundamental concern for TPT design flows but needs to be considered if absolute accuracy is needed , e.g., in mask synthesis. The runtime of SDP is orders of magnitude faster than ILP, which will be important for very large scale and dense designs.

The SAT and WCSP methods were evaluated in [8]. These methods were always able to find a compliant solution and were significantly faster than the brute force method. However, the run time of these methods appears adequate only for coloring networks with limited number of nodes, see Figure 15. For the known TPT-compliant Penrose tiling testpatterns used in the study, recent work at the University of Texas, Austin has been able to develop methods of coloring node simplification which has been shown to reduce the run time for TPT decomposition to be linear with the number of nodes, see Figure 16, and can be used together with all the coloring algorithms described. While not applicable to all circuit geometries, this method should help reduce the network sizes for many cases..

5. Summary and conclusions

In this paper, we first provided background information for major 193nm immersion lithography options for backend layer patterning of the 14nm logic node. We discussed the many process requirements and issues for potential TPT patterning of this node. Next we looked at different EDA/mask synthesis requirements and algorithms at the 14nm node. TPT can be seen in this analysis to be a promising technology for the 14nm logic node although many process, cost and algorithm challenges remain. Future mask synthesis work should focus on improving TPT decomposition methods and developing realistic TPT compliant layouts to validate the effectiveness of these methods.

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Figure 1. ITRS from Dec. 2011 showing introduction of ~22nm half-pitch patterning (14nm logic node) for logic devices into volume manufacturing approximately at middle of 2015 [1].

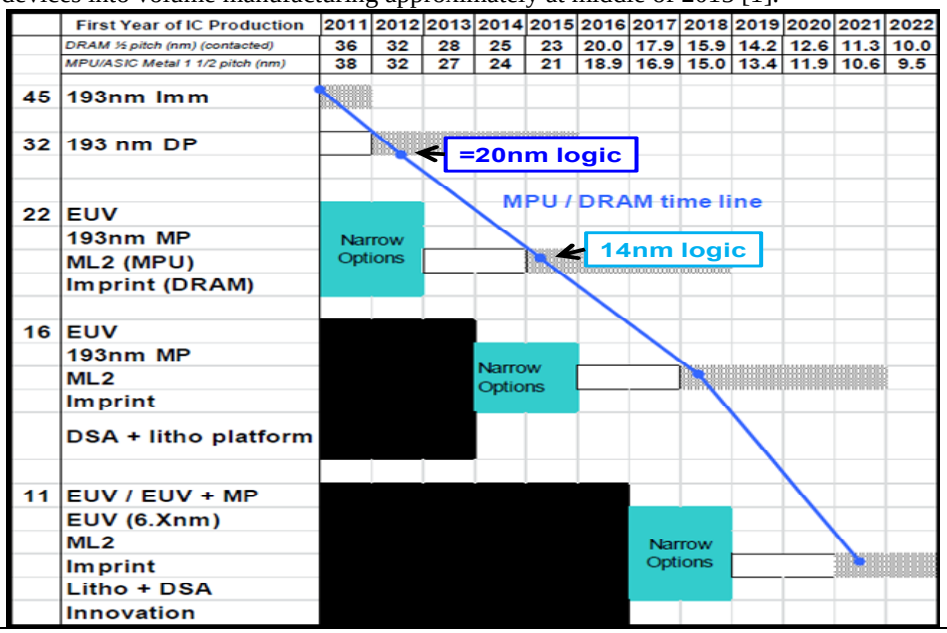


Figure 2. Example showing the flow of LELE DPT design decomposition and patterning. The metal layer design is decomposed into 2 masks (colors) then each is patterned with a ~28nm LE process. [2]

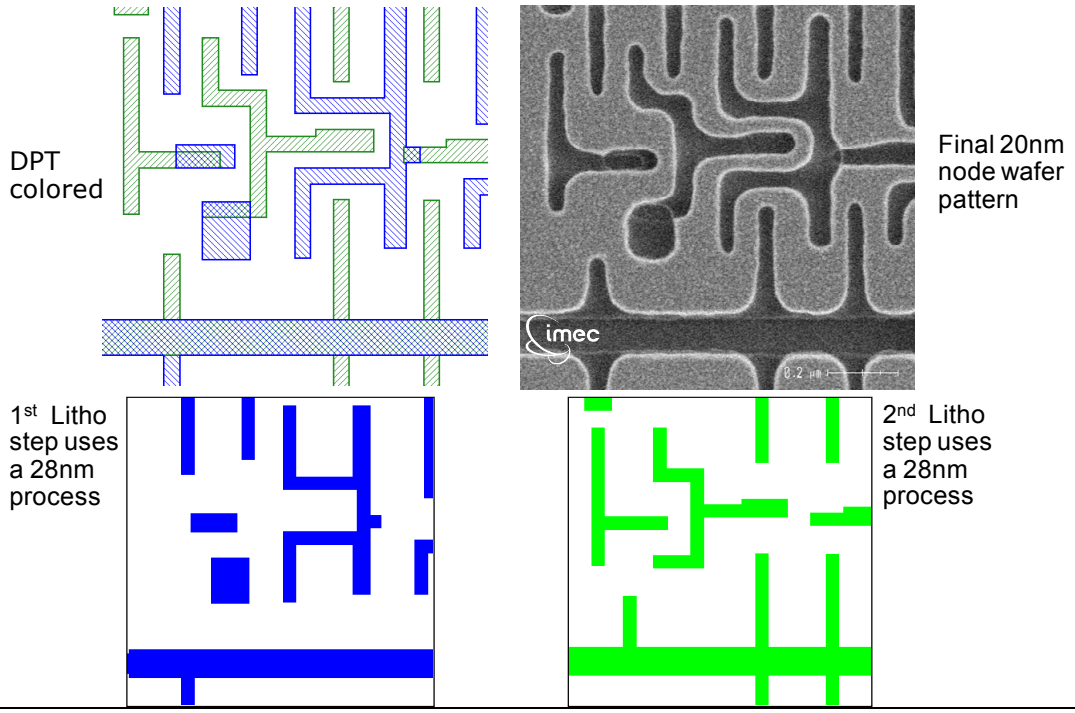


Figure 3. Example showing etch shrink needed for 14nm logic patterning and the impact upon minimum line-end space between features on a single mask. The 45nm resist width features are shrunk to 22nm after etch. If 2 line-ends are patterned even at an aggressive 45nm spacing in resist, the line-end space after etch shrink can expand to ~90nm, hurting design density. This limits the ability to use DPT for routing metal layers at the 14nm node.

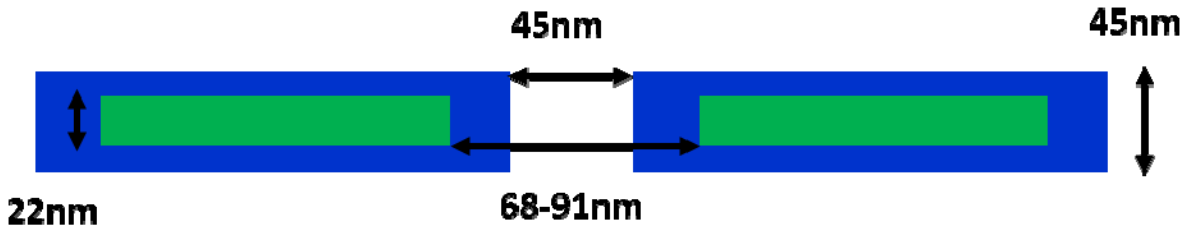


Figure 4. Example of SID spacer decomposition upon SRAM metal1 layer showing the steps of Mandrel coloring, Mandrel patterning, spacer & trim mask generation, and final metal pattern vs. design intent. [6]

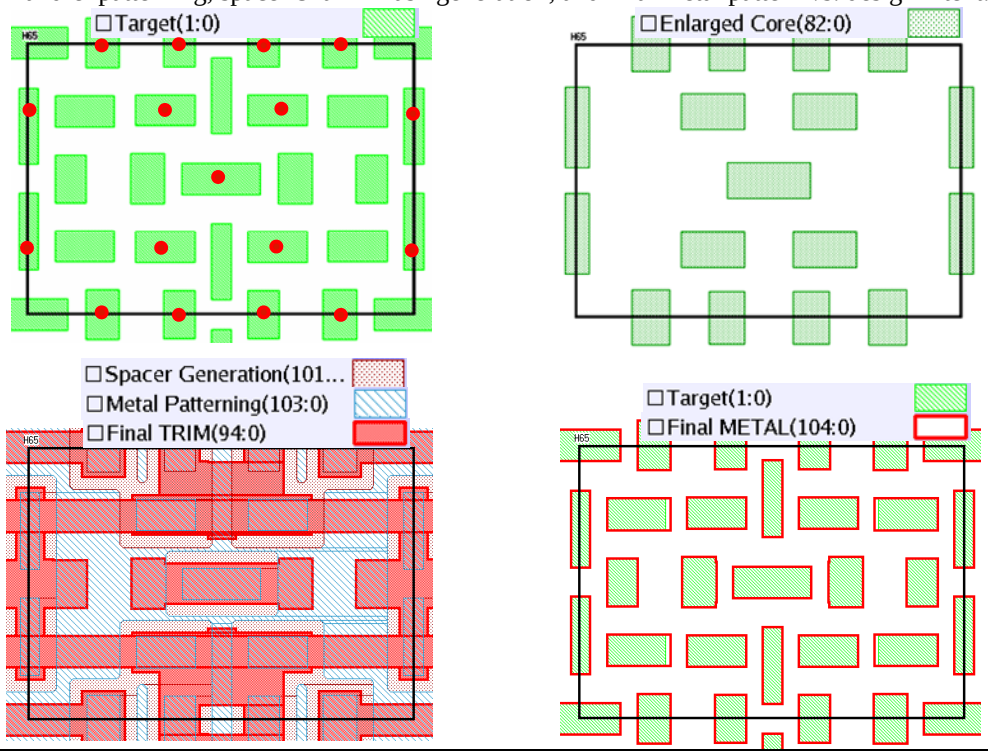


Figure 5. Examples of metal routing configuration in design and with double and triple patterning showing the large potential area shrink benefit of triple patterning for generally 1D features. [8]

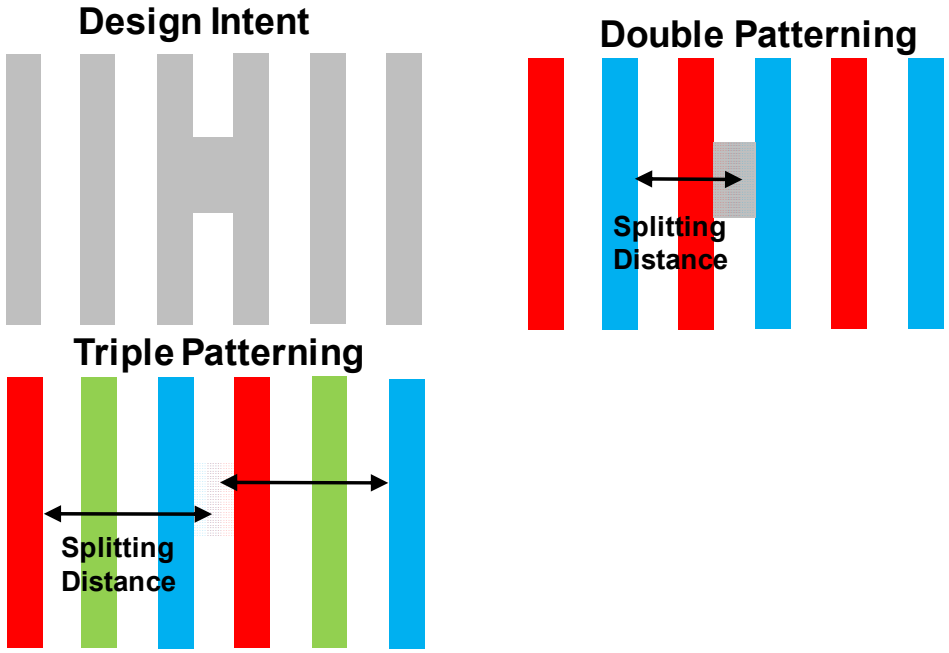


Figure 6. Examples of optimum via configurations for single, double and triple patterning showing the large potential area shrink benefit of triple patterning. [8]

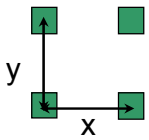
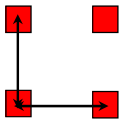
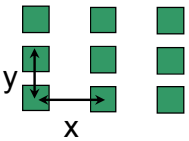
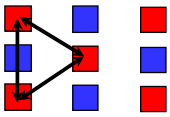
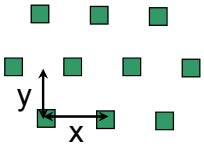
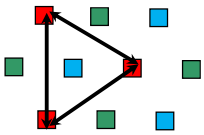
	Design Layout	Split Layout	Design pitch : Splitting pitch ratio	Area
Single Layer: Square Grid			x = 1 y = 1	100%
Double Patterning: Rectangular Grid → Hexagonal Packing	 *Design pitch*	 *Splitting pitch*	x = √3/2 y = 1/2	43%
Triple Patterning: Hexagonal Packing			x = 1/√3 y = 1/2	29%

Figure 7. Examples of routing metal structures and the ability of LELE DPT, SID SADP and TPT to decompose. The figures with X's in the top left corner are not decomposition friendly for that given decomposition method.

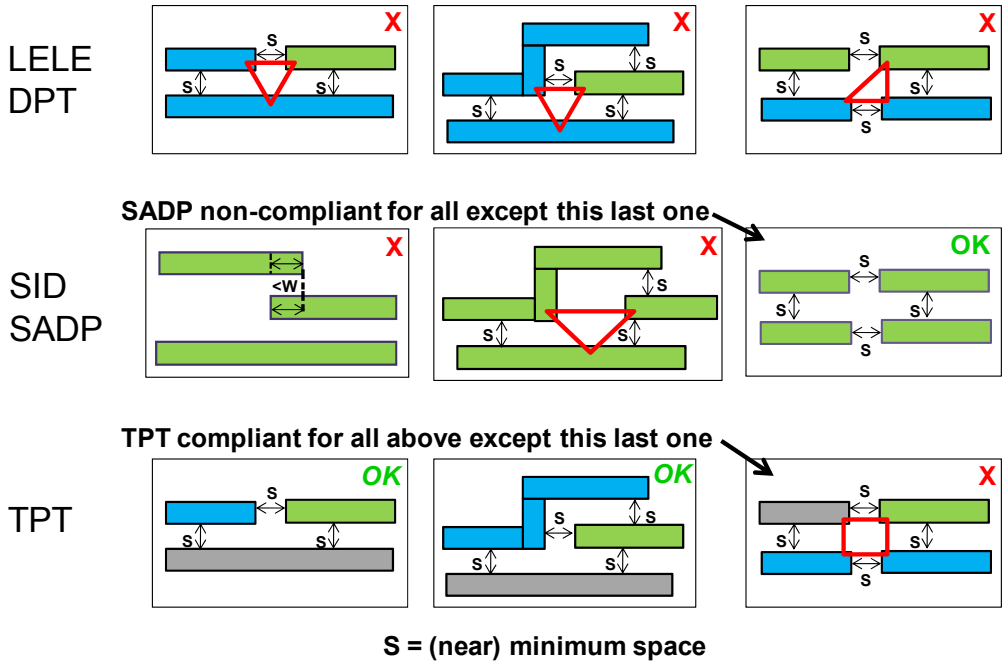
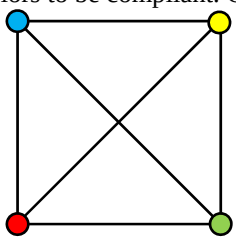
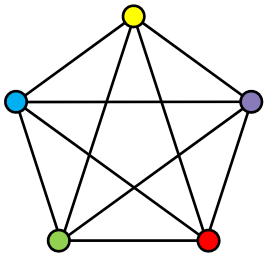


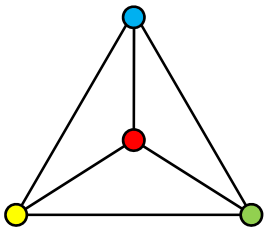
Figure 8. Graphical representation of polygon configurations which are not TPT compliant. The colored circles (nodes) represent polygons to be colored. If 2 nodes are connected by a line they must be colored with different colors to be compliant. Configurations with overlapping odd cycles are not TPT colorable /compliant [8].



Splitting pitch ≥ √2 ~ 1.414 design pitch
- this is 4 odd-cycles aligned together

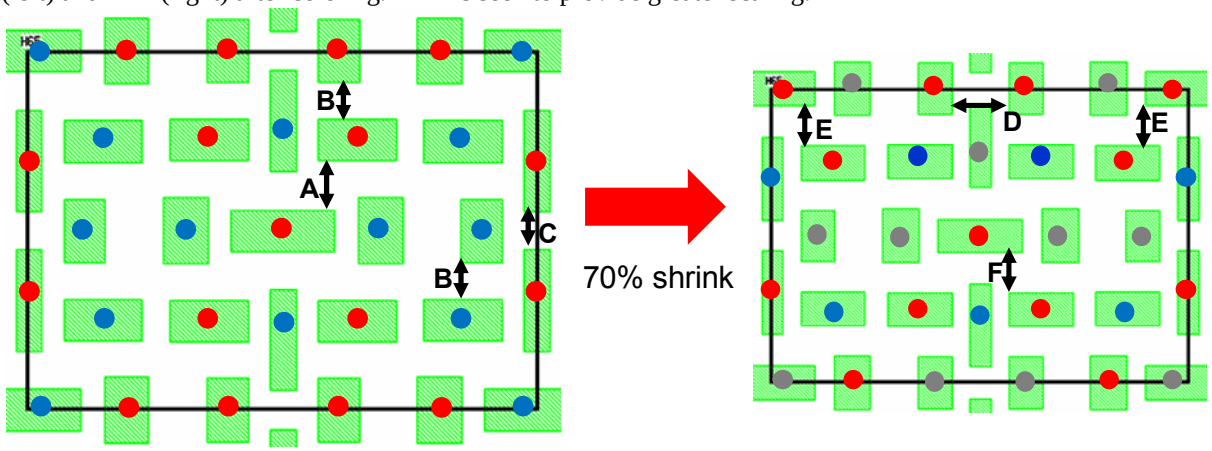


Splitting pitch ≥ (1+√5)/2 ~ 1.618 design pitch
- this is 5 odd-cycles aligned together



Splitting pitch ≥ √3 ~ 1.732 design pitch
- this is 3 odd-cycles aligned together

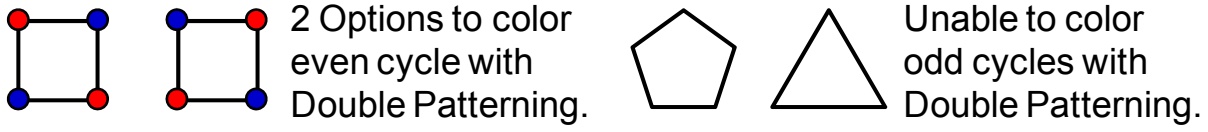
Figure 9. Example showing which spacings between features limit scaling of an SRAM metal1 layer for DPT (left) and TPT (right) after coloring. TPT is seen to provide greater scaling.



DPT/SADP
Limited by key spaces:
- A, B and C.
Limited vertically

TPT
Limited by key spaces
- D, E and F
Vertically and horizontally

Figure 10. Graphical representation of the greatly increased number of coloring options between DPT and TPT. For example, the square with 4 nodes has only 2 coloring options with DPT but has 18 options with TPT [8].



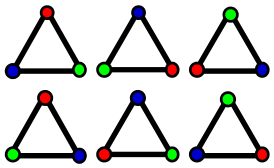
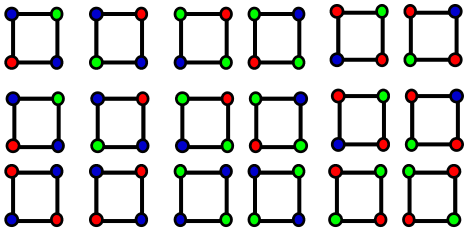
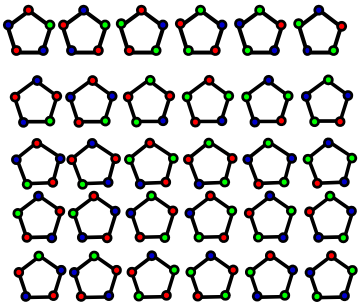
6 options to color 3-way odd cycles with Triple Patterning.	18 options to color 4-way even cycles with Triple Patterning.	30 options to color 5-way odd cycle with Triple Patterning.
		

Figure 11. List of different TPT algorithms investigated for the ability to meet mask synthesis requirements.

- **Poor Man's TPT (=DPT + errors found)**
  - •Run DPT on a layout. Collect all DPT violations & place on 3rd mask.
  - •But lousy color balancing by definition, still need to check 3rd mask is printable
- **Brute Force – try all options**
  - •3 states for N nodes means considering up to 3^N different cases.
  - •For N = 30, this would require 2E14 cases to be considered.
- **Satisfiability Solver (SAT)**
  - •Checks compliance, returns Y/N. If compliant also returns a suitable coloring.
- **Weighted Constraint Satisfaction Problem Solver (WCSP)**
  - •Checks compliance, if not compliant still returns a coloring result which best meets constraints. In addition each constraint can be given a different weight.
- **Integer linear programming (ILP)**
  - •Linear cost function & constraints, integer solutions
  - •Vector-programming formulation
- **Semi-Definite Programming (SDP)**
  - •Approximation to ILP, can be extended to color balancing

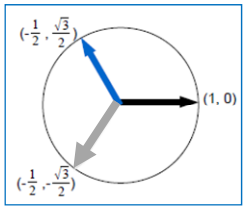
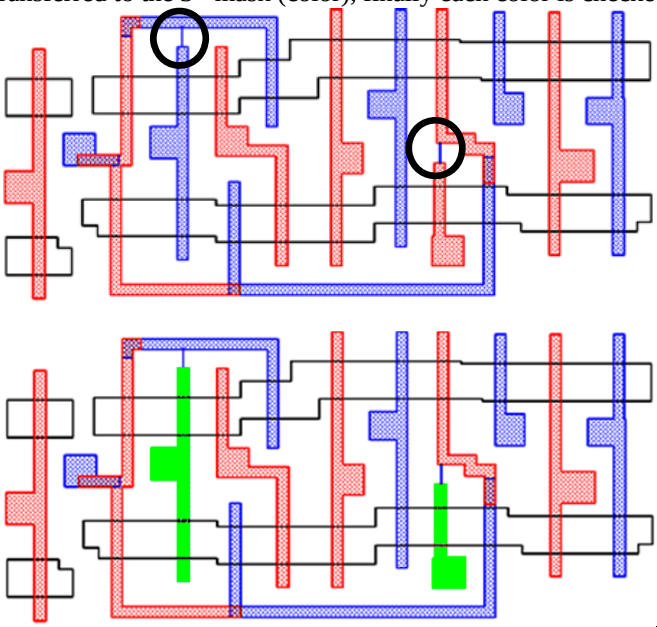


Figure 12. Example showing how the "poor man's DPT" method works to define 3 mask coloring. A traditional 2 color DPT decomposition is 1st run, next DPT conflicts are identified, then one polygon at each conflict area is transferred to the 3rd mask (color), finally each color is checked separately for conflicts (i.e., spacing violations).



Original layout is decomposed by standard DPT methods
- conflicts noted

Polygons causing DPT conflicts can be placed on 3rd mask.

But no guarantee that 3rd mask is conflict free

Figure 13. Example of a "poor man's TPT" decomposition upon a 20nm DPT compliant routing layout shrunk ~30% to 14nm pitch. This method decomposes quickly to find conflicts which can be resolved by introducing a 3rd mask color. However, color balancing is poor.

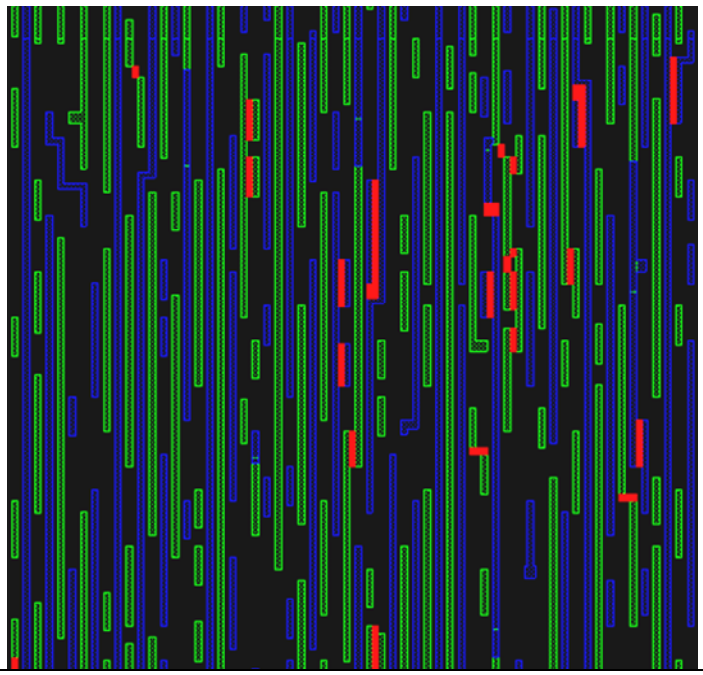
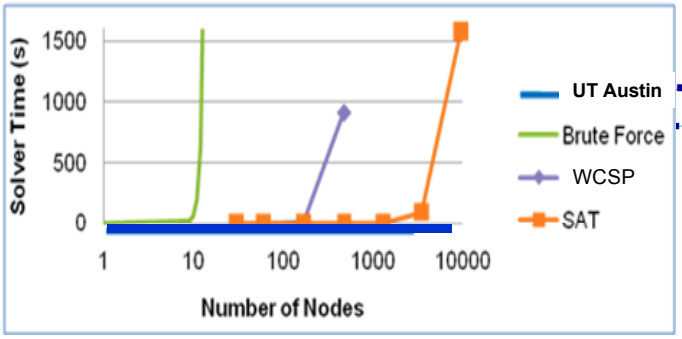
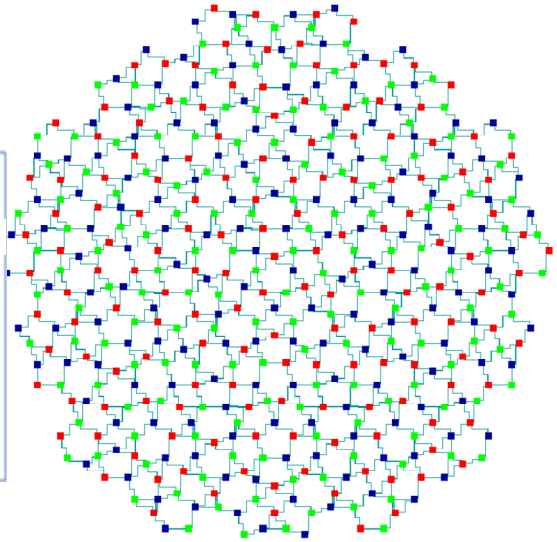


Figure 14. Example showing very large TAT improvement (CPUsec) of SDP method vs. ILT method for TPT decomposition [10]. SDP may occasionally introduce an additional compliance error (cn#) to be fixed however.

Circuit	SE#	CE#	Accelerated ILP			SDP Based		
			st#	cn#	CPU(s)	st#	cn#	CPU(s)
C1	16	247	1	5	5.5	0	6	0.29
C2	38	289	0	15	17.32	0	16	0.77
C3	24	381	0	14	33.41	0	15	0.32
C4	56	437	9	32	203.17	9	32	0.49
avg.	-	-	2.5	16.5	64.9	2.25	17.3	0.468
ratio	-	-	1	1	1	**0.9**	**1.05**	**0.007**

Figure 15. Example of decomposition algorithm TAT vs. the number of nodes to color for known TPT compliant Penrose tiling testpatterns [8]. Also shown is TAT from a Univ. Texas, Austin method which is able to simplify the coloring of this specific testpattern. These methods are promising but may not be universally applicable.





Penrose Rhombic Tiling showing Multiple odd cycle loops. Requires only 3 colors for compliance.