Electromigration-aware Routing for 3D ICs with Stress-aware EM Modeling

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***Abstract*—Electromigration (EM) has become a key reliability concern for nanometer IC designs. For 3D ICs, higher current density/temperature and TSV-induced thermal mechanical stress further exacerbate the EM issue compared to 2D ICs. In this paper, we analyze the root causes of EM for 3D IC signal nets, with consideration of current density, temperature, and TSV-induced thermal mechanical stress. We develop compact EM models for both DC and AC signal nets using detailed finite-element-analysis (FEA) and build EM library for mean-time-to-failure (MTTF). For AC signal nets, we convert AC current into equivalent DC current and model EM with it. One unique property of EM in 3D ICs is that, depending on the current direction, TSV-induced stress may degrade or improve the MTTF, thus routing plays an important role for EM mitigation. We suggest EM-aware routing algorithms for 3D ICs for the first time to our best knowledge, guided by our stress-aware EM modeling. Experimental result shows that our proposed approach improves EM-robustness of 3D IC benchmarks significantly, e.g., 66.4% less EM-violated grids with little sacrifice of conventional routing objectives.**

I. Introduction

One of critical challenges for reliability of nano-scale VLSI is electromigration (EM) [1]. EM refers to the transport of material due to the movement of electrons, and this phenomenon is affected by various factors, such as geometrical shapes, temperature distribution, mechanical stress, current density, and material properties [2], [3]. EM on a wire accumulates more atoms at the end of the wire toward the source pin (anode) and creates hillocks while vacancies appear at the other end of the wire. As a result, circuits with more EM tend to become open or short circuits in a shorter time.

EM causes more reliability issues with 3D IC technology. While 3D IC technology has beneficial features such as realization of small footprint, high bandwidth and suitability to heterogeneous systems, it also brings additional reliability issues such as mechanical stress from coefficient of thermal expansion (CTE) mismatch of TSV and silicon, higher temperature due to the stacked structure, and higher current density to drive multiple dies. These problems in 3D ICs are the factors that can aggravate the EM phenomenon even further.

In traditional 2D ICs, a simple and effective way to reduce EM is decreasing current density. Hence, previous works to enhance EM-robustness focused on routing with optimization of wire width, or current-driven routing to achieve reliability [4]–[7]. Although these works provide reasonable ways to raise EM-robustness in 2D ICs, 3D ICs raise additional issues like mechanical stress and higher temperature on top of higher current density, thus wire width adjustment or current-driven routing are no longer sufficient to guarantee EM-robustness. For 3D ICs, new methodologies are needed to make EM-aware routes, with consideration of TSV-induced mechanical stress and temperature, as well as current density.

In this paper, we model EM with consideration of TSV-induced stress for signal nets, and propose a routing algorithm that increases EM-robustness in 3D ICs. Overall, our contributions are summarized as follows:

- We efficiently analyze EM in 3D ICs with TSV-induced stress consideration, for both AC and DC signal nets
- We effectively predict mean-time-to-failure (MTTF) at a certain location toward any routable direction, with given temperature, current density and TSV-induced stress gradient
- We suggest a net ordering method based on EM-criticality and half-perimeter wire length (HPWL)
- We propose EM-aware maze routing in 3D ICs using expected MTTF, for the first time to our best knowledge
- We develop a technique to balance between EM-awareness and other routing constraints, to prevent over-sacrificing wire length while improving MTTF

II. Motivation

Mechanical stress influences electromigration (EM); applied stress can either retard or accelerate EM depending on the stress gradient and the current direction [8]. We note that significant mechanical stress can be caused by TSVs after annealing process due to different CTE between copper and silicon [9]. Thus, TSV-induced stress can be a driving force for EM, and can affect EM of interconnects in 3D ICs [10]–[13]. We observe unique characteristics of EM in metal wires in 3D ICs from recent works in [12], [13]:

1) TSV-induced stress affects EM near TSV region
2) EM can be either mitigated or aggravated near TSV region depending on routing direction because stress gradient has an impact on EM, and the stress gradient varies with routing direction
3) The lowest metal layer (M1) can be the most dangerous layer on EM due to not only the highest current density and temperature, but also the highest stress gradient among all metal layers

If TSV-induced stress had only negative effect on EM, avoiding TSV region could be the only solution in mitigating EM problem, and it could waste large routing resource. However, as EM-induced lifetime can be varied depending on the routing direction, EM-aware routing can further improve EM-robustness and utilize routing resource more effectively near TSV region. Moreover, since each metal layer has different TSV-induced stress, current density and temperature profiles, a smarter routing scheme can accommodate better reliability across multiple metal layers.

In this work, we propose an EM-aware routing that can effectively choose EM-safe paths for multiple routing layers. To achieve the goal,

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TABLE I
PARAMETER VALUES FOR EM MODELING EQUATION.

Parameter	Representation	Value
Ea	Activation energy	1.3e-19
k	Boltzmann constant	1.38e-23
Z	Effective charge	4
e	Electron charge	1.6e-19
f	Vacancy volume ratio	0.4
Ω	Atomic volume	1.6e-29
D_0	Initial diffusivity	1e-8
ρ	Resistivity of copper[Ωm]	2.2e-8

we model EM in 3D ICs and build *EM library* for quick estimation of EM for a certain layout. After that, we order the nets with EM criticality and wire length. Finally we estimate EM criticality for each routable grid during maze routing, and search the EM-safe path using the cost function. Because most of signal nets are AC nets, we use *equivalent DC current* for AC nets. As a result, our EM routing can deal with both DC and AC signal nets in 3D ICs.

III. STRESS-AWARE EM MODELING FOR 3D ICS

A. Modeling of Electromigration with Stress Consideration

Electromigration (EM) can be defined as the mass transport of atoms due to various driving forces such as high current density, mechanical stress gradient, and temperature gradient [2], [3]. EM can be expressed by the mass balance equations of vacancy concentration [14], [15],

$$\nabla \cdot \vec{q} + \frac{\partial c}{\partial t} = 0 \tag{1}$$

where

$$\vec{q} = \frac{Dc}{kT} Ze\rho\vec{j} + \frac{Dc}{kT} Q\frac{\nabla T}{T} - \frac{Dc}{kT} f\Omega\nabla\sigma - D\nabla c, \tag{2}$$

$$D = D_0 \cdot exp\left(\frac{\Omega\sigma - Ea}{kT}\right). \tag{3}$$

Here, $\vec{q}$ is total vacancy flux, c is vacancy concentration, $\vec{j}$ is current density vector, T is temperature, σ is hydrostatic stress, and D is diffusivity with initial diffusivity D_0. Table 1 shows parameter values that we use. With TSV-induced stress, Black's equation [16] is no longer valid to predict MTTF, and we need to solve Eqn. (1)-(3) using a finite-element-analysis (FEA) simulator to estimate the MTTF [2], which can be very time consuming. For fast MTTF estimation of interconnects during routing, we use EM library introduced by [13]. EM library is a look-up table to get MTTF from inputs such as current density, temperature and stress gradient. We build EM library by solving Eqn. (1)-(3) for a simple wire using FEA simulator. Because we exhaustively simulate MTTF with possible combinations of current density, temperature and stress gradient for EM library, fast estimation of MTTF can be made during routing stage. Meanwhile, we use linear interpolation for intermediate values to keep reasonable data size of library and avoid computational overhead.

B. Stress Gradient Map Generation

Near the TSV region, mechanical stress is generated from the coefficient of thermal expansion (CTE) mismatch of silicon and copper [9]. To estimate stress level of a certain point with given TSV locations, we use FEA simulation result for a single TSV and a superposition method to consider multiple TSV effects [17]. We assume planar stress model as introduced in [9]. Fig. 1 shows a stress map of one of our benchmarks. From Eqn. (2), EM is a function of stress gradient $\nabla\sigma$, which is the rate of increase of stress. Because we can reasonably assume that a wire is a one-dimensional structure, direction of current in a routed wire is a decisive factor to select stress gradient vector. For example, if a wire is positioned along

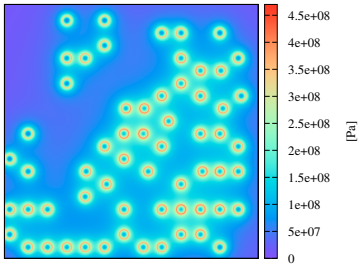
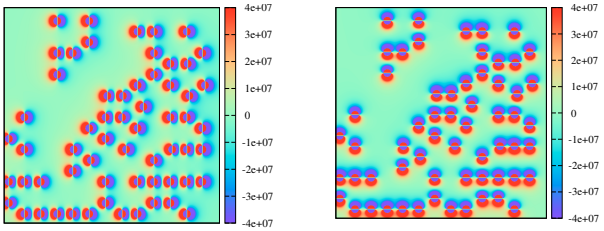


Fig. 1. Stress map of one of the benchmark circuits. A circular shape represents a TSV.



(a) (b)

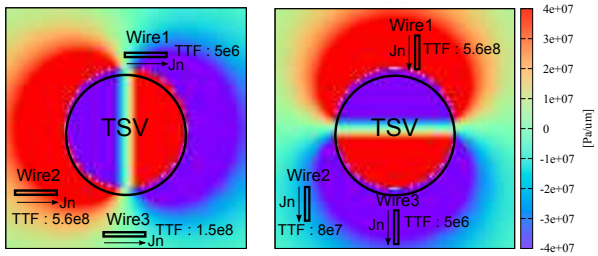
Fig. 2. Stress gradient map of a benchmark circuit for each direction; (a) $+x$ direction, (b) $+y$ direction. $-x$ and $-y$ directional stress gradient maps are symmetric with these two, having same magnitude but opposite polarity.

the $+x$ direction and current flows in $+x$ direction, stress gradient is interpreted as $\nabla\sigma = \frac{\partial\sigma}{\partial x}\hat{x}$. As we need to search every routable direction, we generate a stress gradient map for each direction from the stress map, as shown in Fig. 2. To handle multiple routing layers, we generate stress and stress gradient map for each layer. The further from the device layer, the lower stress level we get.

C. Directional Property of EM in 3D ICs

Directional property is a unique characteristic of EM in 3D IC, that MTTF can vary depending on the routing direction, i.e., current flowing direction. EM in a short interconnect segment can induce *back stress* [18], [19]. Once migrating atoms generate accumulation on anode and vacancy on the cathode, compressive stress and tensile stress are induced on the anode and cathode, respectively. Thus, positive stress gradient w.r.t. current direction appears on the wire segment and it *compensates* the EM, which is called back stress [18], [19]. Recent study [8] shows that additional stress on top of back stress can be analyzed similarly; positive stress gradient can retard EM, while negative stress gradient can accelerate EM. Here, stress gradient vector is based on the current direction from anode to cathode. Works in [12], [13] consider TSV-induced stress as additional stress from [8]; positive stress gradient from TSV can mitigate EM, while negative stress gradient can aggravate EM. As we show in Fig. 2, stress gradient value can be different depending on a routing direction, or more specifically, current flowing direction. Hence, MTTF can be changed with current direction in 3D ICs, which is called *directional property* in this paper.

Fig. 3 shows how wires near a TSV can have different MTTF according to the routing direction. We assume current density values of three wires are the same as $1e9[A/m^2]$ and temperature is fixed as $353^\circ K$ ($80^\circ C$). In (a), current flows in $+x$ direction for three wires, therefore stress gradient for $+x$ needs to be used for EM analysis. For wire1, negative stress gradient is applied and it aggravates EM, meanwhile wire2 has much longer MTTF due to the positive stress gradient w.r.t. current direction. Wire3 has almost zero stress gradient, and its MTTF is longer than wire1 but shorter than wire2. In Fig. 3 (b), wires are routed differently and the current on the wires flow in $-y$ direction. Now wire1 and wire3



(a) (b)

Fig. 3. Example to show *Directional Property of EM* in 3D IC; (a) Stress gradient in $+x$ and wires with current flowing in $+x$ direction, (b) Stress gradient in $-y$ and wires with current flowing in $-y$ direction.

have large positive and negative stress gradient, respectively, while wire2 has small amount of negative stress gradient. Here MTTF of three wires are $MTTF_{wire1} > MTTF_{wire2} > MTTF_{wire3}$. In short, negative stress gradient makes shorter MTTF if current density and temperature are unchanged. Because the effective stress gradient varies depending on the current flowing direction, MTTF also varies depending on the current direction. In general, normal current access *toward* a TSV is helpful to EM-robustness due to positive stress gradient; normal access *from* a TSV has opposite trend. Tangential access besides a TSV can either have shorter or longer MTTF depending on the position.

D. Modeling Equivalent DC Current for AC Nets

Most of the signal nets in VLSI are AC nets with bi-directional current. In the past, AC nets were considered as invulnerable nets to EM, because opposite direction of current can compensate EM to some degree. However, if current imbalance exists between two direction of current, EM cannot be entirely canceled out [20], [21]. Moreover, unlike power/ground nets, every segment of signal routing is critical to failure; even if a small part of the interconnect fails, the entire signal net fails. Hence in deep sub-micron technologies, designers have taken account of AC nets for EM-awareness [1], [22]. In 3D ICs, AC nets can be more vulnerable due to TSV stress-driven migrating factor [13].

To analyze EM for AC nets, we convert AC current waveform into *equivalent DC current*, similar to work in [21], [23]–[25]. As we are interested in the effect of TSV stress on EM, we consider average current, instead of root-mean-square (RMS) current for Joule heating. However RMS current can be analyzed similarly.

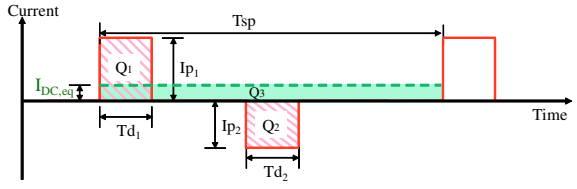


Fig. 4. AC and its equivalent DC waveforms using charge model. Red solid line and green dotted line represent AC and equivalent DC current waveforms, respectively.

We model AC current waveform as a series of rectangular pulses as shown in Fig. 4. In the figure, Td_1 and Td_2 stand for current pulse duration of positive and negative direction, respectively. Ip_1 and Ip_2 are peak current for positive and negative direction, Tsp is average switching period, $I_{DC,eq}$ is equivalent DC current value. We extend average current recovery (ACR) model [25] into charge form. Then, positive charge Q_1, negative charge Q_2 and charge for equivalent DC Q_3 for a single cycle can be expressed as,

$$\begin{aligned} Q_1 &= Td_1 \times |Ip_1| \\ Q_2 &= Td_2 \times |Ip_2| \\ Q_3 &= Tsp \times |I_{DC,eq}| = \begin{cases} Q_1 - c_h Q_2 & \text{if } Q_1 \geq Q_2 \\ Q_2 - c_h Q_1 & \text{otherwise.} \end{cases} \end{aligned} \tag{4}$$

Here c_h is the empirical healing coefficient of EM for opposite direction of current. If $c_h = 1$ and $Q_1 = Q_2$, positive and negative charge can be perfectly cancelled out and equivalent DC current becomes zero. Because migrated atoms cannot perfectly fill the vacancy, c_h is slightly less than 1 in general [25]. To get the c_h value, we use FEA-based EM modeling using COMSOL Multiphysics. First, we measure MTTF by sweeping DC current value, and then measure MTTF with sample AC current waveforms. If MTTF of AC is the same as that of certain DC, we can reasonably assume it as *equivalent DC* for EM. With the AC current waveform and equivalent DC value from FEA simulation, we get Q_1, Q_2 and Q_3 values, and we get $c_h = 0.95$ on average using Eqn. (4).

Next, we check the accuracy of charge model in Eqn. (4). We generate 40 test AC waveforms with random Td_1, Td_2, Ip_1 and Ip_2. While we directly simulate MTTF with FEA simulator and get equivalent DC by comparing MTTF value, we also calculate equivalent DC using Eqn. (4) with $c_h = 0.95$. Equivalent DC from two methods are shown in Fig. 5. Average error rate between two methods is 1.4% for 40 test cases. As charge model is reasonably accurate, we convert AC current into equivalent DC current using charge model in Eqn. (4) with $c_h = 0.95$ in our work.

To get the current profile of benchmark circuits, we use Synopsys NanoSim. For AC nets, we get Ip_1, Ip_2, Td_1, Td_2 from NanoSim and convert it into equivalent DC current with charge model. This equivalent DC can be used as a input for EM library to estimate MTTF. For DC nets, we use current value directly. As a result, we can evaluate EM reliability for both AC and DC nets using *EM library*.

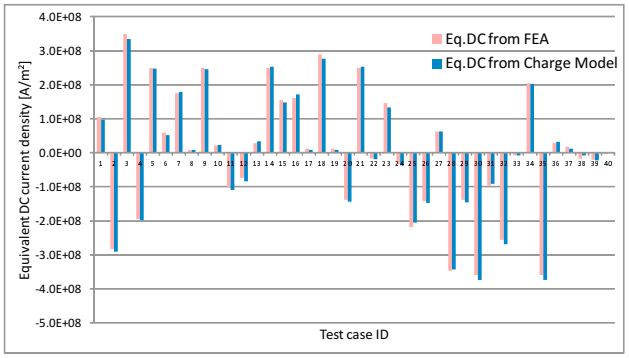


Fig. 5. Comparison of equivalent DC between FEA simulation and charge model for 40 test cases. Wire dimension of M1 in 45nm technology is used to get *current density*.

E. Thermal Consideration

Temperature affects EM by changing diffusivity D in Eqn. (3) and through temperature gradient in Eqn. (2). Actual temperature in a circuit can fluctuate according to time, with the input vector patterns and switching activity. Although EM analysis with time-varying temperature has been shown in work [26], it would make EM analysis too complex to do during routing. Hence, we limit our scope to static EM and assume reasonable static thermal distribution. Fig. 6 shows the thermal map we used for our experiments. The average temperature in this map is $353°K$ $(80°C)$, and standard deviation is 23. During EM evaluation of each grid during routing, we ignore the effect of temperature gradient in Eqn. (2) because temperature

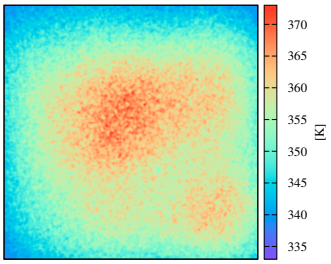


Fig. 6. Thermal map used in our experiments.

difference between adjacent grids is negligible. Still we consider the static temperature effect of diffusivity term in Eqn. (3) and Eqn. (2). In general, high temperature of interconnects makes short MTTF because of higher diffusivity D, if all the other conditions are same. For routing across multiple metal layers, we generate temperature map for each layer. We assume temperature in the lowest metal (M1) is the highest among routing layers, and is decreased by $2^{\circ}C$ per routing layer.

IV. EM-aware Routing for 3D ICs

As we discussed in Section III-B and Section III-C, EM-robustness can depend on the relative orientation of TSVs and wires, and it makes EM-aware routing problem in 3D ICs to be unique. Fig. 7 illustrates an example of EM-aware routing of 3D ICs. For this

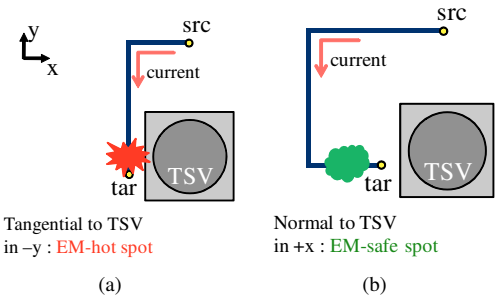


Fig. 7. Example of a EM-aware routing based on stress gradient; (a) a routing without EM-awareness, (b) a routing with EM-awareness.

example, let us consider a simple case where temperature and current do not vary on a routed path, and MTTF is a function of stress gradient only. Considering Fig. 3 in Section III-C, normal directional current access *toward* a TSV is helpful to enhance MTTF at the point near the TSV because of increasing stress gradient, while tangential directional access near the TSV can degrade MTTF due to decreasing stress gradient. Thus around the target pin location in Fig. 7, (b) can be more robust to EM than (a). Note that (b) has more wire length to detour the EM-hot spot instead. From this example, we can see that a new routing methodology is needed to achieve EM-awareness for 3D ICs, with considering directional property of EM. In our work, we calculate MTTF for every direction during EM-aware maze routing, with stress gradient toward each routable direction at a certain point. By doing this, we consider the effects of directional property of EM, as a form of *stress gradient* of each routable direction. Also, we consider the effect of current density and temperature on EM. In the following sections, we will present the overall flow of EM-aware routing, and then explain MTTF prediction during routing, net ordering and maze routing algorithms in detail.

A. Overall Flow

Fig. 8 shows the overall flow of our EM-aware routing for 3D ICs. Initially, we need TSV placement information to calculate TSV-induced stress profile, as described in Section III-B, as well as thermal profile of a circuit and current density of each net. To analyze EM of AC nets we use equivalent DC current density as explained in Section III-D. Since our routing considers one net at a time, net ordering for routing can affect the final routing result. We order nets based on the expected MTTF of pre-routed nets and half-perimeter wire length (HPWL), presented in Section IV-C. And then during EM-aware maze routing, we predict MTTF for each routable direction at the grid subject to search with EM library, as depicted in Section IV-B. Once MTTF is predicted for every direction of the grid, EM cost is calculated during maze routing to find EM-safe paths, as explained in Section IV-D. Finally, EM-aware maze routing can be made based on the cost function. If a net is failed to be routed, rip-up and reroute technique is used.

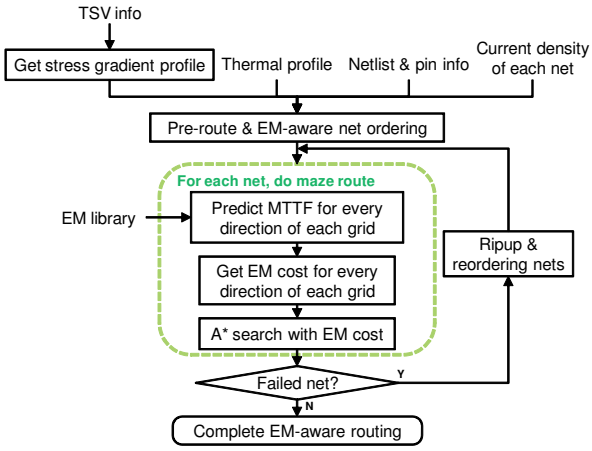


Fig. 8. Overall flow of EM-aware routing for 3D ICs

B. MTTF Prediction with EM Library

To predict MTTF of a grid effectively, we use EM library that uses pre-simulated MTTF with varying stress gradient, current density and temperature as introduced in [13]. This EM library can work as a look-up table that helps retrieving the expected MTTF of a certain grid toward certain direction during routing, which enables us immediate prediction of MTTF.

As we explain in Section III-B, III-D and III-E, we already have stress gradient for each direction in xy-plane, $\{+x, -x, +y, -y\}$, as well as temperature and current information. Therefore, we can easily predict MTTF for these four directions with EM library. To transit to upper or lower metal layer, $+z$ or $-z$ direction, we consider various factors; depending on the metal layer, current density varies due to the different wire thickness and width, temperature and TSV-induced stress also change because the distance from the device layer is different. Current densities in different metal layers are calculated based on 45nm technology rule by assuming minimum wire dimension. Stress profile of each metal layer is generated using damping ratio from FEA simulation result using ANSYS. We assume temperature decreases by $2^{\circ}C$ per a metal layer, as distance from the device layer increases. Using stress profile, current density and temperature for each metal layer, we get the *expected MTTF* for both $+z$ and $-z$ direction, similar to other directions in the xy-plane. As a result, we get six MTTF values around the grid, toward $\{+x, -x, +y, -y, +z, -z\}$ direction. In general, upper metal layers tend to be more robust to EM due to the smaller level of TSV-induced stress, lower temperature and lower current density than M1 metal layer. Algorithm 1 describes our suggested method to predict MTTF on grid g for all the routable directions. During maze routing, we calculate EM cost based on MTTF for each routable direction.

Algorithm 1 PredictMTTF(x_g, y_g, z_g, J_n)

Require: EM library
for each metal layer $L \in \{z_g - 1, z_g, z_g + 1\}$ **do**
  T_L=GetTemperature(x_g, y_g, L) //for grid g in layer L
  $J_{n,L}$=GetCurDen(n, L) //for net n in layer L
  for each direction $i \in$ 4DIR=$\{xinc, yinc, xdec, ydec\}$ **do**
    $\nabla\sigma_L(i)$=GetStressGrad(x_g, y_g, L, i)
    MTTF$_L(i)$=GetMTTF($J_{n,L}, T_L, \nabla\sigma_L(i)$)
    if $L == z_g$ **then**
      MTTF(x_g, y_g, z_g, i)=MTTF$_L(i)$ //set MTTF of $\pm$x,$\pm$y
    end if
  end for
end for
MTTF($x_g, y_g, z_g, zinc$)=$\frac{1}{4} \cdot \sum_{\forall i \in 4DIR}$MTTF($x_g, y_g, z_g + 1, i$)
MTTF($x_g, y_g, z_g, zdec$)=$\frac{1}{4} \cdot \sum_{\forall i \in 4DIR}$MTTF($x_g, y_g, z_g - 1, i$)

TABLE II
EXAMPLE OF EM-AWARE NET ORDERING.

Net id	Pre-route result			Routing order
	HPWL	Grade	MTTF$_{net}$	
net1	49	1	2.2e8	2
net2	72	1	4.2e8	3
net3	87	1	7.6e7	1
net4	113	2	8.3e7	6
net5	148	2	5.3e6	4
net6	185	2	9.4e6	5

C. EM-aware Net Ordering for Routing

Our routing makes routing of nets sequentially, thus net ordering can affect the final result. To achieve two competing goals during net ordering, which are minimization of wire length and improvement of EM-robustness, we use heuristic *grade-based EM criticality consideration* method. In our approach, wire length is the first criteria for net ordering, and for wires with similar length, we consider the EM-criticality for the net ordering. To be more specific, we firstly sort nets with half-perimeter wire length (HPWL), in an increasing order as in [27] to prevent unnecessary detour of short nets. Then, we group nets with HPWL and make nets in the same group have similar HPWL. Once grouping finishes, the *first-grade group* has the smallest HPWL on average, and the last-grade group has the largest HPWL. Then we perform pre-routing to approximate MTTF of a route of each net. Pre-routing is maze routing with A* search without EM-awareness, and we measure MTTF of pre-routed paths to identify EM-critical nets using a method in Section IV-B. After pre-route, from the first-grade group, the most EM-critical net with the shortest expected MTTF is routed first within a group. If a net has a short MTTF, it means that the net will have high probability of EM-induced failure if we do not make an EM-aware routing. Therefore we put high priority in routing to the EM-critical nets among all the other nets within the same group. The rationale of *grade-based EM criticality consideration* is to limit the EM-criticality based net sorting within the group with similar wire length only, so that we can still take advantages of *shorter net first* method in overall.

Table II illustrates an example of our EM-aware net ordering. Let us assume that we have two-level grade for HPWL in this example. Here, net1 through net3 are in the first-grade group, so they needs to be routed earlier than the nets in the second-grade group. Among three nets in the first-grade, because net3 has the shortest MTTF, our routing makes a route of net3 first, and then net1 and net2 are routed sequentially. After that routing for second-grade group is started, and net5, net6, net4 are routed sequentially based on their MTTF. If there is any case that the routing needs to do rip-up and reroute, we re-order the nets to put the failed net to the first priority.

D. Cost Function for EM-aware Maze Routing

EM cost is the key factor for EM-awareness during maze routing. We define EM cost at a grid g toward direction i as a ratio of threshold MTTF ($MTTF_{ref}$) and $MTTF(g, i)$ as Eqn. (5) [28]. Intuitively, for the EM-critical grid who has shorter MTTF in a certain direction, EM cost gets bigger toward that direction.

$$r(g, i) = \frac{MTTF_{ref}}{MTTF(g, i)} \tag{5}$$

Next, we need to make a reliable cost function that can handle both EM-awareness as well as traditional routing constraints. We use *negotiation-based A* search* for this problem.

Negotiation-based A* search is an idea to have robustness in routing by balancing the historical cost and currently congested cost, i.e., present cost [28], [29]. We adopt this method to our detailed maze routing. Instead of using historical cost h and present cost p for each iteration of an edge in a global router [29], we calculate and update h and p for each grid. In Eqn. (6), for a grid g toward direction i, $h(g)$, $p(g, i)$, $dist(g, tar)$ are historical cost, present cost, and distance between g and target pin, respectively. As a path is constructed, $h(g)$ becomes bigger based on Eqn. (8), thus choosing high present cost can be cheaper than choosing high historical cost. It means history of a path - whether it passed EM hot spots or not - can affect to the construction of a path at a present grid. We note that the expected cost from current grid to target, $dist(g, tar)$, affects to the routing cost as well. Balancing between historical, present and expected cost is made by α and δ.

$$cost(g, i) = h(g) + \alpha \cdot p(g, i) + \delta \cdot dist(g, tar) \tag{6}$$

$$p(g, i) = dist(src, g) \cdot \left(1 + \frac{r(g, i)}{\beta}\right) \tag{7}$$

$$h(g) = \sum_{\forall (g,i) \in RP(g)} p(g, i) \tag{8}$$

Adding EM cost effect to the present cost in Eqn. (7) is the key part of cost function of EM-aware detailed maze routing. As we explained in Eqn. (5), $r(g, i)$ is EM reliability cost to show the ratio of current MTTF and the reference MTTF. In Eqn. (7), $dist(src, g)$ is distance between a source and current grid g, and β is a parameter to balance between distance-based routing cost and EM cost. As β increases, impact of EM cost on a total routing cost decreases.

Decision of α and δ is important to balance between historical, present and expected cost. Inspired by the work in [29], we pick α as a ratio between maximum historical cost and maximum present cost that a wire can have. From Eqn. (7) and Eqn. (8), upper bound of maximum historical cost of a path is expressed as Eqn. (9),

$$h_{max} = \sum_{\forall g \in RP} p_{max} \tag{9a}$$

$$= \sum_{\forall g \in RP} \left\lceil dist(src, g) \cdot \left(1 + \frac{r_{max}}{\beta}\right) \right\rceil \tag{9b}$$

$$= K \cdot \sum_{\forall g \in RP} \lceil dist(src, g) \rceil \tag{9c}$$

$$= K \cdot \left\{ \frac{dist(src, tar) \cdot \{dist(src, tar) + 1\}}{2} \right\} \tag{9d}$$

where

$$K = 1 + \frac{r_{max}}{\beta}. \tag{9e}$$

Similarly, upper bound of maximum present cost of a path can be shown as Eqn. (10).

$$p_{max} = \left\lceil dist(src, g) \cdot \left(1 + \frac{r_{max}}{\beta}\right) \right\rceil = K \cdot dist(src, tar) \quad (10)$$

With Eqn. (9) and Eqn. (10), we pick α as Eqn. (11). It guarantees balancing between the worst historical cost and the worst present cost. Since α is a function of distance between a source and a target, it should be calculated for each wire. We use HPWL for $dist(src, tar)$ of each net.

$$\alpha = \frac{h_{max}}{p_{max}} = \frac{dist(src, tar) + 1}{2} \quad (11)$$

For δ in Eqn. (6), we use dynamic adjustment according to the wire length. While finding EM-safe routes, we also want to have reasonably short wire length. To prevent *over-avoiding* EM-hot spots which spends an extremely long wire length, we give penalty to a longer wire than pre-routed wire length, L_{ref}. We note that pre-routing is done without EM-awareness, thus it can give a good reference for the wire length of each net. During routing with EM-awareness, once the wire length grows longer than the L_{ref}, we increases δ exponentially. In this way, as the wire length becomes longer than the L_{ref}, weight of expected cost becomes larger, and driving force toward to the target pin becomes bigger. Eqn. (12) shows dynamic adjustment of δ according to the current wire length, L_{cur}. To have same impact of present cost and expected cost to the total routing cost, we pick δ_o as same as α in this work.

$$\delta(L_{cur}) = \begin{cases} \delta_o & \text{if } L_{cur} \leq L_{ref} \\ \delta_o \cdot \eta^{\frac{L_{cur} - L_{ref}}{L_{ref}}} & \text{if } L_{cur} > L_{ref} \end{cases} \quad (12)$$

E. Routing Algorithm

Algorithm 2 describes our method to route a net with EM-awareness, which is briefly presented in a green dotted box of Fig. 8. For a grid subject to search during maze routing, we predict MTTF for each direction as depicted in Section IV-B, and calculate EM cost and total cost as explained in Section IV-D. Using total cost, A*-based maze routing is made.

Algorithm 2 EM-aware maze routing of a net

Require: current density of a net J_n, source pin src, target pin tar, EM library, thermal and stress gradient profile

```
Start from src, do A* search of neighbor grids
for each grid subject to search g = (x_g, y_g, z_g) do
    PredictMTTF(x_g, y_g, z_g, J_n) //Section IV-B
    for each direction i ∈{xinc, yinc, zinc, xdec, ydec, zdec} do
        r(g, i)=CalculateEMCost(MTTF(g, i)) //Eqn. (5)
        cost(g, i)=CalculateTotalCost //Section IV-D
    end for
end for
Continue maze routing until arriving to tar
```

V. Experimental Results

We implemented our proposed algorithm with C++, and performed experiments on 2.93GHz Intel Quad Core Linux Machine. Benchmark circuits described in Table III are the ones by [30]. In Table III, first three rows are three stacked dies in the same circuit *uP*, one of the industrial microprocessors. Next three rows in the table show another industrial circuit *IDCT*, which performs inverse discrete cosine transformation. We use part of the circuits instead of the whole circuits. Originally each system had four stacked dies after 3D placement from work [30], but we did not use the bottommost dies because they do not include any TSVs which can differentiate EM in 3D and 2D ICs. TSV cell size is $4um \times 4um$ for all cases. We use 20 grades for *grade-based EM criticality consideration* approach for net ordering.

TABLE III
Benchmark circuits.

	Size[um^2]	#Metal	#Nets	#Pins	#TSVs
uP Die0	10000	6 layers	803	1831	33
uP Die1	10000	6 layers	882	2125	42
uP Die2	10000	6 layers	627	1545	50
IDCT Die0	10000	6 layers	579	1383	39
IDCT Die1	10000	6 layers	814	2152	61
IDCT Die2	10000	6 layers	663	1694	58

To get current waveform and its equivalent DC, we use gate-level information of benchmarks. For generating stress data from the TSV, we use placement information of benchmarks generated by [30]. We regard *EM-violation* as the interconnect failure earlier than $MTTF_{ref}$, which is $1e8$ seconds (9.5 years) in this paper. Here we define *failure* as 5% deviation of atomic concentration [3], [12], and define *EM-violated wire* as a wire which has at least a single *EM-violated grid*. We assume a routing grid is same as a grain structure of the wire, thus each grid can be the unit of EM analysis. We use η as 25 for Eqn. (12) in our experiments.

We can change the weight of EM cost by tuning β, as we discussed in Eqn. (7). With increased β, the weight of EM cost in the entire cost decreases, and routing becomes *less EM-aware*. In Table IV, we show trade-off between EM-awareness and routing resources with different β values, for *uP Die1*. As we change β from 100 to 10000, percentage of EM-improvement gets smaller, but we have smaller wire length and via overhead instead. In case of β being 100, wire length overhead and via overhead are larger than the other cases because our algorithm tries to choose EM-safe paths more aggressively. By tuning β, we can balance between MTTF and routing overheads, and can achieve improved EM-robustness within certain routing constraints. For the rest of experimental results, we use β as 1000.

Table V shows experimental results of our EM-aware routing, with comparison of wire length (WL)-driven routing. First, we investigate number of EM-violated wires at a threshold time, in the first column of the Table V. Definition of *EM-violated wire* is a wire which has at least an EM-violated grid. All the benchmark circuits show decreased number of EM-violated wires at the $MTTF_{ref}$, -36.3% on average with our EM-aware routing. Fig. 9 shows cumulative distribution function (CDF) of EM-violated wires according to time for one of our benchmarks, *uP Die1*. In this graph, y-axis represents number of EM-violated wires at a certain time divided by the total number of wires, and x-axis is time in second. We can see that MTTF is significantly improved with our EM-aware routing, compared to wire length-driven one. Fig. 10 shows zoom-in shot of Fig. 9, to examine lower MTTF region.

Next, we study number of *EM-violated grids* along routed paths at $MTTF_{ref}$ as shown in the second column in Table V. The number of EM-violated grids decreases substantially with our EM-aware routing, -66.4% on average. The effect of constructing EM-safe paths and increasing MTTF of each grid in the routed path is displayed more clearly at the CDF graph for *uP Die1* in Fig. 11. Red line represents baseline results of cumulative number of EM-violated grids normalized by total number of routed grids, and a blue line represents that of EM-aware routing. We can see that normalized number of EM-violated grids is much lower with our EM-aware routing. We note that by calibrating $MTTF_{ref}$ at the cost function

[1]One local via is counted as three grids. Wire length unit is [0.1um].

TABLE IV

TRADE-OFF BETWEEN EM-AWARENESS AND WIRE LENGTH, LOCAL VIA IN *uP Die1*. WL-DRIVEN, EMAR, % REPRESENT WIRE LENGTH-DRIVEN ROUTING (BASELINE), EM-AWARE ROUTING, AND DIFFERENCE DIVIDED BY THE BASELINE IN PERCENTAGE, RESPECTIVELY.

	#EM-violated wires			#EM-violated grids			Wire length[1]			#Local via		
	WL-driven	EMAR	%	WL-driven	EMAR	%	WL-driven	EMAR	%	WL-driven	EMAR	%
$\beta = 100$	176	59	-66.5%	3729	243	-93.5%	68689	69490	1.17%	1063	1276	20.0%
$\beta = 1000$	176	89	-49.4%	3729	1040	-72.1%	68689	68996	0.45%	1063	1146	7.81%
$\beta = 10000$	176	96	-45.5%	3729	1503	-59.7%	68689	68856	0.24%	1063	1108	4.23%

TABLE V

EXPERIMENTAL RESULTS OF EM-AWARE ROUTING COMPARING WITH WIRE LENGTH-DRIVEN ROUTING. WL-DRIVEN, EMAR, % REPRESENT WIRE LENGTH-DRIVEN ROUTING (BASELINE), EM-AWARE ROUTING, AND DIFFERENCE DIVIDED BY THE BASELINE IN PERCENTAGE, RESPECTIVELY.

	#EM-violated wires			#EM-violated grids			Wire length[1]			#Local via			Run time[s]	
	WL-driven	EMAR	%	WL-driven	EMAR	%	WL-driven	EMAR	%	WL-driven	EMAR	%	WL-driven	EMAR
uP Die0	55	37	-32.7%	1167	486	-58.4%	39602	39647	0.11%	614	642	4.56%	484	525
uP Die1	176	89	-49.4%	3729	1040	-72.1%	68689	68996	0.45%	1063	1146	7.81%	1909	1888
uP Die2	146	112	-23.3%	3135	1424	-54.6%	43613	43740	0.29%	736	770	4.62%	1209	855
IDCT Die0	91	62	-31.9%	2452	943	-61.5%	39182	39260	0.20%	477	474	-0.63%	863	1014
IDCT Die1	184	114	-38.0%	4780	1220	-74.5%	79521	79793	0.34%	1216	1285	5.67%	2645	2725
IDCT Die2	183	118	-35.5%	4469	1523	-65.9%	65225	65382	0.24%	970	1014	4.54%	1898	2042
Total	835	532	-36.3%	19732	6636	-66.4%	335832	336818	0.29%	5076	5331	5.02%	9007	9049

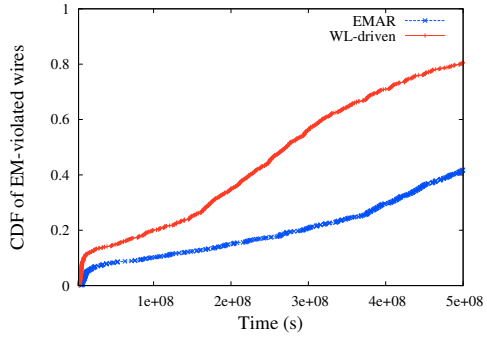


Fig. 9. CDF of EM-violated wires according to the time in *uP Die1*. Our EM-aware routing has significantly less number of EM-violated wires than wire length-driven one.

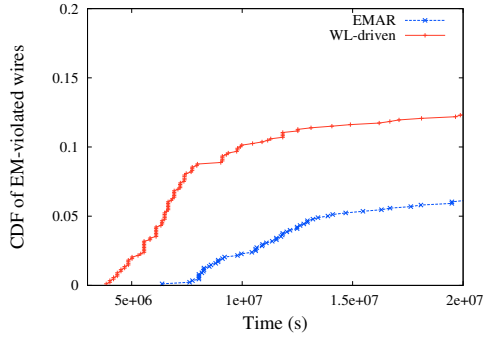


Fig. 10. Zoom-in shot of Fig. 9. Our EM-aware routing has much less number of EM-violated wires than wire length-driven one.

in Section IV-D, we can adjust the threshold MTTF that we are interested in. The third and the fourth column in Table V show wire length and number of local vias of routed paths, respectively. For wire length, we count one local via as three grid units. There are overheads of wire length, 0.29% on average, and number of local vias, 5.02% on average, still these overheads are reasonably acceptable.

TSV-induced stress level decreases as the distance from TSV increases. Thus simply having larger routing keep out zone (KOZ) from TSVs can be helpful for EM-robustness [13]. However as we observe in Section III-C, TSV-induced stress is not always something to avoid; it can either mitigate or aggravate EM depending on the stress gradient. Hence our routing does not just avoid near TSV

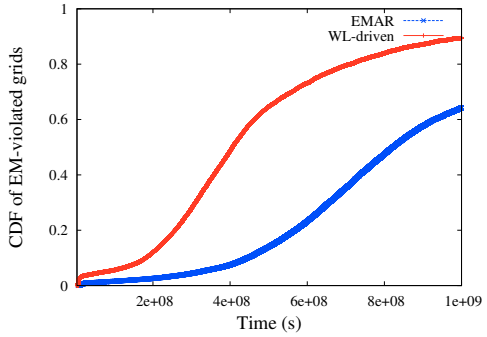


Fig. 11. CDF of EM-violated grids according to the time in *uP Die1*. Normalized EM-violated grids is substantially less with proposed EM-aware routing.

region, rather it chooses more EM-safe routes than the one without TSV. Thus, we actively take advantage of *directional property* of EM in 3D ICs and improve MTTF even further around TSV region. We compare our EM-aware routing result and WL-driven one with larger KOZ sizes in Table VI. Comparing with WL-driven routing with $0.1um$ KOZ, $1um$ and $0.7um$ KOZ show only slightly less number of EM-violated wires. On the other hand, our EM-aware routing reduces it significantly even with $0.1um$ KOZ. In terms of EM-violated grids, $1um$ and $0.7um$ KOZ cases help to have less number of EM-violated grids than the one with $0.1um$ KOZ, for example having 15249 and 17282 total grids respectively instead of 19732. However our EM-aware routing is superior to large KOZ scheme, having only 6636 total EM-violated grids. We note that smaller KOZ means better routability. As a result, our EM-aware routing can have significantly better EM-awareness with better utilization of routing resource than simple routing blockage scheme. Experiments in Table V are performed with $0.1um$ KOZ for both EM-aware routing and WL-driven routing.

VI. CONCLUSION

3D IC technology with die-stacking is one of the most promising technologies nowadays. However, electromigration (EM) problems can be more severe and complex in 3D ICs due to the TSV-induced stress, higher temperature and current density that affect EM. In this paper, we model EM for both AC and DC signal nets under TSV-induced stress, temperature, and current density consideration. AC signals are converted into *equivalent DC* and then analyzed for EM

TABLE VI

COMPARISON OF EM-AWARE ROUTING (EMAR) AND WL-DRIVEN ROUTING WITH VARIOUS ROUTING KEEP OUT ZONE (KOZ). $1um$, $0.7um$ AND $0.1um$ REPRESENT ROUTING KOZ FROM TSV. EMAR SHOWS SUPERIOR EM-ROBUSTNESS COMPARED TO WL-DRIVEN ROUTING WITH LARGER KOZ.

	#EM-violated wires				#EM-violated grids				Wire length[1]				#Local via			
	WL-driven			EMAR	WL-driven			EMAR	WL-driven			EMAR	WL-driven			EMAR
	$1um$	$0.7um$	$0.1um$	$0.1um$	$1um$	$0.7um$	$0.1um$	$0.1um$	$1um$	$0.7um$	$0.1um$	$0.1um$	$1um$	$0.7um$	$0.1um$	$0.1um$
uP Die0	54	56	55	37	892	1066	1167	486	39619	39604	39602	39647	620	614	614	642
uP Die1	174	177	176	89	3117	3524	3729	1040	68757	68721	68689	68996	1075	1063	1063	1146
uP Die2	145	145	146	112	2455	2760	3135	1424	43608	43626	43613	43740	736	739	736	770
IDCT Die0	87	91	91	62	1937	2167	2452	943	39141	39165	39182	39260	468	481	477	474
IDCT Die1	174	185	184	114	3222	3871	4780	1220	79581	79517	79521	79793	1224	1207	1216	1285
IDCT Die2	180	179	183	118	3626	3894	4469	1523	65230	65200	65225	65382	959	953	970	1014
Total	814	833	835	532	15249	17282	19732	6636	335936	335833	335832	336818	5082	5057	5076	5331

criticality. We effectively predict MTTF of a grid toward any routable direction across multiple routing layers, with consideration of stress gradient from TSV, temperature and current density of nets. Based on our EM modeling, we propose an effective EM-aware routing algorithm that performs net ordering with grade-based EM criticality consideration, which gives high priority to EM-critical nets while achieving the advantage of shorter net first method. A 3D EM-aware maze routing procedure is also proposed with effective cost function using predicted MTTF, and we present techniques to balance between EM-awareness and wire length during routing. Experimental results show that our EM-aware routing algorithm improves EM-reliability, having 66.4% less number of EM-violated grids with little sacrifice of conventional routing objectives.

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