Dealing with IC Manufacturability in Extreme Scaling
(Embedded Tutorial paper) *

Bei Yu Jhih-Rong Gao Duo Ding Yongchan Ban Jae-seok Yang
Kun Yuan Minsik Cho David Z. Pan

Department of Electrical and Computer Engineering, Univ. of Texas at Austin, Austin, TX 78712
Contact: dpan@ece.utexas.edu

Abstract

As the CMOS feature enters the era of extreme scaling (14nm, 11nm and beyond), manufacturability challenges are exacerbated. The nanopatterning through the 193nm lithography is being pushed to its limit, through double/triple or more general multiple patterning, while non-conventional lithography technologies such as extreme ultra-violet (EUV), e-beam direct-write (EBDW), and so on, still have grand challenges to be solved for their adoption into IC volume production. This tutorial will provide an overview of key overarching issues in nanometer IC design for manufacturability (DFM) with these emerging lithography technologies, from modeling, mask synthesis, to physical design and beyond.

1. Introduction

As the feature size of semiconductor technology scales to 14nm, 11nm, and $1\times$ nm, the industry is greatly challenged in terms of manufacturability. To deal with the IC manufacturability in extreme scaling, new lithographic technologies are adopted or under research/development, including double/multiple patterning lithography (DPL/MPL), EUV, e-bream direct-write (EBDW), directed self-assembly (DSA), and so on. While other manufacturing issues such as chemical mechanical polishing (CMP), random defects, redundant vias all play important roles in nanometer IC manufacturability, lithographic limitation is still the fundamental bottleneck. On one hand, the industry is still using the 193nm lithography to print feature size one tenth of the wavelength (e.g., 22nm and14nm), using double/triple patterning. On the other hand, there are tremendous challenges yet to be resolved in EUV (light source, etc.), EBDW (throughput) and so on. In this tutorial, we will give an overview of various key design and process integration issues, from modeling, mask synthesis, to physical design and beyond.

2. Modeling Issues

With extreme scaling, line-edge roughness (LER) becomes a fundamental limitation. While LER is mostly believed to be a purely random process, it has been shown that the image log-slope (ILS) can be added into LER modeling to consider proximity effects such as pitch spacing [1]. That is to say, there is certain layout-dependent component in LER. It would be interesting to see how LER modeling can be extended for the extreme scaling, e.g., in EUV, EBDW and DSA.

With the adoption of multiple patterning lithography, how to model the overlay errors for both front end and back end is important. Some works [2–4] discussed the overlay for DPL. It would be interesting to study the overlay modeling for the general MPL.

Hotspot detection plays an essential role in bridging the wide gap between modeling and process-aware physical design tool. In recent years, there have been a lot of hotspot detection works incorporating machine learning and pattern matching [5–10]. How to effectively combine various techniques is still an open problem, for double/multiple patterning lithography with overlay and stitch consideration.

3. Mask Synthesis Issues

Layout decomposition is a fundamental mask synthesis problem for DPL/MPL, which decomposes the original layout into two or multiple masks, subject to minimum spacing constraints and other objectives such as stitch minimization, density balancing, and overlay mitigation. Many papers have been published to address the litho-etch-litho-etch (LELE) type DPL decomposition problem, e.g., [11–16]. To mitigate the overlay-induced timing variations of LELE, overlay compensation scheme with intelligent color-interleaving was proposed in [13]. There are some works on triple patterning lithography (TPL) layout decomposition, which turns out to be a more difficult problem due to huge solution space [17, 18]. Recently, [19–22] proposed several algorithms for the self-aligned double patterning (SADP) type DPL decomposition problem. SADP layout decomposition for 1-D layout is straightforward, but it is not as intuitive for 2D layouts, due to the SADP process. For design-intent aware mask synthesis. it needs close interaction with design knowledge.

4. Physical Design Issues

As the upstream physical design (such as placement and routing) directly determines the physical layout, which to large extend affects the overall IC manufacturability and printability, physical design shall be a key step to deal with nanometer IC manufacturability with more flexibility. The standard cell design and placement should consider the manufacturing issues [23–25] or placement composability such as DPL [26, 27]. At the placement stage, [28, 29] proposed detailed placement algorithms considering the manufacturability issues. At the routing stage, several studies considered the DPL aware routing together with layout decomposition [15, 30–34] and recently there are studies on triple patterning aware routing [35, 36]. For SADP, the decomposition is not as intuitive. There are some studies on the correct-by-construction SADP friendly routing, e.g., [37, 38]. As the feature size becomes even smaller, it is possible that triple, quadruple or even more aggressive multiple patterning with both LELE-type and self-aligned will be used. This will call for new physical design tools and methodologies.

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5. Other Issues

EBDW is a promising maskless lithography technology due to its high resolution and low cost. However the key limitation for EBDW is its low throughput. To overcome this limitation, character projection (CP) has been proposed, where some complex and common shapes are prepared in a stencil. Because of the area constraint of stencil, stencil and character planning shall be performed, and designs shall also take advantage of these characters [39–41].

Another issue for EBDW is temperature during writing, since successive heating in a small region may cause severe CD distortion. Subfield scheduling that reorders the sequence of the writing process is necessary to avoid neighboring subfield writing, and therefore reduce the temperature [42, 43].

For EUV, some key issues related with DFM are the flare effect and the blank defect. Flare is a multi-scale effect which can be mitigated at the levels of both mask synthesis and physical synthesis. There are some studies to model and mitigate flare effects, e.g., [44, 45]. To alleviate the EUV blank defect, several techniques, such as pattern relocation [46] and reticle floorplanning [47] are proposed.

In the longer term, complementary lithography will keep pushing the lithography limit, as it allows two or more different lithography processes to work hand in hand to reach high quality layout patterns. One example is the hybrid lithography with EBDW and 193nm immersion processes [48, 49]. It would be interesting to study other hybrid lithography and corresponding design optimization, e.g., EBDW and DPL, EUV with DPL, and so on for the ultimate nano-patterning.

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