Self-aligned Double Patterning Compliant Routing with In-Design Physical Verification Flow

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ABSTRACT

Among double patterning techniques, Self-aligned double patterning (SADP) has the advantage of good mask overlay control, which has made SADP a popular double patterning method for sub-32nm technology nodes. However, SADP process places several limitations on design flexibility. This work exploits an alternative post routing approach that has the flexibility to resolve lithography violations without the overhead of repeated rule checking. In addition, it allows for successive refinement in the definition of lithographic violations as the process node matures, and implementation of fixes as localized ECO (Engineering Change Order) operations without needing to reroute the complete design.

1. INTRODUCTION

Double patterning has been widely used in dense layers for sub-32nm technology nodes in the industry. In double patterning lithography, adjacent patterns with the space less than the manufacturing limit must be assigned to different masks. Among double patterning techniques, Self-aligned double patterning (SADP) has the advantage of good mask overlay control compared with Litho-Etch-Litho-Etch (LELE) double patterning. This has made SADP a popular double patterning method for advanced technology nodes. However, SADP process places several limitations on design flexibility. These additional restrictions, such as fixed spacing, make it extremely hard to make small changes to the layout if yield-limiting configurations are identified at a late stage. Figure 1 shows one such example for a SADP process with fixed spacing rule. Here, a particular VIA configuration has been identified in post-routing and placement as a lithographic hotspot. In older technologies, minor adjustment to the metal layer is possible allowing elimination of the hotspot, as shown in the figure. However, this is no longer possible in the SADP process as such a change would violate the constant spacing rule. In addition, as we continue to use 193nm lithography for advanced technology nodes, the manufacturability challenges arising out of lithography process have increased. Increasingly, design rules are set to disallow only the worst of the offending configurations. Often, a second set of 'nice-to-have' design rules is possible to be defined to increase manufacturability. However, incorporating these additional constraints into an efficient industrial design flow that achieves the optimal balance of manufacturability vs. design effort remains a challenge.

There have been several double patterning aware routing works[1-3] targeted at LELE type double patterning. However, the manufacturing process and design rules are not quite the same for LELE and SADP. Therefore, those approaches cannot be extended to handle SADP awareness. SADP layout decomposition algorithms have earlier been presented[4-6] to improve SADP compliancy and reduce overlay error. However, these algorithms usually work based on the assumption that the given layout is decomposable and that the final layout has no yield impact. Some studies[7-8] perform SADP layout decomposition and routing simultaneously so that the lithographic feedback is captured during routing. Although embedding lithography-aware information in full routing may achieve higher yield, it involves significant addition of constraints and physical design time. Besides, the explosion of restrictive design rules may cause QoR (Quality of Results) degradation in terms of design metrics such as frequency, power and area. Kodama et al.[9] presented a new grid structure with routing and coloring rules embedded, which can be applied for SADP- and SAQP-aware routing. Although it guarantees the routing results are decomposable, the pins and routes must align to regular grids, which limits the possible design specification.

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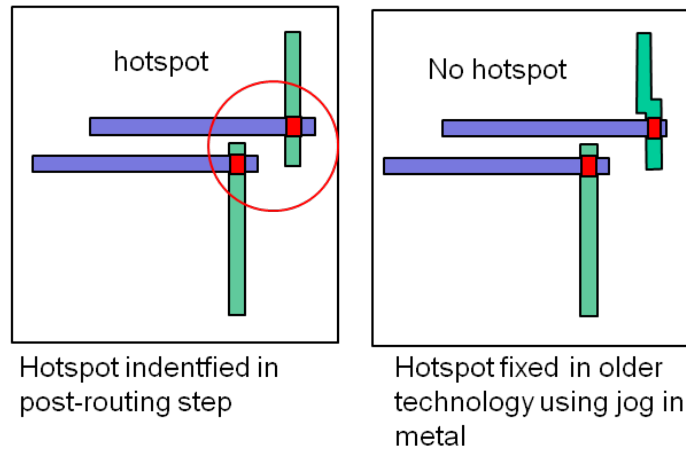

Figure 1. Example of layout changes forbidden in SADP

In-design physical verification flow[10] allows designers to configure an additional set of design rules that are not usually considered in typical routing flow, but are good for manufacturability. Violations caused by these rules are identified and then used to guide the routing engine to refine routes. Recently, Mann et al. presented a DFM optimization method[11] that adopts in-design flow. They perform hotspot fixing after obtaining the routing results, but only target at via replacement rules.

This paper exploits a post routing approach that has the flexibility to resolve lithography violations without the overhead of repeated rule checking. In addition, it allows for successive refinement in the definition of lithographic violations as the process node matures, and implementation of fixes as localized ECO (Engineering Change Order) operations without needing to reroute the complete design. We employ in-design physical verification flow in a commercial router, which allows us to perform physical verification and pass the information to the router. Therefore, by configuring lithography friendly design rules for physical verification, the router can iteratively check lithography validity and perform localized rip-up and reroute to fix violations.

The rest of the paper will be organized as follows. In Section 2, we introduce the SADP process flow, and discuss the challenges to achieve decomposable layouts and routing difficulties. We present our post routing flow in Section 3. The experimental results are discussed in Section 4, followed by the conclusion in Section 5.

2. SADP PROCESS FLOW AND CHALLENGES

2.1 Overview of SADP Process Flow

In general, spacer based patterning process involves mandrel mask generation, spacer deposition, and layout trimming by the trim mask. Depending on the design specification (characteristic of pattern width and space), Spacer-is-Dielectric (SID) or Spacer-Is-Metal (SIM) process can be applied. Recent studies[12-13] have been focus on SID-based SADP, which provides good overlay control and more design flexibility with multiple CDs of dielectric and metal[14]. Figure 2 shows the overall flow of SID-based SADP. The mandrel mask is first used to form part of the layout, and then spacer material is deposited around mandrels as dielectric. The second mask, trim mask, blocks the undesired layout area. Finally, the target patterns are obtained by metal filling process to fill the gap between spacers.

2.2 Challenges of SADP Enablement

Conventionally, designs are first placed and routed, and then a layout decomposition step is applied to divide the layout patterns into two sets for double patterning manufacturing process. One set is generated by the mandrel mask, and the other set is formed by metal filling and the trimming process. However, SADP imposes more restricted design rules and thus is not flexible for achieving decomposable layout.

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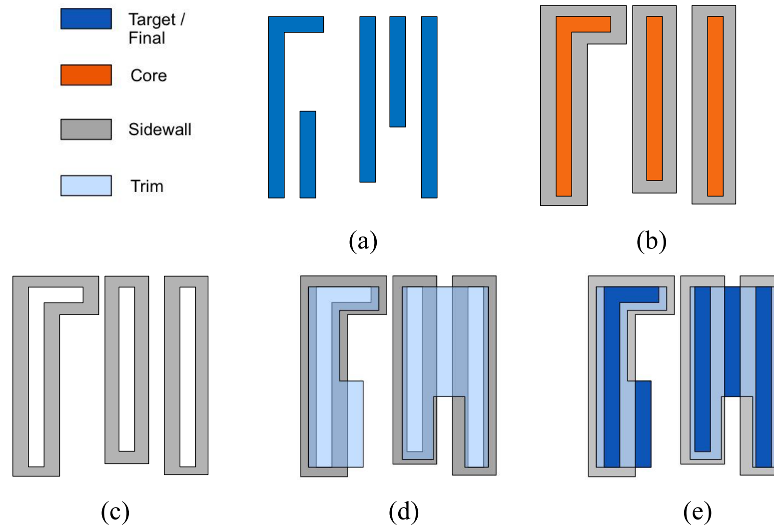

Figure 2. SADP process flow for 2D patterns. (a) Target patterns. (b) Mandrel mask and spacers deposition. (c) Spacers after mandrel removal. (d) Layout trimming. (e) Final patterns.

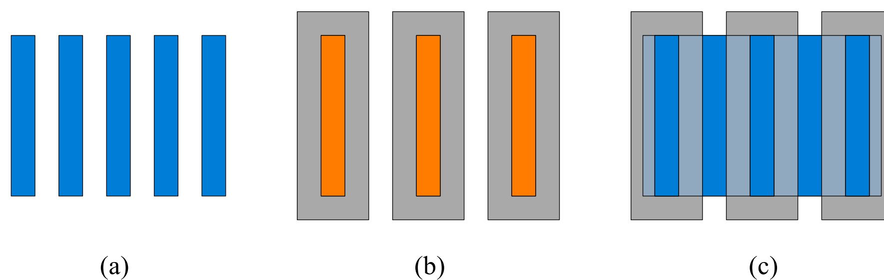

Figure 3. SADP process flow for 1D patterns, where each pattern sides are aligned to spacers. (a) Target patterns. (b) Mandrels and deposited spacers. (c) Trim mask that forms final layout patterns.

In double patterning technology, adjacent patterns with their spacing less than resolution limit must not be fabricated on the same mask. Layout decomposition for 1D patterns is trivial and can benefit from the good overlay control with spacer alignment. Figure 3 shows an example of 1D regular patterns. Since all patterns are aligned to spacers, only tip edges will suffer from overlay error, which is usually tolerable. Layout decomposition for 2D patterns, on the other hand, is much complicated and the decomposability is not guaranteed once the routing is done. Therefore, it is important to generate a SADP-friendly layout in physical design stages to enable successful layout decomposition.

2.3 Difficulty of applying lithography rules during routing

One solution to avoid SADP-unfriendly layout consists of performing post-OPC lithography simulation and identifying the layout hotspots that lead to silicon failure. Unfortunately, the lithography simulation is time consuming, and therefore cannot be used to drive the routing engine. The model based lithographic information must be correlated to topological design rules that can be understood by the routing engine.

The ability to route a given netlist within specified performance criteria (such as timing, current capacity, resistance, capacitance, etc.) in specified runtime constraints is inversely dependent on the number of design rules that need to be satisfied during routing. For 22nm node, the rule count is reported[15] up to 2000. Taking into account all design rules during the routing phase can be computationally expensive and may lead to performance degradation of the resultant layout. In practice, some important design specifications may be sacrificed in order to satisfy rules for manufacturability. Therefore, only a few selected design rules are considered during routing. However, the design rules ignored during the routing phase can be significantly important to avoid lithographically difficult hotspots, thus leading to an adverse effect on the lithography quality of the resultant design.

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Identifying the previously unconsidered design rules that caused lithographic hotspots can help successive application of selective design rules in routing without any degradation in circuit performance. For example, Figure 4 shows the impact on lithography quality (LQ) and routability when the number of design rules increases. Lithography quality *LQ(A)* corresponds to the design choice *A* is obtained by considering only a few design rules during routing, and *LQ(B)* corresponds to the design choice *B* is obtained with larger number of design rules considered during routing. If many lithography design rules are considered, the lithography quality would obviously increase, but the routability would degrade. By using feedback from lithographic simulations and application of context-dependent design rules, the lithography quality of the design can be improved significantly from *LQ(A)* to *LQ(C)* without much loss in routability or circuit performance.

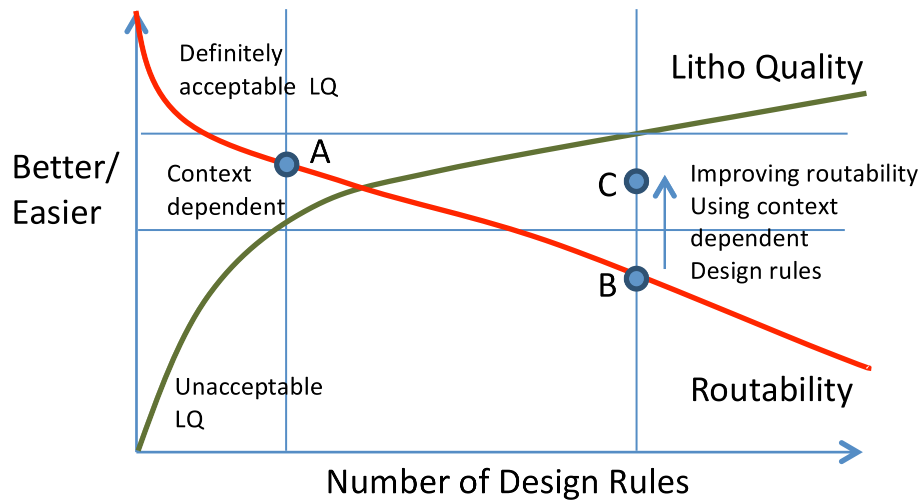

Figure 4. Lithography quality and routability based on different number of design rules.

3. SADP-COMPLIANT POST-ROUTING FLOW

We propose a new routing flow that allows SADP-compliant rip-up and reroute during post-routing stage. Figure 5 shows our overall methodology, including two main steps: lithography rule extraction and lithographic hotspot fixing. First we perform lithographic simulation after typical routing flow. We then characterize the problematic patterns with properties that can be transformed into design rules. These rules are fed back to the routing engine where problematic patterns can be fixed in post-routing stage. The lithographic hotspot fixing is proceeded until an identified quality criteria is met or the iteration upper bound is reached.

3.1 Lithography-aware design rule extration

Advanced processes rely on model-based simulation to evaluate lithography quality accurately. However, it is difficult to adopt this approach in the optimization processes because it is computational expensive. Ignoring the lithography impact in the design flow clearly will create a gap between the obtained layout and the acceptable lithography-friendly layout. As an alternative, we analyze the simulation results under the process specification and transform the important factors into rules that can be applied by rule-based approaches.

We perform lithographic simulation after typical routing flow considering only the mandatory design rules. Based on the simulation results, the analysis tool can identify faulty patterns according to process characteristics, including Edge-placement-error (EPE), variations of line-width and space, etc. We perform pattern matching that helps to classify hotspots caused by similar pattern topologies. The patterns that tend to cause larger number of hotspots are then selected and recommended as rules for improving lithography quality. Usually, they either have more restricted values for design specification, or involve particular features arrangement.

The main characteristic of these problematic patterns, including feature width, feature space, and the geometrical relation between features, are extracted and correlated to design rules. These rules are fed into the sign-off verification tool, which applies pattern matching to identify all faulty patterns in the design. The rules will also guide the routing

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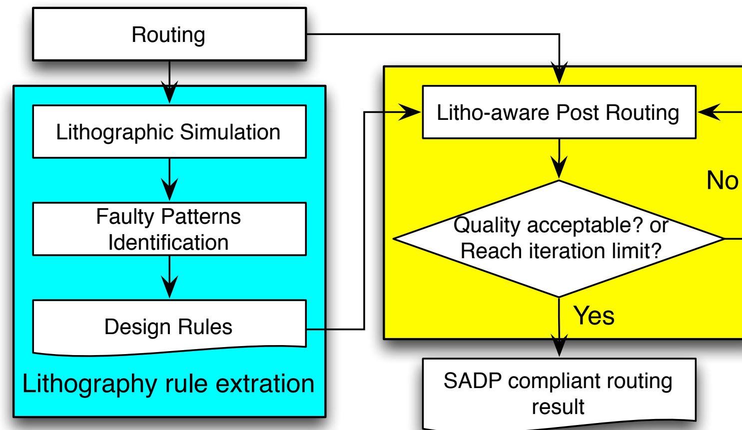

Figure 5. Overall methodology flow.

engine to fix the identified patterns. Note that lithography rule extraction only requires one time effort for a particular manufacturing process/setting. Once the lithography-aware design rules are extracted, these rules can be generally adopted by designs with the same process.

The design rule extraction step is critical to identify the few layout structures leading to highest yield loss. The following cases must be considered:

- Inaccurate rules will result in useless layout structure matches that will be processed with the same priority of the real lithographic hotspots, and thus will waste routing resources and decrease the effectiveness of the fixing flow.
- A huge number of less critical layout structures can nevertheless impact yield. Therefore, the design rule extraction step should also include these hotspots, and the neighboring environment of the hotspot must be considered. The rule should identify layout topologies that could be fixed within the extracted environment, and the fix strategy must be adapted accordingly. As an example, the rule must capture the problematic pattern but also the context to enable correction with the minimum local layout changes.
- The fixing flow is implemented after detail routing and relies on the place and route information. Therefore, the macro and standard cell internals cannot be modified. In addition, the rules must be designed to report the violation for the involved routing structure to avoid routing issues with the macro.

3.2 Lithographic hotspot fixing with in-design physical verification flow

There have been several studies on SADP-aware routing as mentioned above, but there are some difficulties to adopt those approaches in real industrial design flow. First, previous SADP-aware routing studies define new routing strategies for the router to follow, which usually requires a fundamental change of the router behavior. This imposes an implementation overhead for routing tool. Furthermore, lithographic hotspots highly depend on the technology node, manufacturing process, and other parameters. It would be a huge burden to modify router implementation for different processes and foundry settings. Second, although considering SADP compliancy during full routing provides large solution space for decomposable layout, it is computationally expensive to handle all rules. DRC and DFM rule count has been increased as the technology node shrinks. The router complexity to check these rules increases even faster because the rules are more complicated. Too much rules also restrict the solution space for other optimization, such as timing, power, etc. Third, foundries often provide recommended rules for manufacturability improvement except the mandatory DRC rules. These rules are “nice-to-have,” but are enforced strictly. Therefore, these recommended rules should be given lower priority than DRC rules during physical design flow.

We adopt industrial in-design physical verification flow to integrate lithography awareness into routing stage. In-design physical verification flow performs concurrent physical design and physical verification, which helps to improve the turnaround time between physical design and physical verification. The concept is to integrate physical verification

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into routing engine and use verification results to guide the following rip-up and re-route. With this flow, we can formulate SADP-compliant rules as a part of sign-off physical verification, which performs pattern matching to identify violated layout structures.

Our methodology first performs regular routing without consider any manufacturing issues. The lithography-aware rules are then added into the signoff rule deck. We then apply physical verification to identify lithographic hotspots and to guide the localized rip-up and reroute. This process is iteratively performed until all hotspots are fixed or a given iteration count is achieved. The proposed flow has the following features:

1. Easy integration into the existing design flow. Since the SADP-aware rules are configured as signoff rules, there is no need to change the router implementation. These rules are described by formal semantics similar to DRC rules, which creates no ambiguity and can be easily modified depending on different process parameters.
2. Efficient SADP-aware routing. The SADP-aware rules are not considered in the main routing step, which avoids the runtime overhead for extra rule checking.
3. Prioritized rules checking. Our methodology only allows SADP-aware rules in post routing stage. Therefore, the router can first focus on the mandatory design rules and allows more optimization space in the main routing step. In addition, only problematic patterns will be rerouted, which avoids excessive layout changes to affect prior optimized results.
4. Inherent benefits with in-design flow. The in-design flow adopts accurate signoff physical verification with pattern matching, which is especially suitable for checking lithographic hotspots that are usually complicated. In addition, in-design flow can still consider timing closure that helps to keep design performance.

4. EXPERIMENTAL RESULTS

The proposed methodology flow is tested on advanced process node designs. We first perform lithographic simulation on designs with the same technology. By observing patterns with bad printability, we extract their features and correlate them to design rules. Table 1 shows the results by feeding lithography-aware rules into our flow. Three rules are verified after the regular routing, and patterns that violate these rules are identified and re-routed locally. To prevent too much overhead for lithography-aware post routing, we limit the fixing iterations to 3. For each rule, we show the violation fix rate after all iterations. Note that these rules are considered simultaneously in each iteration.

The proposed flow works more effective for Design 1, where each rules has more than 65.6% violations fixed. Design 2 is larger and more complex, and thus the solution space for re-route is more limited. The breakdown of the violation percentages account for each rule is shown in Figure 6. It can be seen that Rule 1 tends to identify more lithographic hotspots. The overall violation fix rate for Design 1 is 75.6%, while for Design 2 is 24%. Figure 7 shows sample layouts before and after the hotspot fixing.

We further verify the impact of our lithography rules and re-routed solutions by performing the lithographic simulation. The hotspot counts are considerably reduced, where the hotspot reduction rate is 58.7% for Design 1, and 51% for Design 2. Figure 8 and Figure 9 show the lithographic simulation results before and after the hotspot fixing for Design 1 and Design 2 respectively, where the hotspot density is much reduced after applying the proposed flow.

Note that these lithography-aware rules are not mandatory. Although our goal is to remove them as more as possible, it is okay not to remove them completely since they are not critical design rules. However, we should make sure the design retains its optimized state from prior routing stage, in terms of normal design rules, timing, etc. We collect the

Table 1. Post routing results after fixing lithography-difficult hotspots.

Design	Violation Fix Rate				Hotspot Red. Rate	ΔDRC	ΔWNS	ΔTNS	ΔCPU
	Rule 1	Rule 2	Rule 3	Total					
Design 1	81.2%	65.6%	71.7%	75.6%	58.7%	0	0	0	1.6%
Design 2	20.3%	55.2%	47.3%	24.0%	51%	-25	-1	0	30%

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DRC report and timing report after applying our flow. Table 1 shows the difference of DRC (ΔDRC), the worst negative slack (ΔWNS), and the total negative slack (ΔTNS). Our flow does not degrade the timing performance. In fact, the timing of Design 2 is slightly improved after several rip-up and re-route. It is worth mentioning that no any violations are introduced in the mandatory design rules. The CPU time is reported as the additional post routing against the normal routing time. Although Design 2 is smaller than Design 1, its hotspot fixing time is much larger, reflecting more difficulty in finding valid routes.

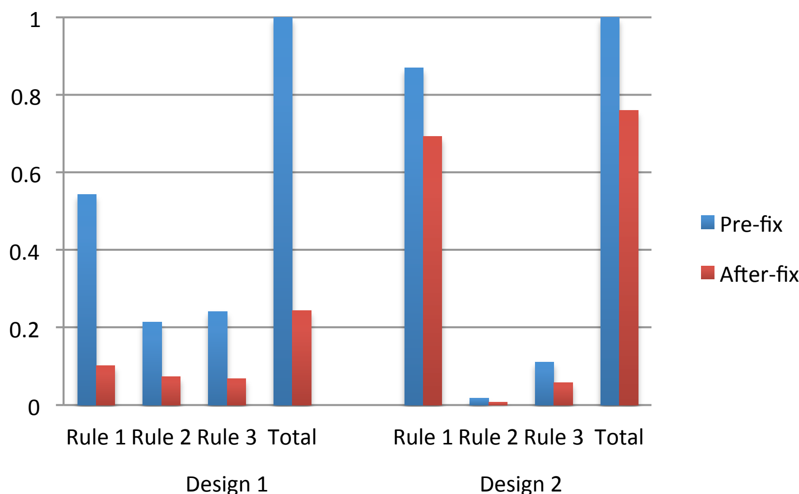

Figure 6 Normalized violation count for each rule.

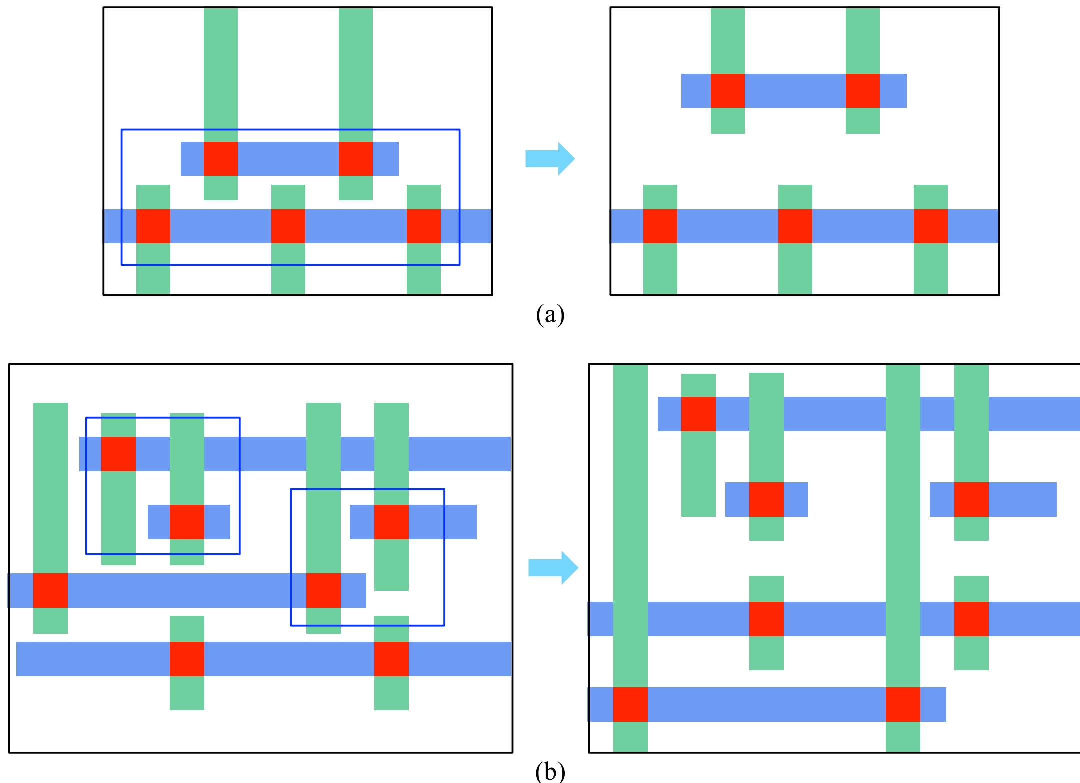

Figure 7. Sample layouts before (left) and after (right) fix. Blue boxes identify hotspots.

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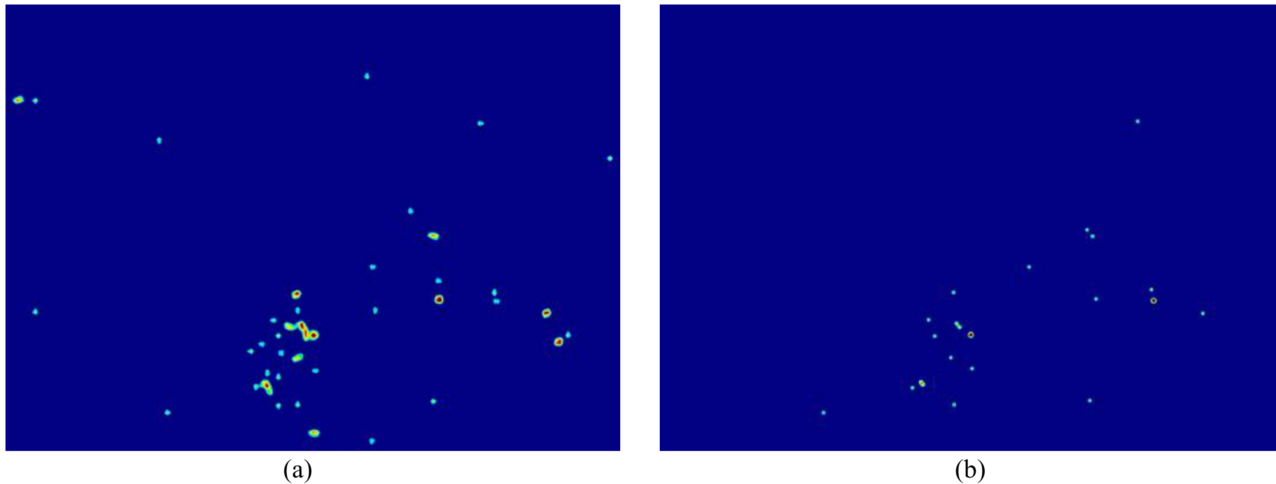
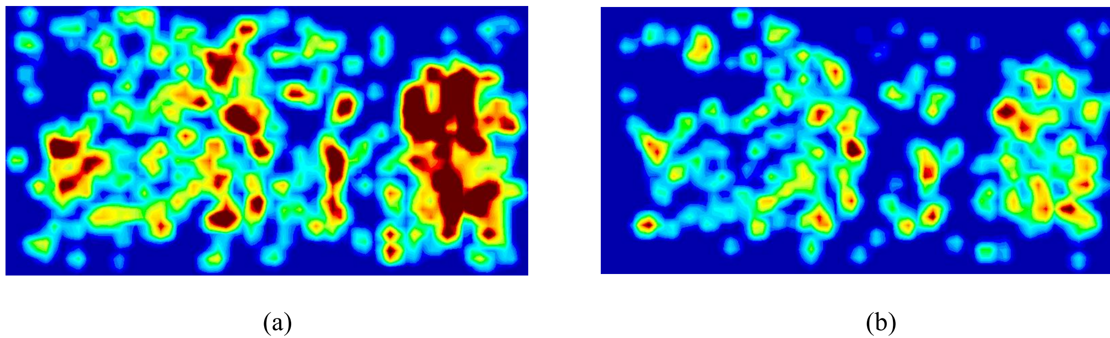

(a) (b)
Figure 8. (a) Pre-fix and (b) after-fix hotspot density map of Design1. Red colors show regions with high hotspot density.


(a) (b)
Figure 9. (a) Pre-fix and (b) after-fix hotspot density map of Design 2.

The above results are obtained under fixed rip-up and re-route iterations for both Design 1 and Design 2. We perform another experiment to study the impact of iteration number. We observe that when the iteration number is doubled, the fix rate of certain rules is increased while that of the others is decreased. The overall fix rate by doubled iterations is even slightly worse than the results with less iteration. This shows that the fix rates in Table 1 has almost reached the upper bound for the given design space and rules. As a future study, we may prioritize these lithography rules according to their lithographic impact. For example, the most important rules are applied at the first iteratioin, and the other rules are gradually added in the following iterations.

5. CONCLUSIONS

We propose a SADP-friendly post routing methodology that adopts industrial in-design physical verification flow. Lithography-aware design rules are extracted from the lithographic simulation and are fed into the verification tool for hotspot detection. The identified hotspots can then guide the localized rip-up and re-route. We compare the lithography quality between the typical routing flow and the proposed flow. The proposed methodology successfully reduces lithographic hotspots without introducing new violations for the existing design rules and without quantitatively impacting QoR of the design. Simulation results show that the hotspot reduction rate can be up to 58.7% compared to the design without considering lithography-aware rules.

The lithography-aware design rules are treated equally and optimized simultaneously in this work. However, the lithographic impact of each rule and the difficulty to fix it may be different. As a future work, we would like to further study the importance of these rules and prioritize them during the iterative hotspot fixing to maximize the lithography quality.

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6. ACKNOWLEDGMENTS

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