Standard Cell Pin Access and Physical Design in Advanced Lithography

Xiaoqing Xu[a], Brian Cline[b], Greg Yeric[b] and David Z. Pan[a]

[a]ECE Dept. University of Texas at Austin, Austin, TX 78712 USA
[b]ARM Inc., Austin, TX 78735 USA
Email: {xiaoqingxu, dpan}@cerc.utexas.edu; {brian.cline, greg.yeric}@arm.com

ABSTRACT

Standard cell pin access has become one of the most challenging issues for the back-end physical design in sub-14nm technology nodes due to increased pin density, limited number of routing tracks, and complex DFM rules/constraints from multiple patterning lithography. The standard cell I/O pin access problem is very difficult also because the access points of each pin are limited and they interfere with each other. There have been several studies across various standard cell and physical design stages, including standard cell pin access optimization, placement mitigation and routing planning, to achieve overall pin access optimization. In this paper, we will introduce a holistic approach across different design stages to deal with the pin access issue while accommodating the complex DFM constraints in advanced lithography.

Keywords: Pin Access, Physical Design, Multiple Patterning

1. INTRODUCTION

In sub-20nm, pin access is becoming extremely challenging during the detailed routing phase.[1] The local standard I/O pin access is difficult as limited number of access points is available for the detailed router and they interfere with each other within limited number of routing tracks. Due to congested routing space on lower metal layers, the routing resource competitions among different nets has been increasing significantly. Moreover, the continued technology scaling has been pushing the pitch shrinking into the resolution limits of 193nm wavelength lithography. Thus, complex design-for-manufacturability (DFM) techniques,[2,3] such as multiple patterning lithography (MPL), have been adopted to enable further technology scaling, which makes the pin access interference even more complicated.[4] In general, there are two kinds of multiple patterning lithography (MPL), including Litho-Etch-Litho-Etch (LELE) type and self-aligned type of MPL. The LELE type of MPL can relax the coloring constraints by allowing stitch insertions but may introduce significant overlay depending on layout design and mask assignment results.[5–9] The self-aligned type of MPL provides tight control on the overlay and line-edge-roughness but introduces complex geometric constraints and prefers unidirectional (1D) layout patterns.[10–12] Practical applications of the MPL are highly technology specific and foundry dependent.[13,14] For example, the LELE-type of MPL is a preferred option for cut mask or via layers,[15] while the self-aligned type of MPL is preferable for lower metal layers with tight pitches.[16–18] An example of the self-aligned double pattering (SADP) for 1D layout patterns is shown in Fig. 1.[11,19] The track-based coloring can be applied in Fig. 1(b), which further leads to the trim mask solution and cut mask solution in Fig. 1(c) and Fig. 1(d), respectively.[16] The complexity of geometric and coloring constraints comes from the trim mask or cut mask, which is dominated by some specific patterning techniques, such as single patterning or multiple patterning.[15,16]

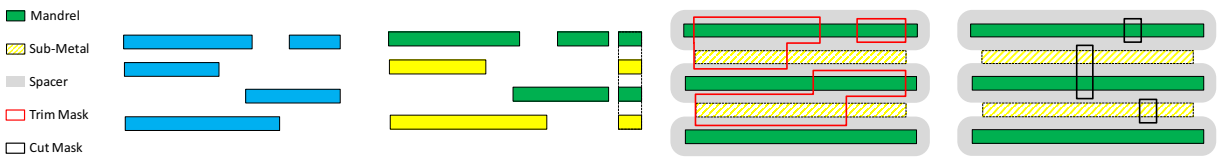


Figure 1. Track-based coloring for unidirectional layout patterns with SADP, (a) unidirectional target patterns, (b) track-based coloring, (c) SADP with trim masks, (d) SADP with cut masks.[20]

In general, the coloring and geometric constraints from MPL have significantly increased the amount of pin access interference among standard cell I/O pins close to each other. For local standard cell pin access, the ideal locations of metal and via geometries are dependent on the neighborhood around geometries in question under advanced MPL constraints. This makes the manual pin access optimization almost impossible in advanced technology nodes. The placement and routing-level impacts of pin access interference are further demonstrated in Fig. 2. To reduce pin access interference at the placement level, white space between neighboring cells can be added to allow more space on lower metal layers for pin access connections as shown from Fig. 2(a) to Fig. 2(b). The routing-level pin access interference is shown in Fig. 2(c), where the routes of first two nets have blocked the M1 pin of the remaining net, leading to pin access failure. However, if a different access point or routing track has been selected for net A, pin access success can be achieved as shown in Fig. 2(d). Furthermore, as a typical detailed router is sequential in nature, the net ordering plays an important role in the pin accessibility or detailed routability during the routing stage.

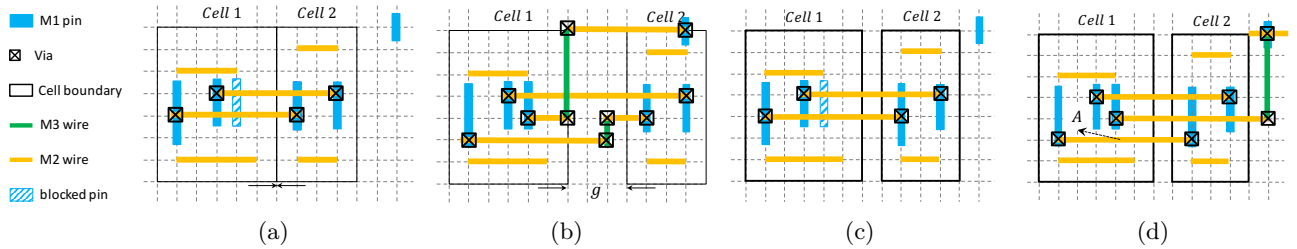


Figure 2. Placement and routing level impacts on standard cell pin access, (a) two cells placed next to each other, (b) two cells placed with a gap of three placement pitches, (c) pin access failure during detailed routing, (d) pin access success during detailed routing.[20]

There has been a wide range of research studies dedicated to the pin access issues, including standard cell synthesis and optimization,[1,4,19,21] placement mitigation,[22] global routing[23,24] and detailed routing.[25–27] However, few works have been focusing on the increased pin access interference due to the complex DFM constraints. Moreover, previous works mainly deal with the pin access issue at a single design stage. The increasing pin access interference aforementioned motivates us to systematically address the pin access issue across various physical design stages under advanced lithography constraints. In this paper, we present a holistic approach to address the pin access issue while considering MPL-induced complex pin access interference, including standard cell pin access optimization, routing and placement planning.

The rest of this paper is organized as follows: Section 2 presents the preliminary background and the overall flow for the pin accessibility optimization, thereby routability improvement, across different physical design stages. Section 3 introduces the pin access optimization engine at the cell level while considering multiple patterning constraints for via and metal layers. Section 4 discusses routing and placement-level pin accessibility and related optimization schemes. Section 5 demonstrates the effectiveness of proposed approaches with comprehensive experimental studies. Section 6 concludes the paper and discusses some future directions.

2. PRELIMINARIES AND OVERALL FLOW

2.1 Advanced Lithography Constraints

Multiple patterning lithography has been widely adopted to maintain the minimum feature size shrinking, which also introduces complex geometric and coloring constraints during layout design and optimization. Fig. 3 illustrates related DFM constraints in advanced technology nodes. As shown in Fig. 3(a), a set of line-end rules on the same routing track or neighboring routing tracks have been introduced to obtain SADP-friendly 1D metal patterns. Specific line-end rules include on-track space (A), off-track space (B), off-track overlap (C) and off-track offset (D) rules.[4] Line-end extension techniques have been extensively used to fix related design rule violations and improve the lithography printability.[4,28,29] For the via layer, LELE-type of MPL has introduced same-mask minimum distance rule (d_0) and different-mask minimum distance rule (d_1) as illustrated in Fig. 3(b). Fig. 3(c) and Fig. 3(d) demonstrates the 2D routing patterns and 1D routing patterns for a net, respectively.

For 2D routing patterns, the metal width is enlarged in the non-preferred direction, e.g., the vertical M2 wire in Fig. 3(c), to improve the printability of associated routing patterns. However, in advanced technology nodes, SADP for metal layers prefers 1D routing patterns as shown in Fig. 3(d), which provides better overlay and line-edge-roughness control. For 1D routing patterns, switching routing direction means changing routing layer, which leads to extra vias and different pin access points in Fig. 3(d). Within back-end physical design flow, these advanced lithography constraints need to be considered to obtain lithography-friendly layout.

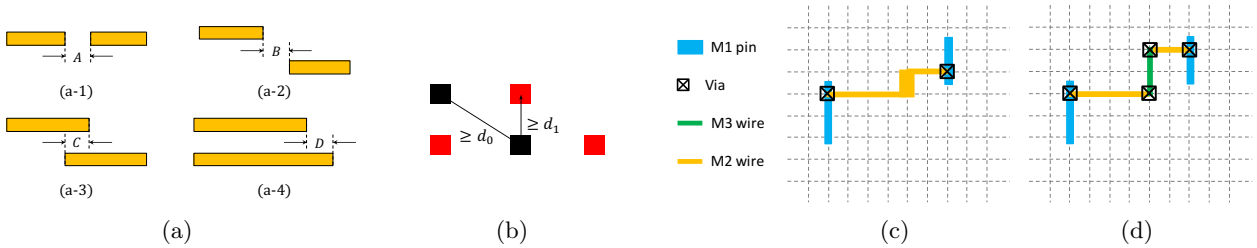


Figure 3. (a) Line-end design rules for SADP, (b) LELE coloring rules for via patterns, (c) 2D routing patterns with restrictive design rules, (d) 1D routing patterns with extra vias.[4, 11, 20]

2.2 Overall Flow

Fig. 4 shows the overall physical design flow for pin accessibility and routability improvement in advanced lithography. First, we propose the pin access optimization engine to maximize the pin access flexibility for each individual standard cell while capturing the pin-to-pin interference under advanced lithography constraints.[4] At the placement level, the pin congestion or pin distribution plays a critical role in the detailed routability, which motivates us to relax the space among standard cells for better pin accessibility. Therefore, placement mitigation techniques are further discussed to reduce the pin congestion at the detailed placement stage.[22] Then, pin access planning schemes are proposed to handshake the standard cell level pin access and detailed routing stage, which aims at improving the detailed routability with 1D routing patterns. At each physical design stage aforementioned, complex coloring and geometric constraints for via and metal layers need to be explicitly considered to obtain lithography-friendly layout in a correct-by-construction manner.

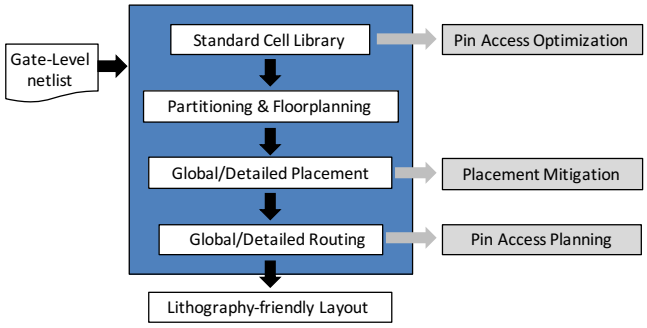


Figure 4. Overall physical design flow for pin accessibility optimization in advanced lithography.

3. PIN ACCESS AND STANDARD CELL LAYOUT CO-OPTIMIZATION

For the standard cell design, the mainstream industrial routine still follows extensive handcrafted design and optimization. In advanced technology nodes, the cell height is a pre-determined value, which allows for limited number of access points for local standard cell pin access. These access points further interfere with each other under advanced lithography constraints as shown in Fig. 3. Although standard cell designers can assist physical design tool through intelligent I/O pin design, these complex DFM rules and neighborhood interactions make manual pin access optimization very difficult in $14nm$ and below. In this section, we propose pin access and standard cell layout co-optimization (PICO) to maximize the cell-level pin access flexibility.

For clear problem formulations, we first propose a set of definitions and metrics for local standard cell pin access. A typical standard cell layout is shown in Fig. 5(a), where only M1 I/O pins, M2 within-cell connections and M2 routing tracks are drawn to illustrate the pin-access scenario for an individual cell. Conceptually, to access the I/O pins of a cell at the routing stage, the router needs to have a set of M2 wires, with each M2 wire connected to an M2 I/O pin directly or to an M1 I/O pin through a via-1. To represent the pin access scenario aforementioned, we introduce the following definitions on (valid) hit point and (valid) hit point combination.[4]

Definition 1 (Hit Point). *The overlap of a Metal-2 routing track (which is pre-determined by the place and route tool) and an I/O pin shape is defined as a Hit Point for that particular I/O pin.*

Definition 2 (Hit Point Combination). *A set of hit points (with a defined access direction, left or right) where each I/O pin in the standard cell is accessed exactly once is defined as a Hit Point Combination for that cell.*

Definition 3 (Valid Hit Point Combination). *If a hit point combination induces zero design rule violations, it is considered a Valid Hit Point Combination. Otherwise, it is considered to be invalid.*

Definition 4 (Valid Hit Point). *If a hit point can be accessed from both directions within some valid hit point combinations for one cell, it is considered a valid hit point. Otherwise, it is considered to be invalid.*

A hit point combination for pin access is shown in Fig. 5(c) with a set of M2 wires and via-1's to connect to the I/O pins of the cell. In a typical $10nm$ technology setup, for a valid hit point combination, we first need to seek a LELE-friendly via-1 positions and then line-end extensions are further performed to achieve SADP-friendly M2 wires as shown in Fig. 5(d). If either LELE-friendly via-1 positions or the SADP-friendly M2 wires can not be obtained, a hit point combination is invalid. In the following sub-sections, we introduce the LELE-aware via-1 assignment and SADP-aware pin access for a given hit point combination.

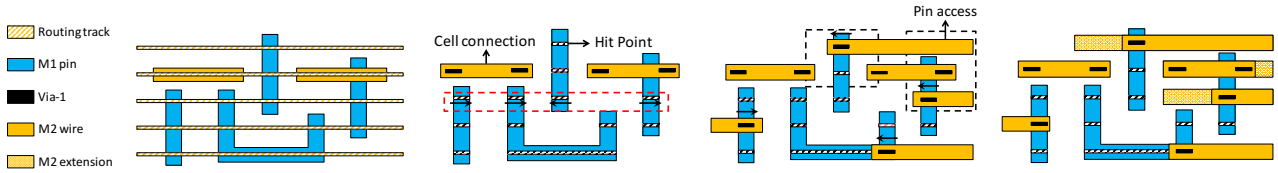


Figure 5. Standard pin access optimization, (a) standard cell I/O pins and M2 routing tracks, (b) hit points and M2 within-cell connections, (c) a hit point combination with M2 pin access, (d) SADP-friendly pin access with M2 extensions.[4]

3.1 LELE-Aware Via-1 Assignment

In advanced technology nodes, to access a standard cell on the M2 layer, a set of LELE-friendly via-1's need to be assigned to connect between M1 I/O pins and pin access M2 wires. It is well-established in literature that no odd cycles exist in the corresponding conflict graph for the LELE-friendly layout patterns.[5,6] Thus, for LELE-aware via-1 assignment, we seek a set of via-1's and the associated conflict graph is free of odd cycles. An example on LELE-aware via-1 assignment is shown in Fig. 6. For the given hit point combination in Fig. 6(a), there are two kinds of via-1's in the design. One kind is the via-1's for intra-cell connection, including v_1 to v_4, which can not be changed during the pin access optimization phase. The other kind is the via-1's landing on the hit points (hp_1 to hp_4) and these via-1 positions are to be designed under LELE coloring constraints. The complexity comes from the long hit point, such as hp_3, where the via-1 position is not determined and the conflict graph can not be explicitly constructed as shown in Fig. 6(b). To make use of long hit points, grid-based segmentation is adopted for long hit points and conflict graph is further constructed as shown in Fig. 6(c). To obtain the optimal via-1 assignment with minimum M2 usage, we estimate M2 usage cost of each potential via-1 position and backtrack the via-1 assignment while maintaining minimum overall M2 usage cost and avoiding the odd cycles in the conflict graph as shown in Fig. 6(d).[4] The outcome of the LELE-aware via-1 assignment will be a legal set of via-1's with minimum M2 usage for a given hit point combination if one exists. Otherwise, the hit point combination is determined to be invalid as not legal via-1 assignment can be found.

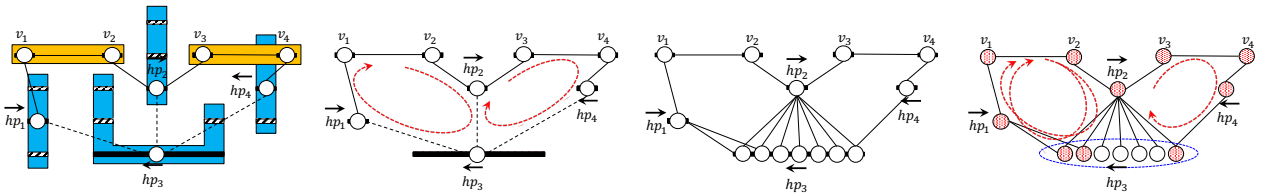


Figure 6. LELE-aware via-1 assignment, (a) standard cell I/O pins and via-1's for within-cell connections, (b) conflict graph for hit points and via-1's, (c) conflict graph with grid-based segmentation for long hit points, (d) odd cycles in the conflict graph.[4]

3.2 SADP-Aware Pin Access

The SADP-aware pin access seeks a set of M2 wires with line-end extensions for a given LELE-friendly via-1 assignment of the associated hit point combination. The need of M2 line-end extensions comes from the observation that, under SADP-specific geometric constraints in Fig. 3(a), we can not simply depend on the via-1 positions to decide the line-end positions of corresponding M2 wires as shown in Fig. 5(d).[4] For local M2 pin access, given the initial line-end positions, the objective is to minimize the M2 usage while determining legal M2 line-end positions within the standard cell boundary. The set of SADP-specific rules in Fig. 3(a) can be further formulated into mathematical constraints of the line-end positions. Furthermore, the mathematical formulations of the objective and constraints aforementioned can be adapted to mixed integer linear programming (MILP) formulation, where integer variables are introduced to allow for the relative order changes of line-end positions for different M2 wires. We can also relax the MILP formulation into linear programming (LP) formulation by fixing the relative orders of M2 line-end positions based on the initial conditions determined by the via-1's. Here, the MILP formulation will achieve an optimal set of M2 wires if one exists while the LP formulation provides degraded solution qualities with much faster runtime. It is worthwhile to compare these two formulations to empirically validate the importance of relative order changes of line-end positions during the pin access optimization phase.

We have explained the pin access optimization (PAO) techniques, including LELE-aware via-1 assignment and SADP-aware pin access, for a given hit point combination. By backtracking all hit point combinations for a standard cell, the PICO engine will apply the PAO techniques and decide the validness of each hit point combination. Therefore, the PICO engine will maximize the pin access flexibility, i.e. finding all valid hit point combinations and hit points for a specific standard cell.

4. ROUTING AND PLACEMENT PLANNING

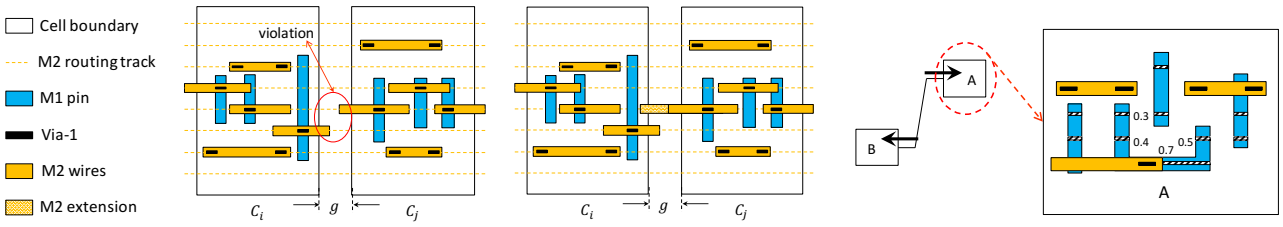
4.1 Detailed Routing Planning

A typical detailed router seeks the routing of nets in a sequential manner. This means the M2 wires for routed nets may block the pin access points of other cells, the connections of which have not been obtained yet as shown in Fig. 2(c). Although standard cell pin access optimization engine may provide many valid hit point combinations for local pin access, sequential detailed routing brings severe degradations on the pin accessibility of remaining cells associated with those nets not yet routed. At the routing level, each cell has a determined position within a standard cell row, which leaves the routing planning as the only opportunity to improve the pin accessibility or detailed routability. In this section, we propose a set of pin access planning schemes based on the intra-cell and inter-cell pin access pre-computation. We further demonstrate an entire detailed routing flow making use of the pin access planning schemes to boost the pin accessibility.

4.1.1 Look-Up Table Construction

When cells are placed next to each other in a standard cell row, inter-cell pin access interference is unavoidable under limited amount of routing space and advanced lithography constraints. As shown in Fig.7(a), two cells (C_i and C_j) are placed next to each other with gap distance as g. An extra rule violation is introduced when selecting one intra-cell pin access solution for each cell, which can be fixed by additional line-end extensions

shown in Fig. 7(b). The procedure aforementioned captures the pin access interference between cells, i.e. inter-cell pin access. For a standard cell library, due to limited number of intra-cell pin access solutions,[4] inter-cell can be further evaluated using the PICO engine discussed in Section 3. In particular, both intra-cell and inter-cell pin access can be pre-computed and stored in a look-up-table (LUT) for a given standard cell library. To avoid the LUT size explosion, we identify a set of pin-access critical cells and only construct inter-cell pin access LUT among them. A standard cell is defined to be pin access critical if it has a small number of valid hit point combinations or some I/O pin have a small number of valid hit points.[20] For a standard cell library, the pin access LUT will store all valid hit point combinations for each cell and compatible pairs of valid hit point combinations when two cells are placed next to each other with a pre-specified gap distance.[20]



(a) (b) (c)

Figure 7. (a) Inter-cell pin access interference with a violation, (b) fix the violation by line-end extension, (c) local pin access planning with dynamic hit point scoring.[20]

4.1.2 Single Row Pin Access Graph

For modern physical design, standard cells share the same height and are aligned horizontally within some pre-specified rows. Power and ground rails run from left to right of the design. Given a row of standard cells, we build the single row pin access graph as shown in Fig. 8. For each cell within the row, a set of graph nodes are introduced with each node corresponding to one valid hit point combination, i.e. one intra-cell pin access solution, for that particular cell. An edge is added between two nodes for neighboring cells from left to right if the two corresponding valid hit point combinations are compatible with each other within the pin access LUT. A virtual source and sink are added on the left and right, respectively. For the single row pin access, we have the following observation.[20]

Observation 1. *The pin accessibility of the standard cells on the M2 layer within the single row is equivalent to the existence of a path from s to t of the pin access graph associated with that particular row.*

From Fig. 8(a) to Fig. 8(b), graph simplification techniques are applied to reduce the number of nodes and edges within the graph. In particular, for some neighboring cells, all pairs of intra-cell pin access solutions are compatible with each other. By adding virtual source and sink nodes, various independent components can be extracted from the pin access graph. Based on Observation 1, a pin access graph component is defined to be infeasible for pin access when no feasible path exists from s to t of that pin access graph component.[20] Since our global pin access planning scheme highly depends on frequent queries on pin access graph components, it is important to apply the graph simplification techniques to control the node size of each graph component. As demonstrated in Fig. 8(b), some routed nets may create routed M2 wire on top of the cells within specific rows, which means some valid hit point combinations will be blocked, such as orange nodes in the figure. This makes the graph component on the right infeasible as no path exists from source to sink in Fig. 8(b).

4.1.3 Pin Access Planning

In this sub-section, we introduce the local and global pin access planning schemes, which make use of the pre-computed pin access interference to guide the detailed routing procedure for better routing solution qualities. Our local pin access planning scheme is based on the dynamic hit point scoring technique. As shown in Fig. 7(c), a net is connecting pin A and pin B. For the connection to pin A within some cell shown in the figure, there are

several hit points available. To differentiate various hit points available for a particular pin, we calculate the hit point score as follows.[20]

$$score(hp_i^{kh}) = \frac{\text{the number of valid hit point combinations associated with } hp_i^{kh}}{\text{total number of valid hit point combinations for } C_i} \quad (1)$$

In Eqn. 1, C_i denotes i^{th} cell and hp_i^{kh} denotes the h^{th} hit point of k^{th} I/O pin for C_i. Our dynamic hit point scoring technique is aware of the routed M2 blockage on top of the cells as shown in Fig. 8(b).

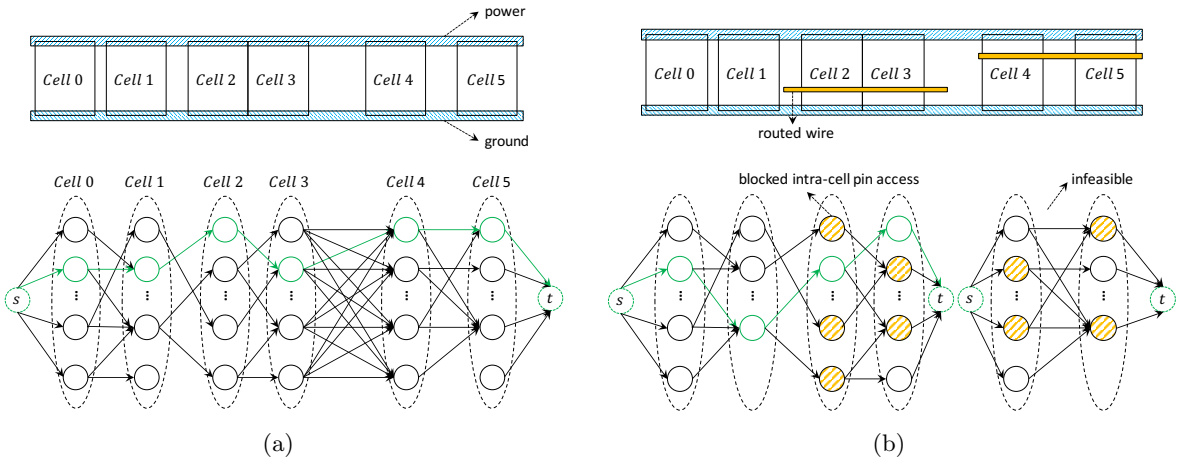
The hit point selection scheme aforementioned is purely local as only intra-cell pin access interference is used to guide the hit point selection. We further propose the global pin access planning scheme to reduce the inter-cell pin access interference and improve the routing solution qualities. The key component of the global pin access planning scheme is the net deferring technique, which dynamically adjust the net ordering based on the feasibility of pin access graph components. Specifically, during sequential routing procedure, we maintain the existence of source-to-target paths within each component of pin access graphs to preserve the pin accessibility of remaining nets. Thus, the dynamic weight for net ordering is calculated as follows.[20]

$$order(n_k) = HPWL(n_k) \cdot (1 + \alpha \cdot \min\{hp_s, hp_t\}) + DCost(n_k) \quad (2)$$

In Eqn. (2), $HPWL(n_k)$ denotes the half-perimeter wirelength of net n_k, α is a user-defined parameter, hp_s and hp_t denote the number of valid hit points for source and target pins, respectively. This means those nets with smaller number valid hit points for source or target pins have the higher priority on the net ordering. $DCost(n_k)$ is the deferring cost of net n_k. For the net deferring technique, we trace the pin access graph components impacted by the routed M2 wires once a net is routed. If no feasible path can be found from source to target of some graph component, the net will be ripped-up and the deferring cost will be increased before rerouting that net. It shall be noted that one net may be deferred for several times depending on the deferring cost upper bound. To quantify that, we introduce the following definition.[20]

Definition 4.1 (Deferring Cycle). *Deferring cycle is the maximum number of times that a net is deferred before reaching the cost upper bound.*

With the local and global planning scheme, some nets within the design are not successfully routed depending on the problem complexity. The pin access driven rip-up and reroute is further proposed to improve the ultimate routability. Our pin access drive rip-up and reroute scheme is achieved by incorporating the dynamic hit point scoring in Eqn. 1 into the traditional rip-up and reroute procedure.[30,31]



(a) (b)

Figure 8. Global pin access planning with single row pin access graphs, (a) initial pin access graph, (b) updated pin access graph with graph simplification and routed M2 wires.[20]

4.1.4 Detailed Routing Flow

Our detailed routing flow follows the sequential routing procedure with single-net routing guided by the A* search algorithm and constrained by 1D routing patterns. Consider a path from one grid (g_i) with cost $c(g_i)$ to its neighbor grid (g_j) with cost $c(g_j)$, the grid cost is calculated as follows,[20]

$$c(g_j) = c(g_i) + \theta \cdot (1 - score(g_j)) + \eta \cdot c(forbid(j)) + \beta \cdot c(WL_{ij}) + \gamma \cdot c(via_{ij}) \quad (3)$$

In Eqn. (3), $score(g_j)$ is the dynamic hit point score for the hit point associated with g_j if g_j is a source or target grid. $score(g_j)$ is set to 1 for other routing grids. This enables the local pin access planning scheme, which means single-net routing prefers the hit points with higher scores for the source or target pins. $c(forbid(j))$ is the forbidden cost for the grids within the prohibited region under SADP constraints.[11,32] $c(WL_{ij})$ and $c(Via_{ij})$ are the wirelength and via cost, respectively. $\beta, \gamma, \theta, \eta$ are user-defined parameters. The overall detailed routing flow is further demonstrated in Fig. 9. Taking the standard cell library as an input, pin access LUT is constructed using PICO engine. Then, single row pin access graphs are constructed for all standard cell rows within the design based on cell placement information and pin access LUT aforementioned. Sequential detailed routing is further performed using local and global pin access planning schemes. Before obtaining the final routing results, pin access driven rip-up and reroute is adopted to improve the routing solution quality. In particular, design rule legalizations, such as line-end extensions for SADP friendliness, are performed simultaneously with the routing procedure.

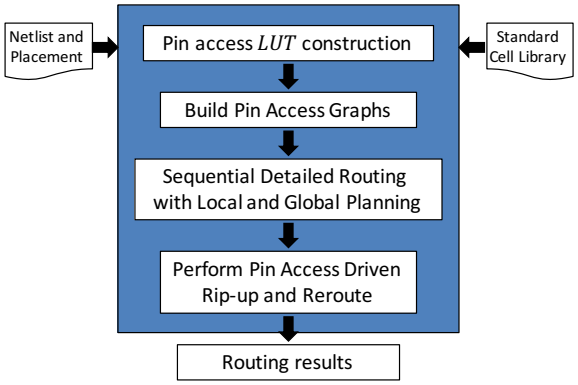


Figure 9. Overall detailed routing flow.

4.2 Placement Mitigation

The placement-level impacts on pin access become critical when cells are placed too close to each other, which leads to high pin congestion and severe pin access interference at both intra-cell and inter-cell level. Therefore, reducing pin congestion or relaxing the space between standard cells is a major technique to improve the standard cell pin accessibility at the placement stage as shown in Fig. 2(b).[22] Novel placement mitigation techniques have been proposed[22] to manage the amount of space between cells. It depends on the pin cost function to identify hard-to-access standard cells and quantify the cell-to-cell pin access interference. Specifically, the pin cost function consists of a pin-existence cost (PEC), a pin-area cost (PAC) and pin-resolution (or spacing) cost (PRC),[22] which captures the local pin congestion to the first order. Moreover, the pin cost of each cell can be further incorporated into the detailed placement algorithms to relax the space among hard-to-access cells in a consistent manner.

However, the advanced lithography constraints bring complex interference at both via and metal layer. The first order approximation of pin congestion, i.e. the pin cost function aforementioned, may become obsolete. For example, the pin-area cost can not represent the detailed routing scenario with 1D routing patterns, where the number of hit points or available routing tracks for a I/O pin become more important than the pin area. The other important concern lies on M2 and via-1 routing blockages and congestion. In advanced technology nodes, M2 wires and via-1's may be used for intra-cell routing of complex standard cells, which bring extra local M2

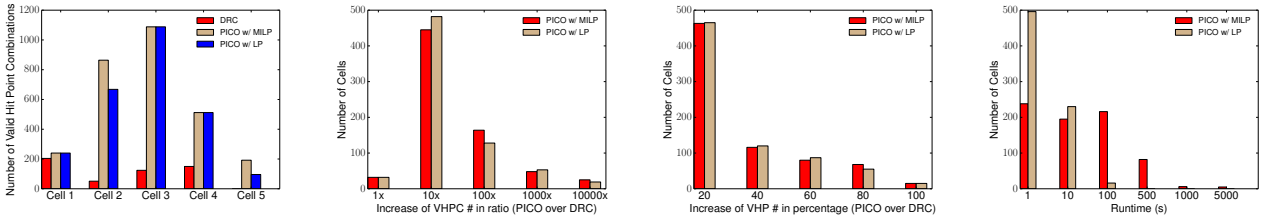
and via-1 blockages during detailed routing. It remains to be an open question on how to incorporate these local M2/via-1 routing congestion into the cell cost evaluation at the placement level. One future alternative will be to evaluate the cost aforementioned using the number of valid hit point combinations or valid hit points proposed in Section 3.

5. EXPERIMENTAL RESULTS

For the standard cell pin access, we have implemented PICO in C++ and tested it using ARM $10nm$ PTM library consisting of around 700 cells. CBC[33] is adopted as our LP and MILP solver and all experiments are performed on a Linux machine with a 3.33GHz Intel(R) CPU.[19] The technology parameter setup for the $10nm$ node can found in.[4,34] For the detailed routing, we have implemented different pin access planning schemes in C++ and tested them using OpenSparc T1 benchmarks as shown in Table 1. All benchmarks are synthesized using Synopsys Design Compiler[35] and placed using Cadence Encounter.[36] The Nangate $45nm$ library[37] is modified and scaled to represent the pin access scenario in $10nm$ node and beyond. The results of a state-of-the-art 2D SADP-aware detailed router, denoted as "DAC'14"[38] in Fig. 11, are generated for empirical comparisons. All experiments are performed on a Linux machine with 3.4GHz Intel(R) CPU and 32GB memory.[20]

5.1 Standard Cell Pin Access Optimization

For PICO, the standard cell pin access flexibility is quantified using the number of valid hit point combinations (VHPCs) and valid hit points (VHPs) for each standard cell. For a specific standard cell, a larger number of VHPCs and VHPs leads to more pin access flexibility during the detailed routing stage. Our pin access optimization engine (PICO) aims at maximizing the pin accessibility at the standard cell level. We compare different pin access evaluation/optimization schemes, including design rule check ("DRC"), "PICO + MILP" and "PICO + LP" in Fig. 10.[19] Among the cell-dependent results in Fig. 10(a), the "PICO + MILP" scheme consistently achieves the best performance, i.e. largest number of VHPCs. For "Cell 1", three schemes obtain similar number of VHPCs, which means the MPL constraints introduce slight degradations on the pin accessibility. However, the "DRC" scheme achieves zero VHPC for "Cell 5" while the "PICO + MILP" scheme recovers around 200 VHPCs. To evaluate the library-level benefits, we apply the PICO engine on each cell in the ARM $10nm$ PTM library and illustrate the improvement from PICO over DRC in Fig. 10(b) and Fig. 10(c). In Fig. 10(b), the improvement is calculated as the "increase of VHPC # in ratio", i.e. the number of VHPCs obtained from PICO divided by that obtained from DRC. The histogram in Fig. 10(b) demonstrates 10X or more improvement in terms of VHPCs for most standard cells. The increase in the number of VHPs is further calculated in percentage and plotted in Fig. 10(c), which shows that over 25% of the cells achieve 30% or more improvement for the ARM $10nm$ PTM library. In Fig. 10(b) and Fig. 10(c), we also find that the "PICO + MILP" scheme is better than the "PICO + LP" scheme in terms of solution qualities since more cells tend to achieve larger amount of increase in VHPCs and VHPs. The runtime for cells within the library is shown in Fig. 10(d) and the pin access optimization can be finished for most cells within 500s. Although the "PICO + MILP" scheme leads to longer runtime compared to the "PICO + LP" scheme, it is still affordable at the cell level as the PICO is a one-time computation task for a specific standard cell library.



(a) (b) (c) (d)

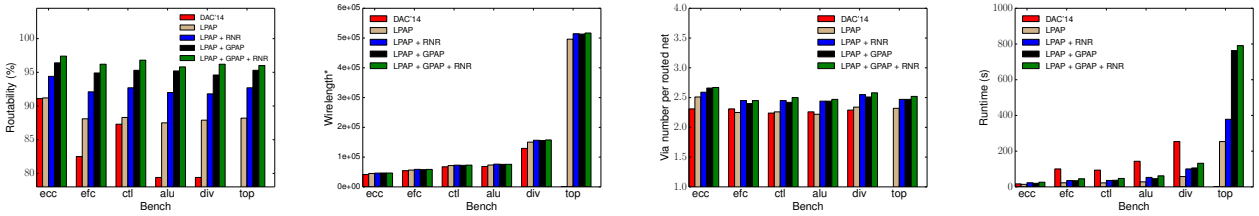
Figure 10. Standard cell pin accessibility improvement from PICO, (a) increase in number of VHPCs for different cells, (b) increase of VHPC # in ratio across the entire library, (c) increase of VHP # in percentage across the entire library.

5.2 Detailed Routing with Pin Access Planning

For the detailed routing stage, we compare the solution qualities of different routing schemes under SADP constraints, include a state-of-the-art 2D SADP-aware detailed router,[38] denoted as "DAC'14", and unidirectional routing with various combinations of pin access planning schemes among local pin access planning ("LPAP"), global pin access planning ("GPAP") and pin access driven rip-up and reroute ("RNR"). In our experiments, specific combinations include "LPAP", "LPAP + RNR", "LPAP + GPAP" and "LPAP + GPAP + RNR". Fig. 11 demonstrates the strength of proposed pin access planning schemes in terms of routability, wirelength, via count and runtime. "Routability" is defined as the number of routed nets over total number of nets in a design. Owing to the problem complexity, it is difficult to route all nets, i.e. achieve 100% routability, in an affordable amount of runtime. "wirelength*" is defined as the summation of routed wirelength of routed nets and half-parameter-wirelength (HPWL) of un-routed nets. "Via per net" is the average number of vias for each routed net. In general, better routing solutions should lead to larger routability, smaller amounts of wirelength, vias and runtime. In Fig. 11, the results for the "top" benchmark with the "DAC'14" scheme is not shown as the routing can not be finished within reasonable amount of runtime. As shown in Fig. 11(a), our proposed detailed routing with pin access planning achieves better routability compared to the "DAC'14" scheme is a consistent manner across different benchmarks. In particular, we obtain largest amount of routability improvement, around 10% on average, from the "LPAP + GPAP + RNR" scheme. To achieve the routability improvement, the trade-off is on the slight increases in "wirelength*" and "via per net" shown in Fig. 11(b) and Fig. 11(c), respectively. For schemes with lower routability, as the remaining nets are difficult to route, we expect that the "wirelength*" and "via per net" may increase significantly if similar routability could be obtained compared to the "LPAP + GPAP +RNR" scheme. The runtime comparisons in Fig. 11(d) further demonstrate that our unidirectional detailed router with pin access planning schemes achieves competitive even faster runtime compared to "DAC'14". Therefore, from Fig. 11, we conclude that unidirectional routing with pin access planning schemes can obtain better solution qualities compared to a state-of-the-art 2D detailed router while accommodating SADP-specific constraints.

Table 1. Benchmarks statistics

Ckt	ecc	efc	ctl	alu	div	top
Net#	1671	2219	2706	3108	5813	22201
Cell#	1302	1197	1725	1802	3260	12576
Size(um^2)	21 x 21	20 x 19	24 x 24	20 x 19	31 x 31	57 x 56

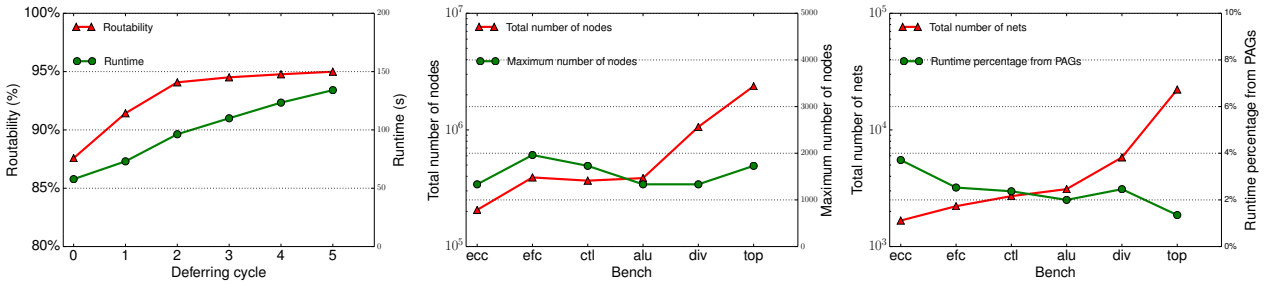


(a) (b) (c) (d)

Figure 11. Comparisons on solution qualities for various detailed routing schemes under SADP constraints, (a) routability, (b) wirelength*, (c) Via per routed net, (d) runtime.

Our proposed pin access planning schemes highly depend on the pin access graphs (PAGs) and the associated net deferring technique. Since the detailed routing itself is computationally expensive, it is worthwhile to validate that the pin access planning schemes lead to controllable amount of computational efforts. For the net deferring technique, a net may be deferred for several times to preserve the pin accessibility of remaining nets. The deferring cycle is defined as the maximum number of times that a net will be deferred during the detailed routing. Fig. 12(a) shows the trade-off between routability and runtime varying the deferring cycle for the benchmark "alu". In Fig. 12(a) the routability improvement saturates after certain deferring cycle while the runtime increases quasi-linearly as the deferring cycle increases. This means the deferring cycle should be set

to obtain maximum routability improvement within reasonable amount of runtime. In our experiments, the deferring cycle is set as 3 for the routability improvement. Fig. 12(b) and Fig. 12(c) further evaluate the cost of PAGs across different benchmarks. In Fig. 12(b), the "Total number of nodes" denotes the total number of nodes within the PAGs constructed for each benchmark and the "Maximum number of nodes" denotes the number of nodes of the largest independent component within the PAGs after the graph simplification stage. We can see from Fig. 12(c) that the maximum node size of each independent component within the PAGs is bounded by 2000 while the total number of nodes increases as the benchmark size increases. Since each update on the PAGs only works on a few components, this leads low computational cost to decide whether related standard cells are accessible during routing. In Fig. 12(c), the "Runtime percentage from PAGs" denotes the percentage of runtime from PAG updates over the total routing runtime. The runtime cost associated with the updates on the PAGs is bounded by 4% as the total number nets increases across different benchmarks as shown in Fig. 12(c). Therefore, Fig. 12 demonstrates that it is possible to control the computational cost of pin access planning schemes within an affordable level.



(a) (b) (c)

Figure 12. The computational efforts related to pin access graphs, (a) routability and runtime tradeoff varying the net deferring cost, (b) pin access graph size for benchmarks with different sizes, (c) the amount of runtime for updating pin access graphs during detailed routing.

6. CONCLUSION AND FUTURE DIRECTIONS

In this paper, we propose a holistic approach to address the pin access issue under advanced lithography constraints, from standard cell pin access optimization to placement and routing planning. Our pin access optimization engine (PICO)[4] can maximize the pin access flexibility and the pin access planning schemes[20] have obtained much better routing solution quality with 1D routing patterns compared to a state-of-the-art 2D SADP-aware detailed router.[38] In the future, we plan to focus on advanced placement mitigation techniques to reduce the pin access interference under advanced lithography constraints. At the same time, we find that the detailed routing stage is becoming more and more challenging in future technology nodes as most current detailed routing algorithms are sequential in nature. We plan to study paradigm-shifting concurrent routing algorithms to further improve the routing solution quality while accommodating advanced lithography constraints.

7. ACKNOWLEDGEMENT

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