O-Router: An Optical Routing Framework for Low Power On-chip Silicon Nano-Photonic Integration

Duo Ding, Yilin Zhang, Haiyu Huang, Ray T. Chen and David Z. Pan
ECE Dept. Univ. of Texas at Austin, Austin, TX 78712
{ ding, yzhang1, dpan }@cerc.utexas.edu, haiyu@mail.utexas.edu, chen@ece.utexas.edu

ABSTRACT

In this work, we present a new optical routing framework, *O-Router* for future low-power on-chip optical interconnect integration utilizing silicon compatible nano-photonic devices. We formulate the optical layer routing problem as the minimization of total on-chip optical modulator cost (laser power consumption) with Integer Linear Programming technique under various detection constraints. Key techniques for variable number reduction and routing speed-up are also explored and utilized. *O-Router* is tested on optical netlist benchmarks modified from top global nets of ISPD98/08 routing benchmarks. *O-Router* experimental results are compared with conventional minimum spanning tree algorithm, demonstrating an average of over 50% improvement in terms of total on-chip optical layer power reduction.

Categories and Subject Descriptors

B.7.2 [**Hardware, Integrated Circuit**]: Design Aids

General Terms

Algorithms, Design, Performance

Keywords

Optical Routing, Low Power Nanophotonic Integration, Integer Linear Programming

1. INTRODUCTION

As raised in the International Technology Roadmap for Semiconductors [8], silicon system complexity rockets exponentially due to increasing transistor counts, fueled by smaller feature sizes and increasing demands for higher integration / performances with lower costs. Consequently, interconnect design becomes more and more important for DSM VLSI as technology further scales down, among which on-chip optical interconnect is a potential quantum leap towards next-generation technology. Ever since its first introduction by Goodman in [5], the concept of on-chip optical interconnect has attracted more and more attention over the years in industry (e.g., [9, 15]) as well as academia (e.g., [3,12,14]), with major focus on device fabrication level. As analyzed and projected in [2], on-chip optical interconnect outperforms traditional copper interconnect in power, throughput and delay with apparent gain below 22nm technology node starting from 2016.

As one of the most promising device level break-through for on-chip optical integration, silicon compatible nano photonic devices (e.g., [11, 15]) take advantage of optical properties of a signal, characterizing great resilience in terms of small delay, low power and high throughput when compared with traditional copper interconnection. Advances in device level improvements of silicon nano photonics (such as photonic crystal structures in [7,16]) have also been demonstrated. In recent years, low RF power optical modulators operating at a few Gbps speed have been successfully demonstrated [6,7], with compact footprint for potential large scale on-chip integration. Compact photodetecters with up to 50Gbps processing rate have also been demonstrated (such as Germanium-on-Insulator photodetecter in [10]). With a proper collection of current Silicon nano-photonic devices and some extended projections / assumptions based on [2,8], there can be exciting CAD synthesis explorations in interconnect planning for optical on-chip integration.

As a related work, [13] studied timing driven and congestion driven on-chip optical routing CAD algorithms under 3-D system-on-package scenario. Yet the routing geometry in [13] was formulated in a very simple manner: point-to-point straight connection, which also means there is at least 1 optical modulator inserted at each pin and Steiner point in the netlist. There are 3 major issues with such an approach: *First*, it neglects the laser power consumption of optical modulators. Since each modulator requires a laser source for electrical-to-optical data conversion, this approach results in a very power consuming chip; *Second*, it neglects the photon-energy loss constraint on optical interconnect; consequently, there could be pins whose received photon-energy drop below the photo-detectors' detection threshold, leading to inevitable malfunction after optical-to-electrical data conver-

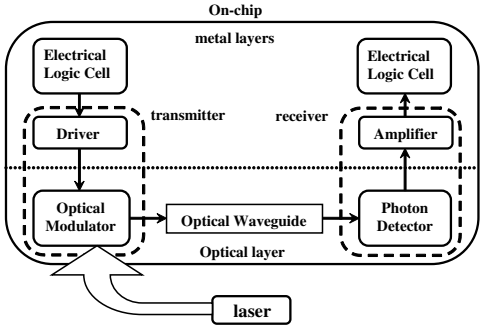

Figure 1: Block diagram for electrical/optical and optical/electrical data conversions

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sion. *Third*, optical routing has very different characteristics compared with conventional electrical (copper) interconnect routing, therefore, special routing geometry must be developed to tackle optical interconnect planning problems. In other words, total laser power consumption (proportional to number of modulators inserted) and the constraints for successful optical-to-electrical detection must both be addressed properly for optimized optical routing geometry.

In this work, we present *O-Router*, an optical routing framework that takes into consideration of various constraints and flexibilities that silicon nano-photonics device libraries and optical waveguide models shall impose on the future on-chip optical interconnect. *O-Router* is driven by low power on-chip silicon nano-photonic integration.

The rest of the paper is organized as follows: Section 2 introduces some preliminaries regarding optical and electrical data conversions and silicon photonics, followed by a motivational example and a summary list of key contributions of this paper. Section 3 describes our *Optical Interconnect Library* built for *O-Router*; Section 4 focuses on the optical routing Integer Linear Programming (ILP) problem formulation and speed-up techniques, followed by experimental results in Section 5. Section 6 concludes the paper by a brief summary and some potential future work.

2. PRELIMINARIES AND MOTIVATION

As shown in Fig. 1, on the transmitter's side, the electric signal from the driver (electrical layer) amplitude modulates the light source from the laser inside an optical modulator, and then send the modulated optical signal onto optical interconnect (optical waveguide on optical layer); on the receiver end, a photo-detector detects the photons from the waveguide and converts it into electric signal (back to electrical layer); an amplifier may be needed if this signal drives a high fan-out net on electric layers.

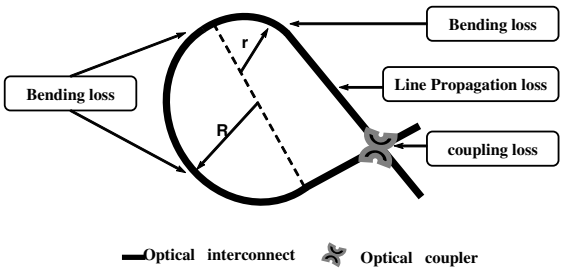

Figure 2: Sources of loss for on-chip optical routing

2.1 Optical Waveguide Routing

As aforementioned, optical routing has unique characteristics when compared with traditional copper routing. Manhattan (X/Y) routing based algorithms are not favored on optical layer because of the huge amount of loss caused by the sharp wire turnings along the data path, unless some special structures be inserted; yet these structures are usually costly in fabrication and/or bulky in footprint size, etc.

O-Router performs gridless optical routing with waveguide couplings/crossings on a single layer. As a result, routing geometry becomes very flexible, with different geometries and penalties according to their respective optical interconnect loss. In order to further explore optical routing geometry, we define the following 3 types of losses (with dB unit) on an optical interconnect path in equations 1- 5.

$$L_{loss} = \alpha \cdot length_{path} \quad (1)$$

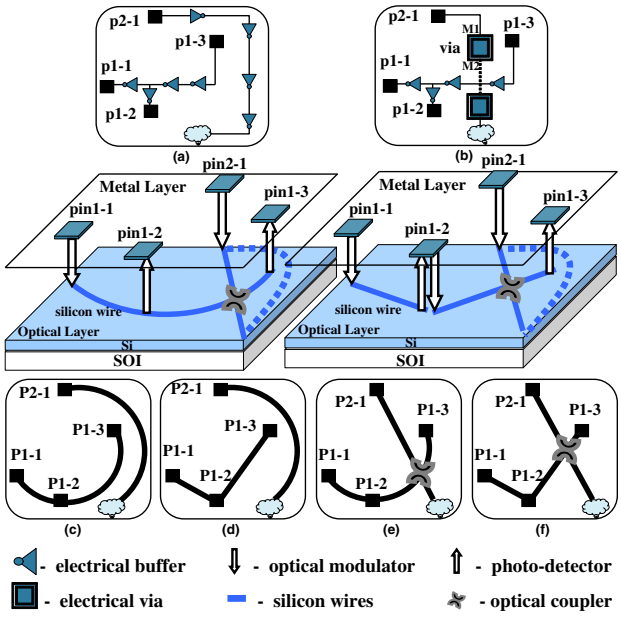

Figure 3: Motivational example for electrical routing v.s optical routing

$$B_{loss} = \beta \cdot \theta \cdot r^{-\eta} \quad (2)$$

$$C_{loss} = \gamma \cdot Num_{couplers} \quad (3)$$

$$P_{loss} = L_{loss} + B_{loss} \quad (4)$$

$$Total_{loss} = P_{loss} + C_{loss} \quad (5)$$

As shown in Fig. 2, L_{loss} is straight line waveguide loss, it is proportional to the length of optical interconnect, with a coefficient α; B_{loss} is the bending loss, since waveguide cross-section width is negligible compared to the bending radius in *O-Router*, we assume B_{loss} to be proportional to the degree of the optical interconnect (silicon waveguide) arc angle θ, and inversely proportional to the radius r of the interconnect, with an index η; C_{loss} is the coupling loss, proportional to the number of couplers (crossings) on the interconnect, with a coefficient γ. All related coefficients are determined by our *Optical Interconnect Library*, which is built for *O-Router* and will be explained further in Section 3.

2.2 Motivational Example

In this section, we briefly explore the different trade-offs for optical routing. As shown in Figure. 3, there are 2 nets to be routed on a chip, noted as *pini-j*, meaning it is the *jth* member of net *i*; Fig. 3(a) and (b) shows two alternatives for conventional routing on electrical layer with buffers and/or metal via inserted to alleviate the timing penalty caused by the long wires across the chip. Buffers are inserted since RC delay increases quadratically with electrical wire length. Yet buffer insertion is not all-powerful technique. Generally speaking, cross-chip timing critical nets are tough to fix thus impose great difficulty to VLSI design timing closure. As technology further scales down and system integration level rockets, issues with electrical interconnect will get more severe.

Fig. 3(c)-(f) show 4 possible routing geometries for the 2 nets on optical layer, according to our optical routing. Routing geometry (c) requires a total of 2 optical modulators: 1 inserted at P1-1, 1 inserted at P2-1, while for (d), 1 extra modulator will be inserted at P1-2, in order to drive P1-3, since sharp turning at P1-2 is either too lossy or too

costly to fix other than using an extra modulator. In (e) and (f), optical coupler is introduced for coupling optical signal across 2 wires, with certain amount of loss. In these 2 cases, couplers can be employed either because doing so results in less amount of loss than taking detours as in (c) and (d), or because taking detours results in more coupling loss with other nets on chip, etc.

We can learn that geometries (c)(e) result in least among of modulating power among (c)-(f), yet optical interconnect bending loss: B_{loss} is also introduced, as well as the coupling loss: C_{loss} (in (e)) so that the constraint for successful detection at P1-3 may be violated due to too much loss on interconnect. To optimally pick the best routing geometry from the (c)-(f) 4 cases is the motivation of *O-Router*.

O-Router targets at finding optimal optical routing geometry to minimize total modulating power, subject to various constraints imposed by the device characterizations.

2.3 Main Contributions of This Paper

Main novelty and contributions of *O-Router* are as follows:

- Based on extensive data collection and road-mapping, we project the technology trends of on-chip silicon nano-photoincs and build *OIL*: an *Optical Interconnect Library* characterized for low-power on-chip integration/synthesis.
- For the first time, we formulate the optical routing problem by taking into considerations of various detection constraints and flexibilities that *OIL* imposes on the future optical interconnect.
- Under gridless single layer optical routing with couplings/crossings, the solution space is theoretically infinite. To reduce solution space without losing optimality, we put a set of constraints on the waveguide routing rules and formulate the optical routing problem with Integer Linear Programming.
- We also propose several key techniques to speed-up the optical routing framework under ILP formulation.

3. OPTICAL INTERCONNECT LIBRARY

To support our *O-Router* framework, we first build an Optical Interconnect Library (OIL), which includes a Mach-Zehnder optical modulator [6], a photo-detector from [10], a fully simulated optical coupler using Rsoft [1], and a set of optical interconnect (silicon waveguide) model. For details regarding OIL, please refer to [4].

3.1 Optical Modulator and Photo-detector

Based on some related research (e.g., [2,8,12]), we project current OIL parameters towards next generation technology, which essentially enables better on-chip integration for nanophotonic devices.

In Table 1, there are 2 sizes of modulators included, one is a normal modulator; the other is ModulatorX: a large modulator with 10X driving power, which will be inserted into a net that suffers greatly from power losses in order to guarantee successful detection. Since the power consumption of ModulatorX is much larger than normal modulator, its usage will be penalized with a constant coefficient $MPow_{penalty}$, details in Section 4.

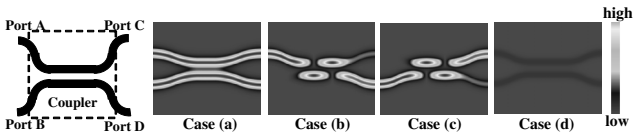

Figure 4: Working mechanism of optical coupler in *O-Router*

Table 1: Major OIL components with high level parameters.

	throughput	length	width	driving power	loss
modul1	>10Gps	<50um	<10um	1X	-
modulX	>10Gps	<50um	<50um	10X	-
detector	>10Gps	<10um	<10um	-	-
coupler	>10Gps	<50um	<5um	-	<10%

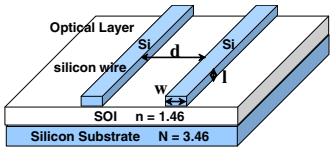

Figure 5: OIL on-chip optical waveguide model

3.2 Optical Coupler and Interconnect Model

The working principle of optical coupler is shown by Fig. 4. There are 4 ports from A to D for each coupler, and the parallel double interconnect region is the arm region. Optical signals will be cross coupled in the arm region. From the 4 simulation cases, we can verify that PortA=PortD and PortB=PortC always satisfy, as if there is wire connection between A-D and B-C. Optical couplers allow us to make full use of the optical layer routing space, making non-planar netlists routable on a single silicon layer. In case (b)(c) in Fig. 4, there is slight loss for high optical logic after the coupler, as is formulated by C_{loss}.

As shown in Fig. 5, the optical waveguide model included in OIL has a reflective index of 3.46, coated on top of a $2um$ thick SOI layer (reflective index < 1.46). The cross-section width of the silicon wire w=$0.5um$, cross-section height l=$0.22um$, wire spacing d between $0.5um$ and $3.0um$. d should be set properly to avoid wire cross-talk.

4. O-ROUTER FORMULATION AND ALGORITHM

Given the pin locations of certain placed netlist for optical routing, *O-Router* seeks optimal routing solution with Integer Linear Programming to minimize total modulating power, meanwhile satisfying various detection constraints according to established OIL parameters. This section is divided into three parts: First is the optical netlist mapping. This is when suitable optical netlist benchmarks for *O-Router* are constructed. Second part is the core ILP formulation, followed by routing speed-up techniques in the third part.

4.1 Optical Netlist Mapping

Given an electrical layer netlist after placement, the goal of this step is to prepare an optical netlist that makes most use of optical layer resource to fix top timing critical nets (i.e., longest) in electrical layer. For our ILP formulation, the resulting optical netlist of this stage consists of only 2, 3 and 4 pin nets. It takes place in 3 phases:

Phase 1: Pre-select top timing critical nets from electrical layer to map onto optical layer. Shown in Fig. 6(a)(b), non-timing critical nets 1/2/3 are not selected.

Phase 2: Cluster within each pre-selected net for routing

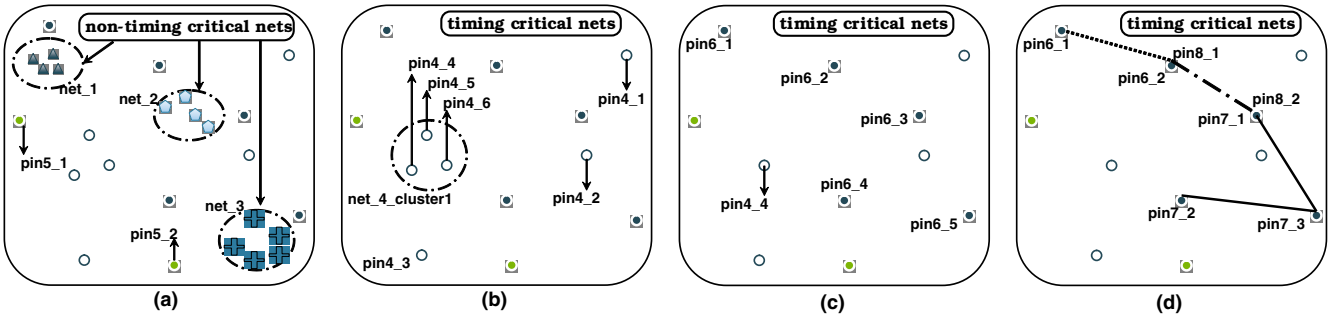

Figure 6: Illustrations for *optical netlist mapping*

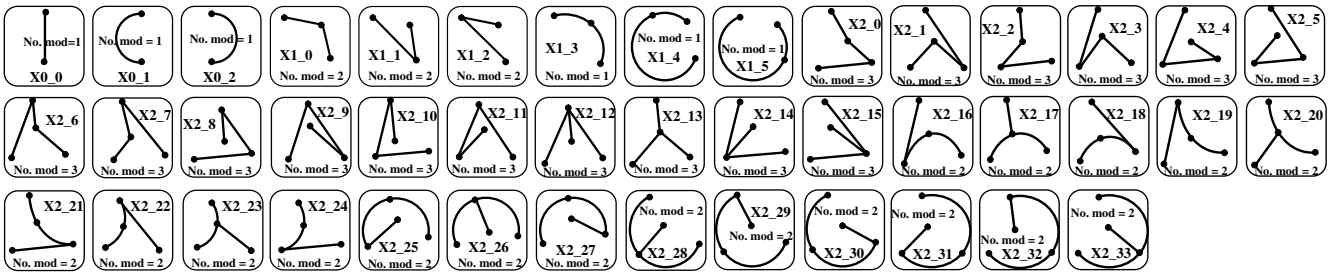

Figure 7: A list of optical routing geometries (represented by integer variables) for 2, 3 and 4 pin nets

efficiency enhancement. Since optical routing is most effective dealing with global interconnect, we map a single pin from each local pin cluster onto the optical layer and leave the remaining pins to electrical layer.

As shown from Fig. 6(b) to Fig. 6(c), the *net_4_cluster1* is represented by *pin4_4* on optical layer. With this phase, the pin number for each optical net becomes very small. For *O-Router*, we manage to keep each optical net size to below 5 pins. Practically, nets with more than 4 pins can be decomposed into a set of 2/3/4 pin nets, as illustrated in (c)-(d), where a 5-pin net6 is decomposed into two 2-pin nets and a 3-pin net.

Phase 3: For intersected 2-pin nets in the netlist from Phase2, expand them to have 2 more integer variables if and only if they can avoid crossing each other by taking an arc detour, meanwhile the detour does not cut a third net. This step further expands the feasible solution space for 2-pin nets.

4.2 Integer Linear Programming Formulation

For the original ILP formulation, we enumerate all routing geometries for the 2-pin, 3-pin and 4-pin nets, shown in Fig. 7(a concave shape 4-pin net is shown as an example). Each X_{ij} is an integer variable, where $i \in$ *net_space*, $j \in$ *sol_space(net i)*. When $X_{ij} = 1$, the corresponding routing geometry from Fig. 7 will be adopted, as part of the final routing solution space. Number of modulators in each X_{ij} is also recorded; OIL will return the actual modulating power based on this number and the ij index.

The ILP formulation is as follows in Equation 6- 15, with all terms and variables explained in Table 2. The objective function is the total power required to drive all the on-chip optical modulators for our optical interconnect framework. The ILP solver will minimize the objective function, subject to constraints imposed from Eq. 7 to Eq. 15. In Eq. 6, the first term $MPow_{Xij}$ is total modulating power consumption for routing geometry X_{ij} using 1X modulators, while the second term $(MPow_{penalty} - P_0) \cdot M_{ij} \cdot N_{ij}$ is for penalizing the usage of 10X driving power ModulatorX: if M_{ij} is 1(hard constraint violation), then ModulatorX will be used to replace all Modulator1's in geometry X_{ij} to meet the constraint (P_0 is the laser power consumption of Modulator1).

$$min\{\sum_{i \in net\_space()}^{j \in sol\_space(i)} [MPow_{Xij} \cdot X_{ij} + (MPow_{penalty} - P_0) \cdot M_{ij} \cdot N_{ij}]\}$$
$$s.t \quad (6)$$
$$\forall i, m \in net\_space, i \neq m, j \in sol\_space(i), n \in sol\_space(m):$$

$$P_{loss_{Xij}} \cdot X_{ij} + net_{loss_{Xij}} \leq loss\_th_{Xij} + pow \cdot N_{ij} \cdot M_{ij} \quad (7)$$
$$P_{loss_{Xij}} = L_{loss_{Xij}} + B_{loss_{Xij}} \quad (8)$$
$$net\_loss_{Xij} = \sum_{m \in net\_space}^{n \in sol\_space(m)} C_{loss_{Xij\_mn}} \cdot X_{ij\_mn} \quad (9)$$
$$C_{loss_{Xij\_mn}} = \gamma_{ij\_mn} \cdot cross\_num < X_{ij}, X_{mn} > \quad (10)$$
$$X_{ij} + X_{mn} \leq 1 + X_{ij\_mn} \quad (11)$$
$$(1 - X_{ij}) + (1 - X_{mn}) \leq 2 - X_{ij\_mn} \quad (12)$$
$$\sum_{j \in sol\_space(i)} X_{ij} = 1, \quad X_{ij} = 0, 1 \quad (13)$$
$$X_{ij\_mn} = 0,\ 1 \quad (14)$$
$$M_{ij} = 0,\ 1 \quad (15)$$

Constraint Eq. 7 is set for each routing geometry X_{ij}, such that its total loss (propagation loss P_{loss} and coupling loss C_{loss}) is bounded by an upper bound of loss threshold: $loss\_th_{xij}$, once the upper bound of loss is exceeded, it means the photo-detection requirements in routing geometry X_{ij} are violated. If among all feasible X_{ij}, some of such constraint is inevitably violated, then ModulatorX will be inserted into the corresponding geometry X_{ij} and replace existing 1X modulators. Constraint Eq. 10 explicitly maps the crossing number of a net into corresponding coupling loss using OIL.

For ILP formulation of the calculation of optical interconnect coupling number, we introduced the cross-term integer

Algorithm 1 **ILP based Optical Routing for low power chip**

Require: mapped optical netlist benchmark
  invoke optical netlist parser; **link** OIL
  while $i \in net\_space$ **do**
    while $j \in sol\_space(i)$ **do**
      calculate ($L_{loss_{Xij}}$,$B_{loss_{Xij}}$,$MPow_{Xij}$,$MPow_{penalty}$,etc.)
      while $m \in net\_space, m \neq i$ **do**
        while $n \in sol\_space(m)$ **do**
          calculate ($C_{loss_{Xij\_mn}}$, constraint coefficients,etc.)
        end while
      end while
    end while
  end while
  generate glpk syntax file; **invoke** glpk ILP solver – minimize
  return optical routing for minimum modulating power

Algorithm 2 **ILP variable number reduction via trimming**

Require: mapped optical netlist benchmark
  while $i \in net\_space$ **do**
    while $j \in sol\_space(i)$ **do**
      calculate ($L_{loss_{Xij}}$,$B_{loss_{Xij}}$)
      if $L_{loss_{Xij}} + B_{loss_{Xij}} \geq threshold_{Xij}$ **then**
        exclude X_{ij}; update data structures
      end if
    end while
  end while
  return trimmed set of routing geometries for each net

Algorithm 3 **ILP cross-term variable reduction via merging**

Require: mapped optical netlist benchmark
  while $i \in net\_space$ **do**
    while $j \in sol\_space(i)$ **do**
      while $m \in net\_space, m \neq i$ **do**
        while $n \in sol\_space(m)$ **do**
          if $i > m$ **then**
            swap (i,j) with (m,n) in X_{ij_mn}; **calculate** cross-term constraint coefficients; **update** glpk syntax file
          end if
        end while
      end while
    end while
  end while
  return reduced set of cross-terms

Algorithm 4 **bounding box for C_{loss} computation speed-up**

Require: mapped optical netlist benchmark
  generate $bounding\_box\_matrix[\,][\,]$
  while $i \in net\_space$ **do**
    while $m \in net\_space, m \neq i$ **do**
      if $bounding\_box\_matrix[i,m] == 1$ **then**
        calculate $C_{loss_{ij\_mn}}$; update glpk syntax file
      end if
    end while
  end while
  return optical routing for minimum modulating power

variables: X_{ij_mn}. Numerically, it is the product of term X_{ij} and X_{mn}. Since variable multiplications are not supported by ILP solver, we add the constraint pair Eq. 11- Eq. 12. Integer constraints Eq. 11 and Eq. 12 bound the X_{ij_mn} term so that it always equals the product of its two corresponding routing geometries. Equality constraint Eq. 13 makes sure that the ILP solver eventually picks only 1 routing geometry out of each net for the final optimal solution. For further details please see Table 2 and Algorithm 1.

Table 2: **Descriptions for ILP involved terms and variables.**

Name	Description
$net\_space()$	set of nets for an optical netlist
$sol\_space(i)$	set of possible routing geometries for net i
$MPow_{Xij}$	total modulator power consumption of routing geometry X_{ij}
$MPow_{penalty}$	power consumption penalty for using each ModulatorX. Set to 10 times of P_0
P_0	power consumption of Modulator1
N_{ij}	least number of optical modulators used for geometry X_{ij}
$C_{loss_{Xij}}$	coupling loss power between routing geometry X_{ij} and X_{mn}
$P_{loss_{Xij}}$	propagation loss power on silicon wires of X_{ij}
X_{ij}	integer variable. $X_{ij} = 1$ means to accept the jth routing geometry of net i
M_{ij}	integer variable. $M_{ij} = 1$ means to insert modulatorX into jth routing geometry of net i
X_{ij_mn}	integer variable. numerically equals to $X_{ij} \cdot X_{mn}$
$loss\_th_{Xij}$	loss threshold for O-E conversion for X_{ij}
pow	more driving power each ModulatorX brings than Modulator1
γ_{ij_mn}	coupling loss coefficient returned by OIL dependent on geometry X_{ij} and X_{mn}

4.3 Variable Reduction and Speed-up Techniques

Apparently, a direct implementation of Algorithm 1 will result in very large number of variables as well as tremendous among of computations, especially for large optical netlists. Here we propose some useful techniques to speed-up *O-Router*.

4.3.1 Variable Trimming/Merging

Variable trimming procedure first scans through the X_{ij} list and calculate bending loss B_{loss} and line propagation loss L_{loss} for each X_{ij}. If the loss of X_{ij} itself becomes unbearable, then such a routing geometry is dumped before invoking ILP. Variable trimming procedure successfully trims off the infeasible integer variables in Fig. 7 and greatly reduces the variable set. Solution optimality will not be harmed with careful choice of the *threshold* value. Details about this procedure are shown Algorithm 2.

Variable merging procedure runs in parallel with *variable trimming procedure*. As described in Algorithm 3, it cuts the cross-variable set to half of original size, and the idea is amazingly simple:

$$X_{ij} \cdot X_{mn} = X_{ij\_mn} \tag{16}$$

$$X_{mn} \cdot X_{ij} = X_{mn\_ij} \tag{17}$$

$$X_{ij\_mn} = X_{mn\_ij} \tag{18}$$

Essentially, X_{ij} and X_{mn} generate non-zero constraint coefficients only when both of them are adopted, which means the product equality holds in Eq. 16 and 17, consequently, Eq. 18 also holds, so we can rename half of the cross-term variables to the other half, since they are identical. Details about this procedure are shown in Algorithm 3.

4.3.2 Bounding Box Elimination for Speed-up

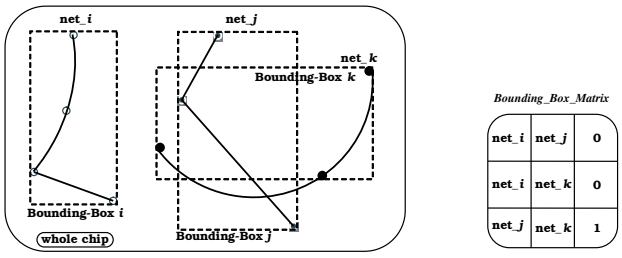

Figure 8: **Illustration of Bounding Box Elimination**

Table 3: Performance comparisons between *O-Router* and Minimum Spanning Tree algorithm.

	photo-detection threshold : 55%				photo-detection threshold: 75%			
	ibm01	ibm02	ibm03	ibm04	ibm01	ibm02	ibm03	ibm04
Net number	5	20	50	137	5	20	50	137
Pin number	15	50	155	391	15	50	155	391
Pin/net ratio	3	2.5	3.1	2.85	3	2.5	3.1	2.85
MST-routing (normalized power)	3.5	6	35.66	305.13	3.5	12.75	39	306.25
O-Router (normalized power)	1	2.88	10.75	57.75	2.13	5.38	16.5	100.25
Improvement	71.40%	52.00%	69.90%	81.10%	39.10%	57.80%	57.70%	67.30%

The introduction of Bounding Box contributes to computation speed-up of O-Router. *Bounding Box* of net i is defined as the rectangle that bounds all the pins of net i. It is defined by 4 values as in Eq. 19:

$$Bounding\_Box_i = (min(X), max(X), min(Y), max(Y)) \quad (19)$$

$$where \quad X \in x\_axis\{net_i\}, \quad Y \in y\_axis\{net_i\} \quad (20)$$

As illustrated in Fig. 8, a *Bounding_Box_Matrix* will be generated in pre-scanning stage; for any pair of nets with non-overlapping bounding boxes, a 0 is recorded, otherwise, 1 is written; In Fig. 8, *net_j* and *net_k* have potential crossings, thus only them will be processed for constructing coupling loss constraints. This procedure worth the efforts because a general algorithm for calculating C_{loss} is much more complicated than min/max value search. Further details for bounding box elimination procedure are shown in Algorithm 4.

With all 3 speed-up procedures, the original ILP formulation in Section 4.2 is modified, implemented and tested.

5. EXPERIMENTAL RESULTS

Simulations are carried out according to the aforementioned 3 steps in Section 4, and original electrical benchmarks come from ISPD98/08 routing benchmarks. ibm01-04 are the final 4 optical netlists benchmarks, listed as in Table 3. Due to considerations of silicon wire spacing/low coupling noise communication, the sizes of the optical netlists are kept from small to medium, and the optical layer pin density is kept from low to medium. As a baseline for *O-Router*, Minimum Spanning Tree (MST) routing algorithm is implemented on ibm01-04. Both *O-Router* framework and MST algorithm are repeated on ibm01-04 for 2 different photo-detection threshold values: 55% and 75%. Such percentages signify the photo-detection power threshold for received signals at the end of optical interconnect. Therefore, 75% threshold photo-detectors impose stricter detection requirements on *O-Router* framework. In Table 3, the simulated power consumptions are normalized by the amount of power reported by *O-Router* on ibm01, under photo-detection threshold of 55%. For 55% threshold, *O-Router* achieves above 50% of power reduction compared to MST baseline, with a max of 81.1% on ibm04. For the 75% threshold, *O-Router* reports slightly less power reductions due to higher detection requirements; still an average of above 50% reduction, with a max of 67.3% of power reduction on ibm04.

6. CONCLUSION

In this paper, we present the first optical routing framework, *O-Router* for low power on-chip integration of silicon nano-photonics with consideration of various detection constraints. Based on ILP formulation with several variable reduction techniques for routing speed-ups, *O-Router* utilizes Optical Interconnect Library, which is an established collection of some silicon compatible on-chip nano-photonics devices and optical interconnect models, with key parameters projected for future technologies based on optical interconnect roadmap. Experimental results show promising improvements compared with traditional Minimum Spanning Tree routing algorithm. We expect to see a lot of future works along this direction as new nano-photonics devices are introduced for the ultimate global optical and electrical interconnect co-synthesis and planning.

7. ACKNOWLEDGMENT

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