

# ELIAD: Efficient Lithography Aware Detailed Router with Compact Post-OPC Printability Prediction

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## ABSTRACT

In this paper, we present ELIAD, an efficient lithography aware detailed router to optimize silicon image after optical proximity correction (OPC) in a correct-by-construction manner. We first propose a compact post-OPC litho-metric for a detailed router based on statistical characterization. We characterize the interferences among weak grids filled with one of predefined litho-prone shapes (e.g., jog-corner, via, line-end). Our litho-metric derived from the characterization shows high fidelity to total edge placement error (EPE) in large scale, compared with Calibre-OPC/ORC. As a chip itself is in the largest scale, ELIAD powered by the proposed metric can enhance the overall post-OPC printed silicon image. Experimental results on 65nm industrial circuits show that ELIAD outperforms a ripup/rerouting approach such as RADAR [17] with 8x more EPE hotspot reduction and 12x speedup. Also, compared with a conventional detailed router, ELIAD is only about 50% slower.

## Categories and Subject Descriptors

B.7.2 [Hardware, Integrated Circuit]: Design Aids

## General Terms

Algorithms, Design, Performance

## Keywords

VLSI, Routing, Lithography, OPC, Manufacturability

## 1. INTRODUCTION

Nanometer VLSI design is facing increasing challenges from manufacturing limitations. These include the printability issues due to sub-wavelength lithography [2, 11, 13, 17, 21], the topography variations due to chemical-mechanical polishing (CMP) [3, 6, 8, 20], the random defects due to missing/extra material [4, 14, 18], the via failure [1, 15, 22], and

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so on. Thus, we need to ensure not only conventional design closure but also manufacturing closure in nanometer regime. As it has been shown that manufacturing issues are strongly layout-dependent, manufacturability aware layout optimization for manufacturing closure shall play a key role in the overall yield improvement.

Regarding multiple manufacturing issues, lithography with 193nm wavelength is one of the most fundamental challenges due to its impact on yield and timing, and expected to be more serious in more advanced technologies. Even worse, next generation lithographies are not likely to be in the mainstream in the near future [16]. Accordingly, major IC manufacturers still use 193nm lithography to print 65, 45, 32nm and below, heavily relying on resolution enhancement techniques such as optical proximity correction (OPC).

OPC which modifies GDSII for better printability as a post-tapeout mask synthesis is a crucial step in manufacturing, but at a cost of high computational complexity as well as mask cost overhead. Nevertheless, OPC may be too late to make all the necessary corrections due to restricted design flexibility. These drawbacks of OPC put lithography aware design (as a part of design for manufacturability (DFM)) in greater demand than ever so that the downstream lithography and OPC effects can be abstracted and estimated for better design decisions in terms of manufacturability and manufacturing cost.

As a result, there are many manufacturability aware efforts in earlier design stages such as logic synthesis and placement [7, 10], but routing is often believed to be one of the most important stages to address the lithography issue due to the following reasons [11, 17]: **(a)** wire printability is coupled with interconnection network which is mainly determined by routing, **(b)** routing is the last major VLSI physical design step before manufacturing, thus has more comprehensive and accurate information on lithography, **(c)** routing still has considerable design flexibility to find reasonable tradeoff between printability and conventional design objectives (e.g., timing, noise, power). These factors lead to a lot of recent academic and industrial efforts in *lithography aware routing*, especially detailed routing due to small influence window of optical lithography.

One easy approach for lithography aware routing would be to introduce manufacturability aware rules, but such rule-based approach suffers from exploding number of rules, expensive rule-checking, and more importantly large area/timing overhead due to over guard-band. This downside leads to several model-based approaches. The first OPC aware maze routing is proposed in [11] based on multi-constrained short-

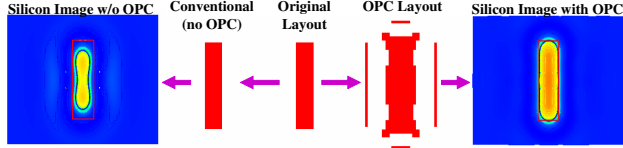


Figure 1: OPC example [11].

est path optimization by subgradient method. A multilevel routing approach to minimize the number of OPC features is studied in [2]. As a post-optimization, ripup/rerouting to remove litho-hotspots is proposed based on fast lithography simulation [17] or pattern matching [13]. However, there are a few drawbacks in these prior works: (a) printed or silicon image is not directly addressed [2, 11], (b) the result is not verified with an industrial sign-off tool under inevitable defocus [2, 11, 17], (c) the burden of trivial litho-hotspots which can be easily fixed by OPC is imposed on router by ignoring OPC [17], (d) post-optimization inherently cannot make radical changes enough to address lithography issue [13, 17].

In this paper, we propose ELIAD, an efficient lithography aware detailed router based on a compact and high fidelity post-OPC litho-metric. Our litho-metric shows high correlation ( $>0.95$ ) to total EPE computed by Calibre-OPC/ORC in large scale. We plug this metric into ELIAD using Lagrangian relaxation. The major contributions of this paper include the following.

- We propose a compact and high fidelity litho-metric with OPC taken into account. Our metric is from statistical weak grid characterization which has several advantages over pattern characterization.
- We present an efficient lithography aware detailed router, ELIAD to optimize post-OPC silicon image. In our formulation, we adopt the proposed litho-metric in ELIAD based on Lagrangian relaxation technique.
- We propose a technique for fast convergence of subgradient optimization using weak grid shadowing around blockages and routed nets
- ELIAD is the first lithography aware detailed router targeting post-OPC image in a correct-by-construction fashion. Routing results are verified with an industrial optical rule check (ORC) under a realistic OPC recipe.

The rest of the paper is organized as follows. Section 2 provides preliminaries on lithography. Our litho-metric is described in Section 3. Section 4 proposes ELIAD. Experimental results are discussed in Section 5, followed by conclusion in Section 6.

## 2. PRELIMINARIES

To fill up the gap between rapidly shrinking feature size and optical wavelength, several resolution enhancement techniques (RETs) are applied in advanced technologies such as optical proximity correction (OPC), phase mask shifting (PSM), off-axis illumination (OAI), and so on. Among them, OPC is one of the most widely used RETs which modifies layout patterns to improve printability [19]. Fig. 1 shows an example of OPC by contrasting silicon images with OPC and without OPC. Since OPC is not optional in 90nm and below, it is essential to consider in any lithography

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### Algorithm 1 Statistical WGT Characterization

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**Require:** A set of WGT  $T$ , a max distance  $d$

```

1: Table WGT_TABLE  $\leftarrow \emptyset$ 
2: for each type  $t1 \in T$  do
3:   for each type  $t2 \in T$  do
4:     for  $i = 1$  to  $d$  do
5:        $P =$  a set of patterns which have one  $t1$  and one
            $t2$  with the distance  $= i$ 
6:        $sum = 0$ 
7:       for each pattern  $p \in P$  do
8:         lithography simulation of  $p$  after OPC
9:         for each EPE hotspot  $h \in p$  and  $\geq$  noise do
10:           $sum +=$  EPE of  $h$ 
11:        end for
12:      end for
13:      WGT_TABLE( $t1, t2, i$ )  $= \frac{sum}{|P|}$ 
14:    end for
15:  end for
16: end for
17: return WGT_TABLE

```

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aware design optimization the limitations of OPC (whether a hotspot can or cannot be fixed by OPC) [23, 24].

In optical lithography, EPE is measured as the difference between a target contour and a printed contour. EPE is a popular concept to adjust the polygon edge during OPC, and can be used to measure the quality of layout in terms of printability [17]. Accordingly, a litho-hotspot can be defined as a spot where EPE is larger than a given critical dimension (CD) tolerance, and detected by optical rule check (ORC).

## 3. POST-OPC PRINTABILITY PREDICTION

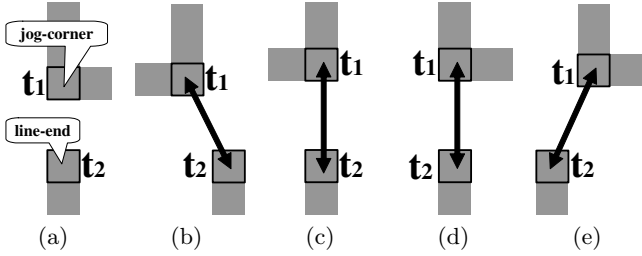
In this section, we present our litho-metric to predict post-OPC printability during detailed routing. The focus of our metric is to estimate the impact of a routing decision on *global* (large scale) printability in faster time, so that it can be plugged in as a part of a detailed router. We intend to neither compute the exact EPE of a certain spot nor identify litho-hotspots accurately. We are mainly interested in guiding a router to generate more litho-friendly layout by capturing global *trend* at small cost. In this aspect, our metric is different from another fast hotspot detection using graph in [12], and more suitable for a detailed router.

The motivation behind OPC consideration in our metric is that a pattern which is believed to be *litho-unfriendly* can be printed successfully depending on OPC algorithm and recipe. Considering OPC as an essential step, a litho-metric or fast lithography simulation [17, 24] without OPC can burden a detailed router unnecessarily by blindly optimizing some easy-to-fix-by-OPC litho-hotspots.

In Section 3.2, we propose our litho-metric using the statistical weak grid type (WGT) characterization in Section 3.1. Section 3.3 shows the high fidelity of our metric.

### 3.1 Statistical WGT Characterization

In industry, pattern matching has been done to identify litho-unfriendly patterns, so that it can be used in post-optimization for litho-hotspot removal. Also, it can yield very accurate hotspot detection even in fine scale, if a pattern library is comprehensive enough. However, pattern matching is inefficient in guiding a detailed router in a correct-



**Figure 2:** WGT characterization for  $t_1$ =jog-corner and  $t_2$ =line-end is shown where (b), (c), (d), and (e) are the cases with the same distance. Thus, the mean EPE will characterize this interaction between  $t_1$  and  $t_2$  at this distance.

by-construction manner for the following reasons.

**Runtime** Pattern matching is computationally too expensive to be used in a detailed router even with the latest algorithm [23, 24], as detail routing is already one of the slowest steps in VLSI design.

**Memory** Depending on technology, the number of patterns we need to store can explode. Therefore, it may consume too large memory for an already-memory-hungry detailed router.

**Update** Whenever there is a change in either process technology or OPC recipe, the characterization needs to be redone to reflect the latest fab condition. However, pattern characterization for pattern matching requires long time and huge effort due to the large number of possibilities.

**Decomposability** Pattern matching cannot be done incrementally due to the lack of decomposability. Any change in layout should invoke a new pattern matching, as the change cannot be decomposed from the original layout. Considering many ripup/reroutings in a detailed router, pattern matching is not efficient.

Therefore, we propose a simple yet effective weak grid type characterization scheme based on the following definitions:

- Weak grid (WG) is defined as a detailed routing grid filled with one of the predefined litho-prone shapes.
- Weak grid type (WGT) is defined as the type of the litho-prone shape embedded on the corresponding WG.

Fig. 2 (a) shows an example of two WGTs, a jog-corner and a line-end. Based on given predefined shapes which are highly prone to lithography or CD variation, the interference between WGT is studied statistically.

We describe our statistical WGT characterization in Algorithm 1. The first input is a set of WGT which includes via, jog-corner, line-end, fat-wire-edge, and so on. The second input is the maximum distance at which two types from  $T$  can interfere (typically less than  $0.8\mu m$ ). Then, as in line 5, we enumerate multiple patterns w.r.t. two types at various distances to see the relation between distance and a pair of WGTs. After performing a lithography simulation for each pattern as in line 8, we compute a mean EPE for a triple which consists of two WGTs and distance as in line 13. While computing the mean, we ignore noise/minor EPE hotspots (in our case,  $\leq 5nm$ ) as in line 9. Hence, the mean EPE statistically represents printability as a function of distance. Fig. 2 (b)-(e) shows some example patterns with the same distance between the jog-corner and the line-end.

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### Algorithm 2 WG\_Shadowing

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**Require:** A Table WGT\_TABLE, a grid  $e$ , a set of WGTs  $T$ , a max distance  $d$

- 1:  $G =$  a set of grids within  $d$  from  $e/\{e\}$
- 2:  $t =$  a WGT embedded at  $e$
- 3: **for** each grid  $g \in G$  **do**
- 4:   **for** each type  $t^* \in T$  **do**
- 5:      $g.cost[t^*] += WGT\_TABLE(t, t^*, dist \text{ from } g \text{ to } e)$
- 6:   **end for**
- 7: **end for**

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In typical case, the number of WGTs would be around 10, and the number of patterns for each pair of WGTs would be like 50. Thus, the total number of cases is about  $10 \cdot \frac{(10-1)}{2} \cdot 50 = 2250$  which can be done in a few hours including OPC (also one time job!). Therefore, the characterization update can be done in short time, and each characterization triple (the line 13 of Algorithm 1) needs only 4 bytes and  $O(1)$  access time by table lookup.

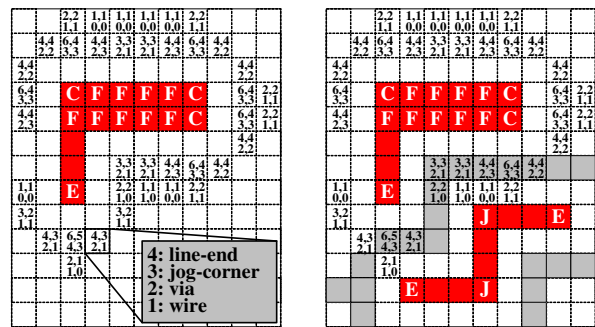
Consequently, with statistical WGT characterization, we can see advantages over pattern characterization in terms of runtime and space. Moreover, as any polygon can be decomposed into grids geometrically, we can estimate printability *incrementally*, which is critical for a detailed router. Then, the question is about the fidelity of our metric, which will be shown in Section 3.3.

## 3.2 Compact Litho-Metric with OPC

After the characterization, we can use it to estimate printability during detailed routing. We propose the following litho-metric for a detailed routing grid  $e$ :

$$litho(e) = \begin{cases} e.cost[t] & \text{if WGT of } e = t \\ 0 & \text{otherwise} \end{cases} \quad (1)$$

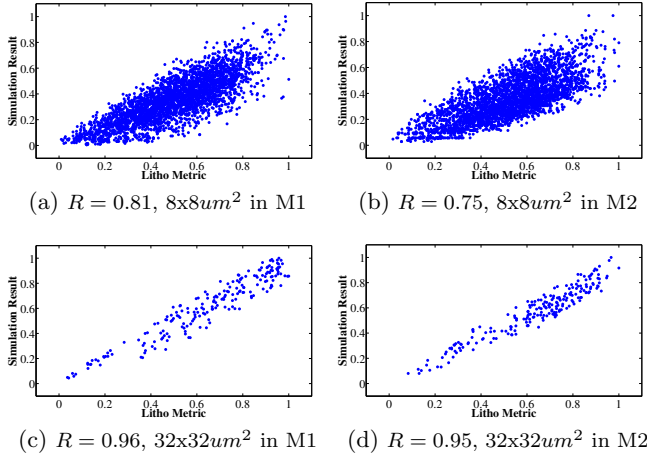
where  $e.cost[t]$  is a lithography cost computed by Algorithm 2. Fig. 3 shows a simple example of WG\_Shadowing around a blockage and a net. For each WG, we will shadow neighbor-



(a) WG\_Shadowing is performed along the contour of the blockage. Hence, grids within a certain distance get shadowed by a cost array.

(b) WG\_Shadowing needs to be performed along the routed wire. Thus, the costs in the arrays of the grey grids will be updated/increased.

**Figure 3:** Respectively assuming C, F, E, and J are blockage-corner, fat-wire-edge, line-end, and jog-corner, WG\_Shadowing examples are shown. Each grid has a cost array which contains the costs for jog-corner, line-end, via, and wire.



**Figure 4: Our litho-metric shows higher fidelity to post-OPC printability in larger scale.**

ing grids within the maximum distance. While shadowing a grid, we prepare costs for all possible WGTs so that the grid has a cost array as in line 5 in Algorithm 2. In Fig. 3 (a), each grid has four costs which will penalize any new polygon passing it by the corresponding cost. Later, if a wire is embedded in one of these shadowed grids, it gets a lithography penalty based on the WGT (e.g., whether a via is dropped, a line is ended, and so on) by Eq. (1). After the wire is embedded, we will perform WG\_Shadowing for grids around the wire as in Fig. 3 (b).

### 3.3 High Fidelity of Our Litho-Metric

We evaluate the fidelity of our litho-metric by comparing with Calibre-OPC/ORC (for detailed setup, see Section 5). Fig. 4 proves the high fidelity of our litho-metric where  $Y$  axis is the summation of EPEs. We collect the samples from industrial  $65m$  design layouts, while varying the sample size from  $8 \times 8 \mu m^2$  to  $32 \times 32 \mu m^2$ . When the sample area is  $8 \times 8 \mu m^2$  as in Fig. 4 (a) and (b), it does not correlate with the simulation result well enough to guide a detailed router. However, the larger the sample area is, the better it correlates, as shown in Fig. 4 (c) and (d). When the sample area is  $32 \times 32 \mu m^2$ , it correlates more than 95% for both M1 and M2 where the most number of litho-hotspots occur. The reason for higher fidelity for larger sample is because we take the average of EPE for each distance during WGT characterization as line 13 of Algorithm 1. With smaller sample area where we may get some extreme cases, the prediction can deviate from the real trend. Statistically, however, with larger sample area where we can get enough cases to capture the statistically real trend, the prediction gets more accurate.

Low correlation in small area is not a problem for us, as the goal of our metric is to capture the overall printability for entire chip. If we treat the design itself as a maximum sample area (where high correlation exists), we can improve the global printability by following our litho-metric. It is obvious that our metric cannot capture the fine scale lithography effect, but should be enough to guide optimization globally. If we guide a detailed router using our metric, we can obtain a globally litho-friendly layout which is exactly our objective in design stage printability optimization.

## 4. ELIAD

In this section, we propose our algorithm for ELIAD, an efficient lithography aware detailed router. Our router is guided by the metric in Section 3 based on Lagrangian relaxation technique which will be discussed in Section 4.1. The overall algorithm is proposed in Section 4.2.

### 4.1 Problem Formulation

We can mathematically formulate a lithography aware detailed routing problem as follows:

$$\begin{aligned} \min_P : & \sum_{e \in P} 1 \\ \text{s.t.} : & litho(e) \leq L \quad \forall e \in P \end{aligned} \quad (2)$$

where the objective is to minimize wirelength and the constraint is to keep  $litho(e)$  from Eq. (1) less than a given threshold  $L$ . If we treat the cost array in each grid as a weight-vector, optimally solving Eq. (2) is equivalent to finding multi-constrained shortest path (MCSP) [5] which is proven to be NP-hard [25]. Therefore, we use Lagrangian relaxation by introducing Lagrangian multiplier  $\lambda_e$  for each grid in the design. Then, we can show this [11, 22, 25]:

$$\begin{aligned} \min_P \{ \sum_{e \in P} 1 : litho(e) \leq L, \forall e \in P \} \\ \geq \max_{\lambda} \min_P \{ \sum_{e \in P} 1 + \lambda_e (litho(e) - L) : \lambda_e \geq 0 \} \end{aligned} \quad (3)$$

The implication from Eq. (3) is that a maximum lower bound of the optimal solution for Eq. (2) can be obtained by solving the following Lagrangian subproblem:

$$\begin{aligned} \max_{\lambda} \min_P : & \sum_{e \in P} 1 + \lambda_e (litho(e) - L) \\ \text{s.t.} : & \lambda_e \geq 0 \quad \forall e \in P \end{aligned} \quad (4)$$

which can be solved by repeatedly finding a min-cost path for each net after assigning  $1 + \lambda_e litho(e)$  to a grid  $e$ . Also, the optimal solution of Eq. (4) is the optimal solution of Eq. (2) under some conditions. See [25] for details. Since Eq. (4) is a convex programming and  $litho(e)$  is not differentiable everywhere, we can use a subgradient method to solve Eq. (4) in ELIAD as in Section 4.2.

### 4.2 Algorithm

As discussed in Section 4.1, we can implement, ELIAD by solving Eq. (4) as in Algorithm 3. In lines 1-6, we perform WG\_Shadowing for the existing blockages. In detailed routing, power/ground network, clock network, pins/connections from standard cells, and timing critical nets are already embedded forming routing blockages. Hence, we should detect the contour of each blockage and perform WG\_Shadowing around it. Since a blockage can be in a complicated shape, we use Moore-Neighbor Tracing algorithm [9] for contour detection in our implementation.

In lines 7-20, we use subgradient method where a min-cost path minimizing the objective of Eq. (4) for each net is searched. Since a new route not only is influenced by neighbors but also affects them, we need multiple iterations to converge. Subgradient method to solve MCSP is already used in [11, 22, 25], but our algorithm has two key improvements in terms of memory and convergence. First, in [11, 25], each detailed routing grid needs to have a cost array which should be as big as the number of nets in the design. As the number of nets is over thousands for even small ASIC, it may

result in unacceptable memory overhead. However, ours requires a cost array just as big as the number of grid types (in general, less than 10). Second, differently from [11, 25], we achieve faster convergence by starting with small non-zero Lagrangian multipliers ( $\lambda_e$ ) and performing WG\_Shadowing after each net is routed. Hence, even the first iteration will be lithography aware for faster convergence.

## 5. EXPERIMENTAL RESULTS

We implement ELIAD in C++ and test with two industrial 65nm ASIC designs on Intel Xeon 2.4 GHz Linux machine with 4G RAM. We use Calibre-OPC/ORC from Mentor Graphics for model based OPC and ORC. Our optical parameters are wavelength ( $\lambda$ ) = 193nm, numerical aperture (NA) = 0.85, and annular illumination  $\sigma = 0.92/0.72$ . The thicknesses of photo-resist and bottom anti-reflective coating (BARC) are 0.165 $\mu$ m and 0.038 $\mu$ m, respectively. Following industrial practice, we first perform full OPC, and then assume DOF=0.1 $\mu$ m during ORC. Fig. 5 illustrates our overall detail routing flow.

For though comparison, we prepare a conventional grid-based detailed router (**DR**) as well as a lithography-aware ripup/rerouting like RADAR [17] (**RR**). Instead of doing lithography simulation without OPC in [17], we apply OPC to RR as well for more accurate hotspot detection. Therefore, we can have four different routers **DR**, **DR+RR**, **ELIAD**, and **ELIAD+RR**. Note that we use A\* search to find min-cost path in all the routers.

Table 1 comprehensively compares results from all the routers. It shows that ELIAD significantly improves overall EPE for both designs. In terms of M1 hotspot (with 15nm EPE tolerance), ELIAD has 75% less than DR and 66% less than DR+RR for ckt1, and 84% less than DR and DR+RR for ckt2. The reduction is even much more for M2 hotspot, at least 93% and 96% for ckt1 and ckt2, respectively. When ELIAD combined with RR (ELIAD+RR), it can further improve printability (about 10%). This implies

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### Algorithm 3 ELIAD

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**Require:** A set of blockages  $K$ , a set of nets  $N$ , a table WGT\_TABLE, a max distance  $d$

```

1: for each blockage  $k \in K$  do
2:    $G =$  a set of grids from contour of  $k$ 
3:   for each grid  $g \in G$  do
4:     WG_Shadowing(WGT_TABLE, g, d)
5:   end for
6: end for
7:  $\lambda_e = \epsilon > 0, \forall e$  in design
8: repeat
9:    $P \leftarrow \emptyset$ 
10:  for each net  $n \in N$  do
11:     $M =$  a set of grids on min-cost path of  $n$  by Eq. (4)
12:    for each grid  $m \in M$  do
13:      WG_Shadowing(WGT_TABLE, m, d)
14:    end for
15:     $P = P \cup M$ 
16:  end for
17:  for each grid  $e \in P$  do
18:     $\lambda_e = \max(0, \lambda_e + \theta \cdot litho(e))$ 
19:  end for
20: until max iteration

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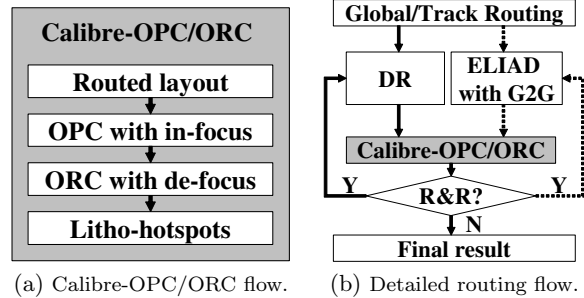


Figure 5: Industrial Calibre-OPC/ORC flow is applied in our detailed routing experiments.

that ELIAD, a correct-by-construction approach is highly superior to post-optimization (RR) approach, but can be complementary with it (RR) by providing an excellent starting point. Regarding runtime, while ELIAD is at most 60% slower than DR, RR involves huge overhead mainly from hotspot detection using expensive OPC/ORC. ELIAD is at least 10x faster than any approach with RR (DR+RR and ELIAD+RR). Finally, there is negligible difference among routers in terms of wirelength.

Table 2 further analyzes the performance of ELIAD by comparing EPE reduction with DR+RR in partition-by-partition manner. As expected, ELIAD yields significantly better EPE reduction, but our point here is that ELIAD can improve EPE globally, while DR+RR cannot. When we compute the coefficient of variance (cov) of hotspot reduction over 12 partitions (P1-P12) for ELIAD and DR+RR, ELIAD and DR+RR have 0.45 and 0.046 respectively. The implication of 10x smaller cov is that the performance of RR highly depends on the complexity of initial routing and local congestion (e.g., hard to find a totally new routing path), as it cannot make radical change to improve printability. However, since ELIAD runs in a correct-by-construction way from the scratch, it can consistently improve printability all over the place. This situation can also be observed from the Fig. 6 in RADAR [17] where most of hotspot removals are from the outer regions rather than the core.

## 6. CONCLUSION

Manufacturability optimization during design stage receives larger attention than any time before due to aggressive technology scaling and delayed next-generation lithography system. In this paper, we present ELIAD, a lithography aware detailed router in a correct-by-construction approach based on a fast yet high fidelity litho-metric with OPC consideration. Experimental results shows that ELIAD is significantly superior to a ripup/rerouting technique or a post processing strategy, only at small runtime overhead.

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**Table 1: Comparison between various routers on two industrial designs.**

design	router	wirelen (mm)	runtime breakdown (sec)			EPE (nm)						Ratio		
			router	OPC/ORC <sup>a</sup>	total	M1			M2			runtime	M1 hotspot	M2 hotspot
						5-10	10-15	15+	5-10	10-15	15+			
ckt1 59.5K $\mu m^2$ 5.6K nets	DR	6002.4	509.9	n/a	509.9	16572	5182	<b>285</b>	7468	4304	<b>90</b>	1	4.0	15.0
	DR+RR [17]	6008.0	835.3	7529.0	8364.3	13592	4549	<b>226</b>	4831	2176	<b>82</b>	16.4	3.1	13.7
	ELIAD	6003.5	798.6	n/a	798.6	1985	985	<b>76</b>	257	37	<b>6</b>	1.6	1.1	1
	ELIAD+RR <sup>b</sup>	6008.1	1194.5	7775.6	8969.1	1774	895	<b>72</b>	221	27	<b>6</b>	17.6	1	1
ckt2 50.2K $\mu m^2$ 7.9K nets	DR	10168.5	353.8	n/a	353.6	17124	5834	<b>424</b>	4082	2062	<b>54</b>	1	7.6	27.0
	DR+RR [17]	10175.1	606.4	6654.1	7260.5	14104	5127	<b>394</b>	2614	1385	<b>49</b>	20.5	7.0	24.5
	ELIAD	10169.6	491.9	n/a	491.9	1318	1209	<b>69</b>	354	22	<b>2</b>	1.4	1.2	1
	ELIAD+RR	10174.8	767.8	6688.4	7456.2	1179	1125	<b>56</b>	331	18	<b>0</b>	21.1	1	-

<sup>a</sup> The runtime ratio between OPC (8 iterations) and ORC is about 2.5 : 1 according to our experiments.

<sup>b</sup> EPE tolerance for litho-hotspot is 15nm.

**Table 2: Detailed EPE reduction (%) over DR comparison between DR+RR and ELIAD by partition.**

router	DR+RR [17]								ELIAD							
	ckt1				ckt2				ckt1				ckt2			
design	M1		M2		M1		M2		M1		M2		M1		M2	
layer	5-10	10+	5-10	10+	5-10	10+	5-10	10+	5-10	10+	5-10	10+	5-10	10+	5-10	10+
EPE (nm)	5-10	10+	5-10	10+	5-10	10+	5-10	10+	5-10	10+	5-10	10+	5-10	10+	5-10	10+
P1	31.4	30.5	13.5	49.3	14.5	14.4	36.1	36.6	82.1	73.2	91.7	98.9	92.9	77.9	90.4	100.0
P2	21.9	13.1	33.0	55.7	12.1	7.3	37.3	37.0	82.8	69.8	90.3	98.8	91.7	74.5	90.6	99.1
P3	22.8	17.6	24.5	46.7	16.7	11.1	40.2	31.4	83.5	74.4	92.4	98.8	90.0	79.0	94.0	99.2
P4	11.6	1.9	35.8	40.3	32.9	34.3	44.0	53.8	92.7	77.7	84.7	97.0	90.5	91.4	84.0	100.0
P5	9.6	8.5	37.8	41.5	18.6	17.8	16.7	16.0	95.4	88.6	99.1	98.8	90.4	76.9	92.3	99.5
P6	18.4	10.5	46.9	55.5	19.4	19.6	37.2	39.2	91.9	86.5	99.9	100.0	88.6	73.5	91.4	99.5
P7	12.7	20.1	40.8	51.1	14.4	22.4	41.3	41.3	88.2	85.1	99.9	98.6	91.8	81.6	89.0	97.1
P8	9.4	0.0	10.3	22.4	8.2	21.7	37.8	50.0	85.9	91.1	99.1	100.0	95.9	91.7	97.3	95.5
P9	9.1	19.2	43.6	51.8	19.8	20.5	37.9	38.0	93.1	87.2	99.5	99.1	94.4	86.5	90.8	99.5
P10	16.7	15.1	41.1	52.2	17.1	19.8	30.7	28.5	93.4	91.5	99.8	100.0	93.7	85.4	92.4	98.2
P11	16.3	17.7	49.5	59.0	23.0	24.3	46.4	38.6	83.5	84.7	99.7	99.7	95.7	87.4	91.2	99.1
P12	-8.3	10.0	34.9	58.5	43.4	48.1	-14.8	23.1	94.8	95.0	100.0	100.0	94.6	86.4	88.9	100.0
avg	14.3	13.7	34.3	48.7	20.0	21.8	32.6	36.1	89.0	83.7	96.3	99.2	92.5	82.7	91.0	98.9
std	9.7	8.3	12.4	10.2	9.6	10.7	16.7	10.5	5.1	8.1	5.2	0.9	2.4	6.3	3.2	1.4
cov ( $\frac{std}{avg}$ )	0.68	0.61	0.36	0.21	0.48	0.49	0.51	0.29	0.06	0.10	0.05	0.01	0.03	0.08	0.03	0.01

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