Modeling and characterization of contact-edge roughness for minimizing design and manufacturing variations

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Abstract. Despite intensive attention on line-edge roughness (LER), contact-edge roughness (CER) has been relatively less studied. Contact patterning is one of the critical steps in a state of the art lithography process; meanwhile, design rule shrinking leads to larger CER in contact holes. Since source/drain (S/D) contact resistance depends on contact area and shape, larger CER results in significant change in a device current. We first propose a CER model based on the power spectral density function, which is a function of rms edge roughness, correlation length, and fractal dimension. Then, we present a comprehensive contact extraction methodology for analyzing process-induced CER effects on circuit performance. In our new contact extraction model, we first dissect the contact with a same distance, and then calculate the effective resistance considering both the shape weighting factor and the distance weighting factor for stress-induced complementary metal-oxide semiconductor (CMOS) cells. Using the results of CER, we analyze the impact of both random CER and systematic variation on the S/D contact resistance, and the device saturation current. Results show that the S/D contact resistance and the device saturation current can vary by as much as 135.7 and 4.9%, respectively. [DOI: 10.1117/1.3504697]

Subject terms: contact-edge roughness; line-edge roughness; lithography; variation; characterization; standard cell; manufacturing design.

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1 Introduction

As semiconductor device dimensions have continuously scaled into the nanometer regime, contact printability has become one of the most critical issues in the lithography process.[1–4] Contact variation due to lithography causes area change and overlay problems between the metal layer and silicide layer from the targeted design, which leads to contact resistance variation, and therefore, transistor performance degradation.[1,4]

There are two types of lithography variations that cause undesirable performance mismatch in identically designed transistor: *systematic variation* and *random variation*. Systematic lithography variation for contact patterning is caused by deterministic pattern proximity. As shown in Fig. 1(a), the lithography proximity makes the contact pattern rounded due to the limitation and variation of lithography equipments. A lithography process with systematic variation is defined by a set of defocus and exposure levels. Even for nominal defocus and exposure levels, the printing of small geometries results in loss of image quality.[5,6] This causes distorted nonrectangular shapes of the geometries in the source/drain (S/D) contact layer.

The random lithography variation, e.g., contact-edge roughness (CER) for contact patterning, becomes more important in sub-32-nm node devices.[7–10] That is because a patterned photoresist (PR) layer used to produce such small feature sizes typically has a high aspect ratio, and maintaining a desired critical dimension (CD) can be very difficult due to small process margins.[11,12] Despite intensive attention on line-edge roughness (LER),[13–16] CER has been relatively less studied even though contact patterning is one of the most difficult lithography processes. As aggressive scaling continues into the nanometer regime, CER does not scale accordingly and becomes an increasingly larger fraction of the contact pattern.[8,17,18]

Geometrically, CER caused by lithography process variation brings both edge roughness and area change of a contact pattern,[8,10] as shown in Fig. 1(b), which can result in the change of contact resistance and even device performance degradation. According to the experimental results in 32-nm contact manufacturing, if the 3σ roughness of CER is 4 nm, then the area variation (σ) was more than 48 nm^2. When we consider 3σ corner variation, the area variation could be up to 144 nm^2, which is as much as 10% of the total area of a circular contact.

Moreover, if the systematic lithography variation, i.e., dosage and focus, is also added in the contact patterning, the contact area variation would be much more. Reference 4 shows that the variation of contact resistance is up to 50% in 65-nm designs based on their silicon experimental data, where both systematic and random variations are considered for the manufacturing process. Thus we can easily guess that the variation could be higher in 32-nm devices, because the portion of systematic and random contact variation becomes much larger than that of 65-nm devices in a whole contact area.

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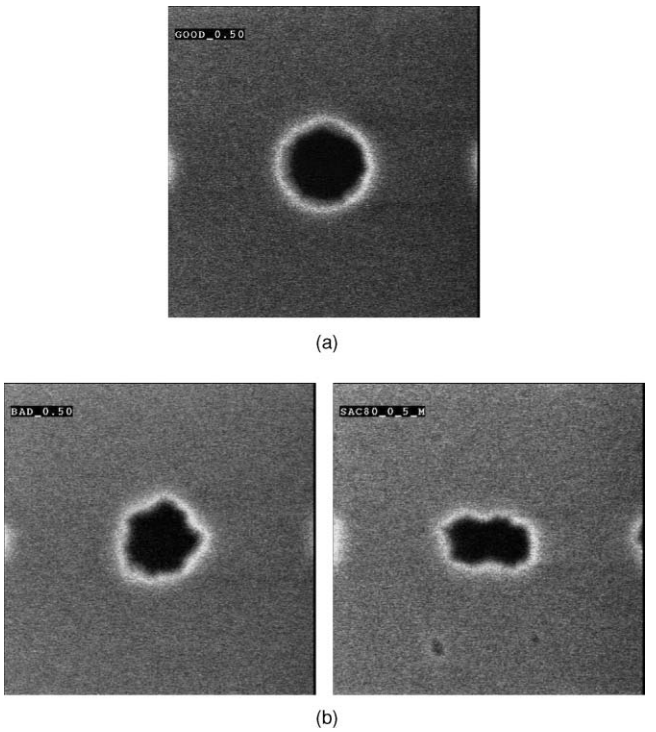

Fig. 1 Lithographic variations for contact patterning: (a) lithographic proximity and (b) systematic and random CER variation.

In this work we propose a CER model and a comprehensive contact layout extraction method for analyzing process-induced CER effects on circuit performance. Our approach is mainly based on the new SPICE-level compact model (Synopsys, Mountain View, California) for S/D contact layout. The objective of the proposed CER model and the extraction method is to understand the impact of contact variation on circuit performance, and to give a guide for robust design of standard cell layouts. The major contributions of this work include the following.

- We propose a CER model based on the power spectral density model, which is a function of rms edge roughness, correlation length, and fractal dimension.
- We present the first systematic study on the impact of contact shape on the device saturation current, and propose a simple yet effective model to estimate the performance impact of S/D contacts. Our model considers contact distance from gate, contact shape, and contact area.
- We investigate the impact of S/D contact variation on the circuit performance in a standard cell. This is the first study for the CER-aware extraction and its timing impact.

The rest of the work is organized as follows. Section 2 describes the sources of S/D contact variation and the timing impact. Section 3 presents our CER model. Section 4 presents the new compact model and its validation. Experimental results are discussed in Sec. 5, followed by conclusions in Sec. 6.

2 Impact of Source/Drain Contact Variation

Lithography tools have remained at 193 nm, even with technology scaling below 32 nm resulting in significant variations. Printing of small geometries results in loss of image quality,[5] which results in distorted nonrectangular shapes of the geometries in the S/D contact layer. In reality, due to the relatively small process margin, contact patterning is one of the most challenging tasks in hyper-NA lithography.[10,12] The increased imaging challenges for advanced node contacts lead to strong off-axis illumination[19] and inverse lithography techniques,[11,20] which implies that modern contact patterning still suffers from the CD and area variation due to the lithography proximity and process variation. Both variations cause the area change of contact plug, which induces device performance degradation.

Electrically, the contact area variation is highly related to the S/D device saturation current degradation. In this experiment, we used a commercial HSPICE (Synopsys, Mountain View, California) simulator[21] by changing the source/drain contact resistances, and assumed that the contact resistance of n-type metal oxide semiconductor field-effect transistor (NMOS) and p-type metal oxide semiconductor field-effect transistor (PMOS) are the same. The nominal contact size is 40 nm for all standard cells. In our experiments, as shown in Figs. 2(a) and 2(b) in NMOS devices, we observe that

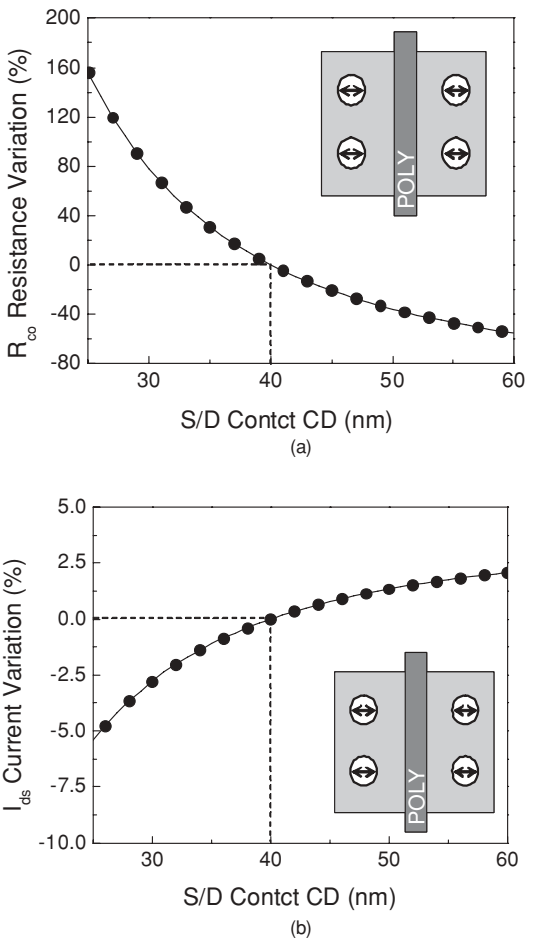

Fig. 2 The impact of S/D contact CD variation: (a) impact on the contact resistance and (b) impact on the device saturation current.

as the S/D contact CD decreases, the S/D contact resistance dramatically increases, whereas the device saturation current greatly drops down. Since the parasitic S/D contact resistance is highly increased due to the smaller contact area, the portion of the contact resistance becomes higher in a total device current path from the source to the drain. The contact resistance and current variation are highly correlated with a resistivity (~sheet resistance) of a contact and silicide materials. We measured S/D contact resistances and currents using lots of standard cells, where we found up to 5% degradation of the saturation current and more than 100% increase of the S/D contact resistance with 10-nm S/D contact CD variation. Figure 2 from a 32-nm node inverter cell shows that the S/D contact resistance and current variations are highly correlated with the S/D contact CD variation. As we mentioned in Sec. 1, CER can change the edge roughness, contact area, and contact shape. Therefore, we should first make the CER model and then propose a new contact layout extraction model to understand the impact of CER on contact resistance and device performance.

3 Contact-Edge Roughness Model

Conventionally, LER is represented as a function of spatial frequency through the power spectral density (PSD) function, which is theoretically the Fourier transform of the autocorrelation function.[22–25] If we define $z(x)$ as a 1-D distribution of edge locations, the PSD $S(f)$ can be expressed as in Eq. (1)[24]: PSD $S(f)$ is mathematically defined as;

$$S(f) = \lim_{L\to\infty} \frac{1}{L} \left| \int_{-L/2}^{L/2} z(x) \exp(2\pi i f x)\, dx \right|^2. \quad (1)$$

Therefore, the autocorrelation function of $z(x)$, $R(\tau)$, is formulated as:

$$R(\tau) = \mathbb{F}^{-1}\{S(f)\} = \lim_{L\to\infty} \frac{1}{L} \int_{-L/2}^{L/2} z^*(x) \cdot z(x+\tau)\, dx. \quad (2)$$

The rms roughness σ is often defined in terms of $z(x)$ as:

$$\sigma^2 = \lim_{L\to\infty} \frac{1}{L} \int_{-\infty}^{\infty} |z(x)|^2\, dx = 2\int_0^{\infty} S(f)\, df. \quad (3)$$

Thus, the autocorrelation function $R(\tau)$ follows an exponential function by the distance r for line edge as follows:

$$R(r) = \sigma^2 \exp\left[-\left(\frac{r}{L_c} \right) 2^{\alpha} \right], \quad (4)$$

where L_c is the correlation length, σ is the standard deviation of the line edge, and α is related to the fractal dimension D ($\alpha = 2\text{-}D$). Therefore, PSD is approximated by the following equation[23]:

$$S(k) = \frac{2\sigma^2 L_c}{\left(1 + k^2 L_c^2\right)^{0.5+\alpha}}, \quad (5)$$

where $k = 2\pi f$, $f = i1/N\Delta z$, and $0 \le i \le N/2$, N is the number of points along the line. Hence, the LER for a large number of resists can be characterized by just three numbers, σ, L_c, and α.

σ, rms amplitude, is the most important parameter for LER. σ corresponds to the transversal magnitude to the line, and the larger σ shows greater roughness of the line, whereas the correlation length L_c shows a longitudinal magnitude along the line, and the fractal dimension α is related to the high frequency fluctuations (edge smoothness) of edge roughness. Among the three parameters of LER, L_c and α are highly dependent on the photoresist type and relatively less critical than σ.[25] Thus, in this work we are focusing on presenting LER with regard to σ.

With the magnitude information provided by $S(f)$, we can reconstruct random line edges by applying a random phase to each frequency component of the PSD to form a unique signal in the frequency domain. A line edge with roughness can be simulated by doing an inverse Fourier transform of this signal. Random lines are distinguished through random phases applied. The contact roughness-formation mechanism could be different from lines, and there was not as much work done for contacts as for lines. Here, we assume that the distribution of radii of a contact at angles from 0 to 2π follows the PSD mentioned before. Hence, contacts with roughness can be reconstructed.

4 Circuit Level Compact Source/Drain Contact Model

Lithography variation including LER can vary the S/D contact shape, area, and even the distance from the gate line, which cause performance degradation. Thus, we should consider the impact of S/D contact variation on the standard cell performance in design time, which needs a new circuit level compact model of the S/D contact pattern. In this section, we first illustrate the technology computed aided design (TCAD) simulation of a complementary metal oxide semiconductor (CMOS) cell to generate base-line data representing wafer experimental results in Sec. 4.1. Then we propose our new circuit level compact model for nonrectangular contact layout in Sec. 4.2.

4.1 *Technology Computer Aided Design Simulation Setup*

A Sentaurus (Synopsys, Mountain View, California) process and device simulator[26] is used to estimate impacts of the S/D contact variation on device performance, and is used to verify accuracy of our compact model for nonrectangular contact layout. To investigate the impact of S/D contact patterning displacement, we used the 2-D device structure of a 32-nm standard cell in Fig. 3(a). Then we measured the S/D saturation current by varying the position of S/D contacts. The 32-nm CMOS cell uses intensive stress-enhancement techniques: NMOS uses a tensile stress liner and PMOS has a compressive stress liner and embedded SiGe in the S/D region.

We also use 3-D TCAD simulation for looking into the impact of contact size and shape. We first generate printed images of contact patterns with optical proximity correction (OPC) taken into account. For lithography simulation, we use a commercial lithography simulation tool.[27] The standard cell layout is converted into 3-D structure for TCAD simulation with a Ligament (Synopsys, Mountain View, California) layout editor[26] as shown in Figs. 3(b) and 3(c). To save simulation time and memory, a quarter of the structure mesh is generated, and the other structure is created by reflection.

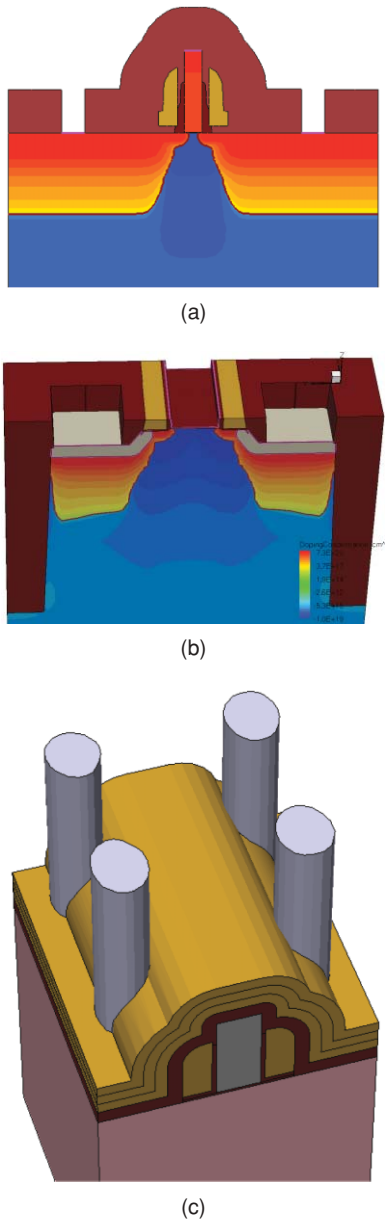

Fig. 3 Structural view of TCAD simulation: (a) 2-D TCAD structure, (b) 3-D TCAD structure, and (c) 3-D structure from printed images of S/D contacts.

4.2 *Equivalent Contact Resistance Model*

Mask overlay problems cause the displacement of the S/D contact patterning from the gate polylayer. The change of the contact position also affects the saturation current in a device. In 32-nm node standard cells, MOSFETs are used as a stress enhancement technique in which the mobility of carriers in the substrate depends on the distance of contact and gate polyline, because neighboring contacts can relax the actual strain in channel.

To analyze the overlay impact due to contact pattern shifting, we use rigorous 3-D TCAD simulation tools combined with our CER-generated contact layout, and investigate the impact on the systematic and random lithographic variations on manufacturing as well as the timing and power variations on circuit performance.

According to previous papers[2,28,29] the variation of the contact position causes a degradation of the saturation current in the stress-induced device. This is because neighboring contact holes can locally relax the actual strain in a channel. To investigate the current variation according to the S/D contact pitch, we simulated device current variation with 3-D TCAD simulation, assuming that the S/D contacts are placed the same distance from the gate polyline. As shown in Fig. 4(b), in which the results are referred from Ref. 29, the saturation current degrades as contacts are placed closer to the gate in PMOS devices. Since the mobility modulation of PMOS is different from that of NMOS, the trend of NMOS devices may be another trend. Although the current variation can be different from the input stress parameter, we find that the current variation by stress relaxation can happened due to the displacement of the contact position.

The contact shape also impacts the device current in our experiments. To scrutinize the impact of contact shape, we test a set of contact patterns that have the same contact area and contact position but different contact shape under TCAD simulation conditions; meanwhile, the total area of the contact is equal for all test layouts. As shown in Fig. 5, as the contact length along the gate line is larger, the saturation current is increased. This is because there is less current crowding from the S/D electric field and less stress

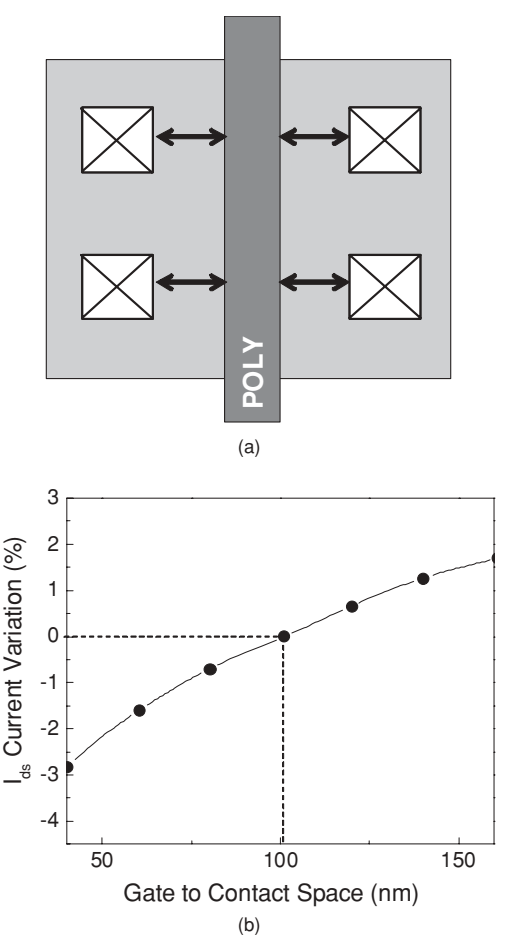

Fig. 4 The impact of S/D contact position: (a) view of contact space to polyline, and (b) impact of contact position variation on device saturation current.

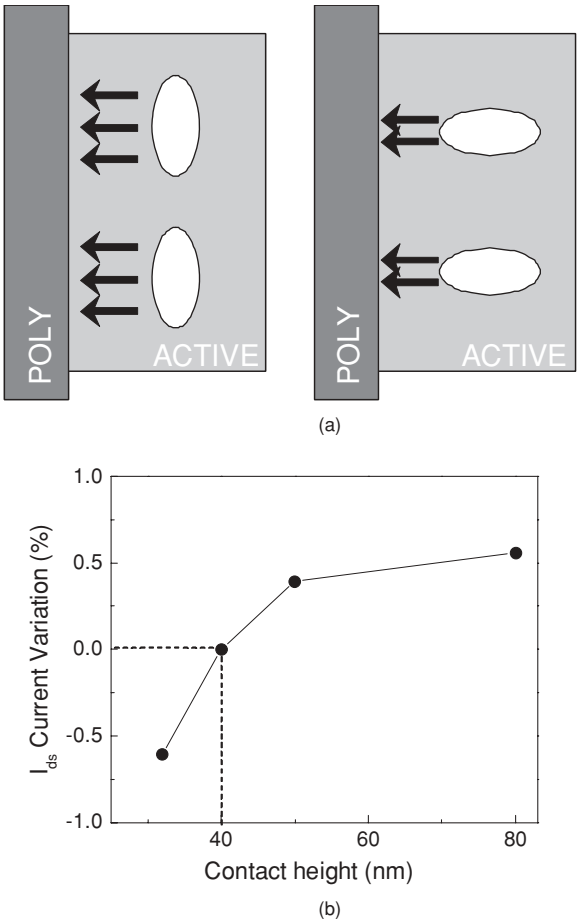

Fig. 5 The impact of S/D contact shape: (a) view of contact shape, and (b) impact of contact shape variation on device saturation current.

Table 1 Algorithm 1: equivalent S/D contact resistance model.

Require: a SPICE netlist *N*, a set of lookup table *T*, contact print-mages *I*

1: $nCNT = I \cap nactive$

2: $pCNT = I \cap pactive$

3: $totalR = 0$, weighted area factor inv$R$

4: **for** each contact $C \in nCNT$ **do**

5: find distance between contact and gate

6: $invR_C = 0$, resistivity ρ

7: **for** each *slice* $S \in C$ **do**

8: find a sliced area A

9: find distance/shape weighting factor ω_d, ω_s

10: $invRC \mathrel{+}= \omega_d \cdot \omega_s \cdot A$ from T

11: **end for**

12: $invR \mathrel{+}= invR_C$

13: **end for**

14: update $totalR = \rho / invR$

15: **for** each contact $C \in pCNT$ **do**

16: same sequence as *nCNT*

17: **end for**

18: update netlist *N*

relaxation of the stress liner, as the longest contact length is in the same direction as the gate.

As we can see in Figs. 2, 4, and 5, the saturation current due to the variation of S/D contact is highly dependent on the contact area, the horizontal distance from the gate line, and the contact shape along the vertical gate line. Since the saturation current is in inverse proportion to the contact resistance, we can consider the current impact of S/D contact by updating the S/D contact resistance. It implies that we get an accurate S/D contact resistance by exhibiting both the horizontal distance weighting factor and the shape weighting factor of the vertical direction.

To estimate the current impact of contact resistance in a circuit level simulation, we propose an equivalent contact resistance model for various shapes of contact patterns, as described in the algorithm in Table 1. We first construct a set of look-up tables that include shape weighting factor and distance weighting factor for NMOS and PMOS S/D contact. Those two weighting factors are directly generated from the relations among the saturation current and the contact distance variation in Fig. 4, and the contact shape variation in Fig. 5, respectively. Once the printed images of contact holes are generated, we then classify NMOS and PMOS contacts in lines 1 and 2. Each contact is vertically sliced by a set of equal width polygons, which keeps the original contact edge, as shown in Fig. 6. Then, in lines 8 and 9, we calculate a sliced polygon area and get a shape weighting factor (ω_s) and a distance weighting factor (ω_d). The weighting factors are directly related to the saturation current. Therefore, the weighting update can be done in O(1) access time.

Given the i'th slice of a contact, the resistance of a sliced polygon is as follows:

$$R_i = \frac{\rho}{\omega_{d,i} \cdot \omega_{s,i} \cdot A_i}, \tag{6}$$

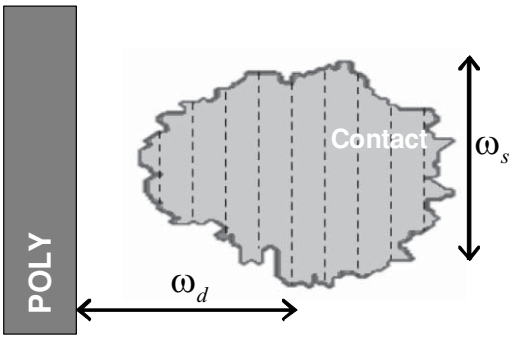

Fig. 6 A compact model of S/D contacts: we propose a compact S/D contact extraction model by considering the contact position, shape, and area.

where ρ is resistivity and A_i is the area of a slice. Since the S/D contact resistance is in inverse proportion to the contact area, the equivalent resistance of a contact is computed by summing all weighted areas of sliced polygons as the following equation:

$$\sum_i \frac{1}{R_i} = \frac{1}{\rho} \cdot \sum_i (\omega_{d,i} \cdot \omega_{s,i} \cdot A_i). \quad (7)$$

Since the S/D contact resistance is highly dependent on the device saturation current, we can make the relation between the saturation current and our new contact model as the following equation:

$$I_{dsSat} \propto \frac{1}{R_{co}} = \frac{1}{\rho} \cdot \sum_i (\omega_{d,i} \cdot \omega_{s,i} \cdot A_i). \quad (8)$$

Since the total contact area can be a linear function of the number of contacts,[29] the total weighted area is summated for all contact holes in line 12 in Algorithm 1 in Table 1. The total resistance is calculated by dividing the resistivity (ρ) by the total weighted area as described in line 14. By applying this compact model, we can deal with any kind of contact shape due to the lithography variations.

5 Experimental Results

We implemented the compact S/D contact extraction model in Tcl and Perl script language and tested with the industrial 32-nm standard cell. The nominal contact size is 40 nm for all standard cells. After calculating the effective S/D contact resistance, we updated the value in a netlist file and measured the current and the delay using HSPICE.[21] For model-based OPC and printed images of S/D contacts, we used Calibre-OPC/Printimage (Mentor Graphics, Wilsonville, Oregon).[27] Our optical parameters are wavelength (λ) = 193 nm, numerical aperture (NA) = 1.25 immersion lithography, and quasar unpolarized illumination σ = 0.9/0.7. The thickness of photoresist is 150 nm. Following industrial practices, we first perform full OPC for all contact holes and swept the process variation: dose = $\pm$7%, focus = $\pm$50 nm, and mask error = $\pm$1 nm. Then, we chose the nominal, the worst, and the best printed images for the given contact layer.[30] For delay and current simulation, we set the nominal S/D resistance on 100Ω as defined in the ITRS road map for 32-nm CMOS devices.[31]

Figure 7 illustrates the overall flow of our model-based geometrical and electrical analysis toolkit. The flow is divided into three main steps.

1. **Print Image Simulation**
   This step involves simulating the lithography models and generation of nonrectangular contours/shapes due to the printed image. We use commercial OPC and lithography simulation tools to get the print images of the nominal condition and process corners. After doing lithography print image simulation, rule-based etch corrections for etch proximity effects are applied to the print images. Once we recieve the final print images, we can also simulate the impact of CER. Input CER conditions are first requested, then the CER variations are added on the edge of the final print images.

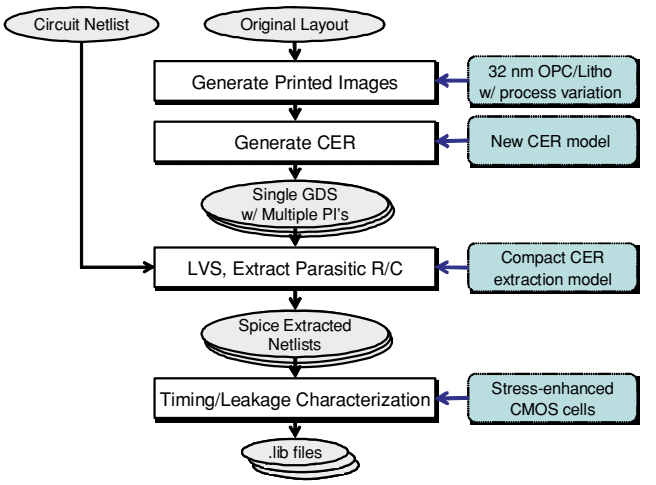

Fig. 7 CER-aware cell layout extraction and characterization flow.

2. **Extraction with print image**
   This step extracts device dimensions considering the nonrectangular shape in the S/D contact layer due to the print image. To get the parasitic resistance and capacitance parameters of a cell, we use a commercial layout extraction tool; meanwhile, we back-annotate the contact resistance by our circuit level compact extraction model.
3. **Characterization for several corners**
   This step characterizes the cells for delay and leakage information using the extracted parameters from the previous step. We use a commercial circuit simulation tool to get the delay and power of a cell for each process corner.

The simulated print image is written to a new layout file, which is an input file for an extraction tool. We use an industrial extraction tool to extract the devices and parasitic parameters in a SPICE netlist format. This extraction is then updated with actual contact resistance values, followed by timing and power analysis with an industrial circuit simulator. All the sequences are implemented and automated in our cell characterization flow.

We first validate our compact S/D contact model by comparing with a rigorous process/device simulation (TCAD)[26] and HSPICE simulation (conventional).[21] Note that the conventional circuit simulation just considers the contact area variation, which is directly related with the contact resistance by dividing the contact resistivity by the contact area; meanwhile, it is limited to analyzing the contact shape and the contact distance effect due to device stress relaxation. Figure 8 proves that our contact resistance model is well matched with TCAD results in terms of the distance from the PMOS gate [Fig. 8(a)], the contact shape [Fig. 8(b)], and the contact CD (area) of NMOS [Fig. 8(c)]. The reason why our model goes with the TCAD results is that we use the contact distance and shape weighting look-up tables generated from accurate TCAD simulations. The result shows the great agreement with the rigorous TCAD results with the overall 0.16% current error. By directly implementing our equivalent S/D contact model into the conventional circuit model,

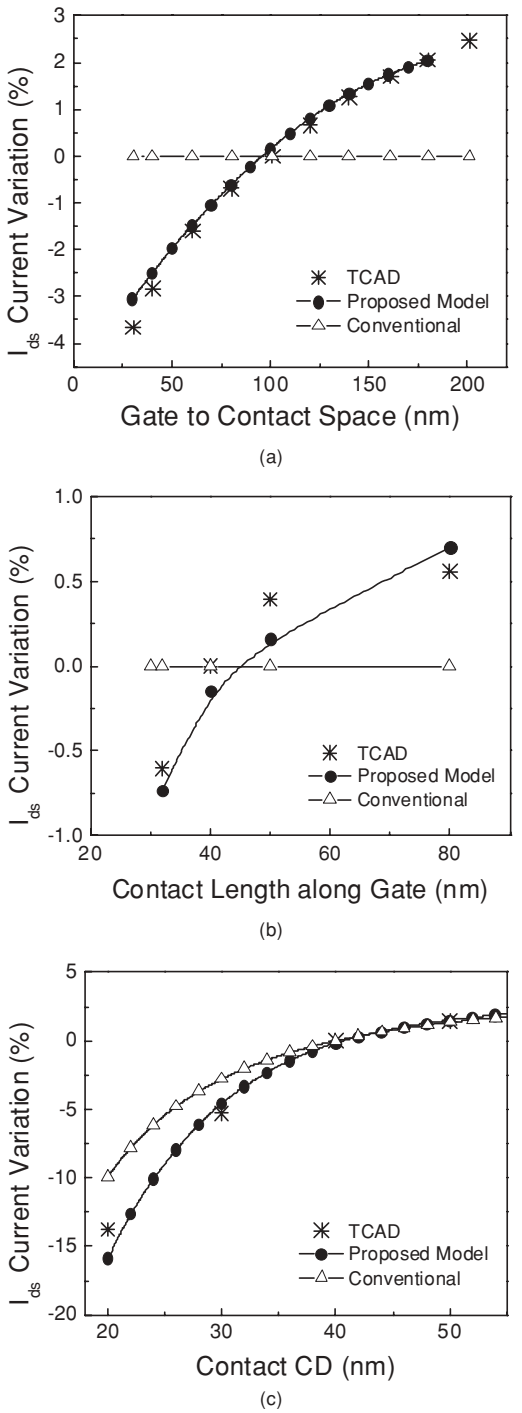

Fig. 8 Validation and results of our compact S/D contact extraction model: (a) contact displacement, (b) shape, and (c) area.

we can handle the contact variation in fast simulation time because there is no additional simulation overhead.

With our CER and contact extraction model, we analyzed the impact of CER on the S/D contact resistance and the saturation current. We first ran the contact OPC and print-image simulation with the best optical condition. In conventional line-edge roughness (LER), the realistic value of LER for 32 nm is around 4 nm or so. Meanwhile, CER could be higher than LER, because CER induces change of contact

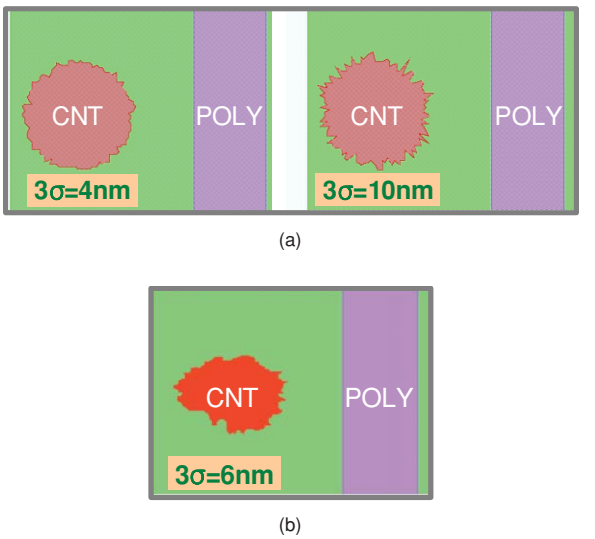

Fig. 9 Contact-edge roughness simulation: (a) circular-type estimation, where the mean contact area does not change, and (b) noncircular-type estimation, in which the contact area changes according to the edge roughness based on wafer experimental data.

shape. Moreover, lithography proximity for contacts, e.g., contact corner rounding, shortening, bridging, etc., makes CER much worse. Thus, we swept CER on the contact printed images 3σ from 0 to 10 nm, where we generated two CER cases: 1. circular-type CER, where the mean contact area does not change; and 2. noncircular-type CER, in which the contact area changes according to the edge roughness as shown in Fig. 9. Based on silicon wafer results, we change the contact area with respect to the rms CER in the noncircular-type CER. To understand the impact of CER, the only input variable is the rms value of CER, thus we fixed all other lithography process variables, e.g., dosage, focus, and mask bias. Then, we generated more than 1000 CER patterns for a particular rms value of CER, so that the results are shown as a distribution.

We investigated the S/D contact resistance variation with the amount of CER, then the device saturation current variation in an industrial 32-nm inverter standard cell, where the nominal contact CD is 40 nm. The black circled dot represents the average of the variation, and the small rectangular bar shows the upper and lower bound of the variation in Fig. 10. It assumes that CER is generated on top of the circular shape of contacts. The contact position and shape weighting factors are also considered in this case to receive the more accurate contact resistance value. As shown in the results, the deviation between the upper and lower bounds is increased as the CER increases, while the average values have no significant difference. Even though the geometrical center of a contact is not changed in the standard cell, the result reveals that the variation of the S/D contact resistance and the saturation current are up to 24.5 and 0.90%, respectively, where the rms CER value is 10 nm. Due to the small process window (tolerance) of contact patterns, the 10 nm of CER could happen in a sub-32-nm lithography process, which means that more than 24% change of the S/D contact resistance can occurred.

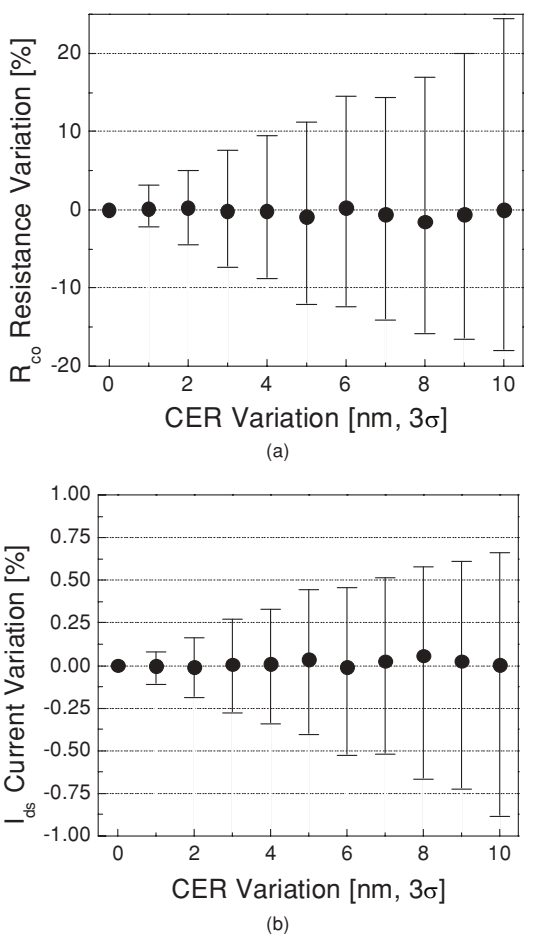

Fig. 10 The impact of CER on (a) the contact resistance and (b) the saturation current when the position, shape, and area weighting factors are considered in a stress-enhanced NMOS cell.

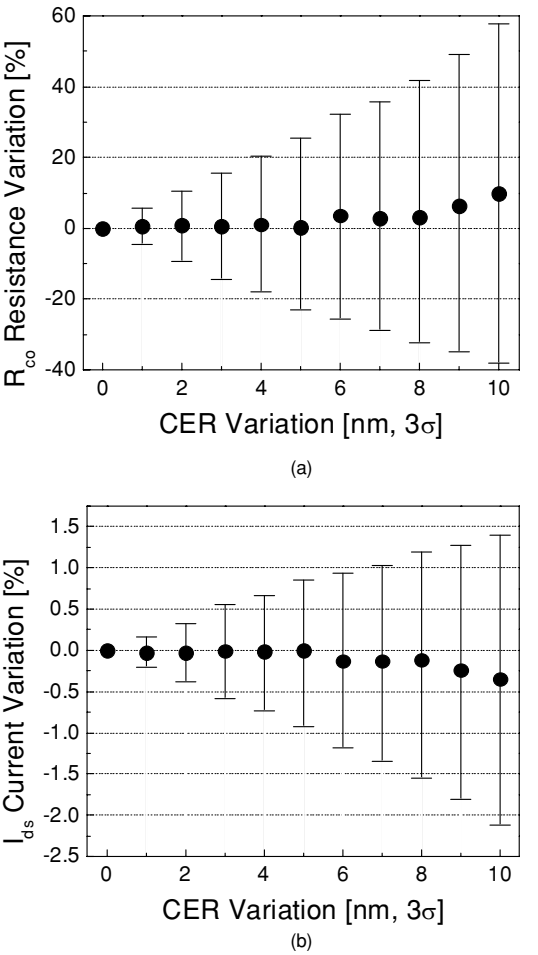

Fig. 11 The impact of CER on (a) the contact resistance and (b) the saturation current when CER causes the change of the S/D contact area at the nominal lithography condition.

Figure 11 shows the impact of CER on the contact resistance and the saturation current when CER causes the change of the S/D contact area, according to the rms roughness of CER at the best lithography process condition. As mentioned in Sec. 1, when the 3σ roughness of CER is 4 nm, the S/D contact area variation is as much as 10% in our 32-nm contact manufacturing. This is because CER affects the contact shape, which causes great change in the S/D contact area. Thus, we assume that the higher CER causes the larger contact area variation, which is linearly proportional to the rms CER. The result presents that the variation of the S/D contact resistance and the saturation current are up to 57.8 and 2.12%, respectively, where the rms CER value is 10 nm. Meanwhile, the average value of the resistance is slightly increased, and the trend of the saturation current is slightly decreased. Compared with the results of Fig. 10, the resistance and saturation current of the S/D contact are more than doubled. As a result, if designers want to keep the worst-case S/D contact resistance within 30% from the typical resistance value, more than 5-nm CER should be avoided for the 32-nm standard cell library at the best lithography condition.

Figure 12 shows the impact of CER on the contact resistance and the saturation current when we consider random CER variation as well as systematic lithography variation, e.g., focus, dose, etc., because both random CER and systematic lithography variation cause contact area variation, and hence device performance variation. The result shows as much as 135.7% increase of the S/D contact resistance and 4.9% decrease of the saturation current at the worst process corner. When compared with Fig. 11, the worst-case resistance increases as much as 77.9% and the worst-case saturation current decreases 2.78%, respectively. In other words, the portion of random CER among the total variation is around 43% in 32-nm node standard cells. In these experiments, we assume that random CER is independent of systematic lithography variation. However, according to Ref. 32, the rms magnitude of LER is highly related to image log slope, which implies that CER could be highly related with systematic lithography variation. We will study further the correlation between random CER and systematic lithography variation for future work.

Table 2 reports the impact of CER on the S/D contact resistance and saturation current. In a conventional approach that just considers the contact area variation due to CER, the

Table 2 Impact of CER on S/D resistance and device saturation current. Conventional, when the area variation of the S/D contact is the only factor of the contact model. Weighted CER, when the position, shape, and area weighting factors are considered in the circular contact layout extraction (Fig. 10). Noncircular CER, when CER causes the area change of the S/D noncircular contact, which is linearly proportional to the rms CER value (Fig. 11). CER plus process, when both the systematic lithographic process and random CER are considered (Fig. 12).

	Conventional	Weighted CER	Noncircular CER	CER + Process
ΔR_{ds} at CER 4 nm	6.2%	9.4%	20.5%	93.8%
ΔR_{ds} at CER 10 nm	17.3%	24.5%	57.8%	135.7%
ΔI_{ds} at CER 4 nm	0.23%	0.34%	0.74%	3.52%
ΔI_{ds} at CER 10 nm	0.63%	0.88%	2.12%	4.90%

impact on device saturation current is around 0.5%. When we consider the position, shape, and area weighting factors in the contact layout extraction, the impact of CER is a little bit increased, yet less than 1.0%. Those two results assume that CER is generated on the circular-type contact, where the mean contact area does not change, as shown in Fig. 9(a). Meanwhile, when we assume that CER induces noncircular contact shapes, as shown in Fig. 9(b), the impact of CER is highly increased: more than 2% of saturation current and around 60% of contact resistance. When both systematic and random CER variation occur on S/D contacts, the impact of contact variation results in as much as 135% of contact resistance and around 5% of saturation current. 5% decrease of the saturation current due to S/D contact variation is equivalent to about 8% increase of the effective gate length.[6,7] Thus, the optimization of the S/D contacts in standard cells can minimize the contact variation due to random CER and systematic lithography variation.[30]

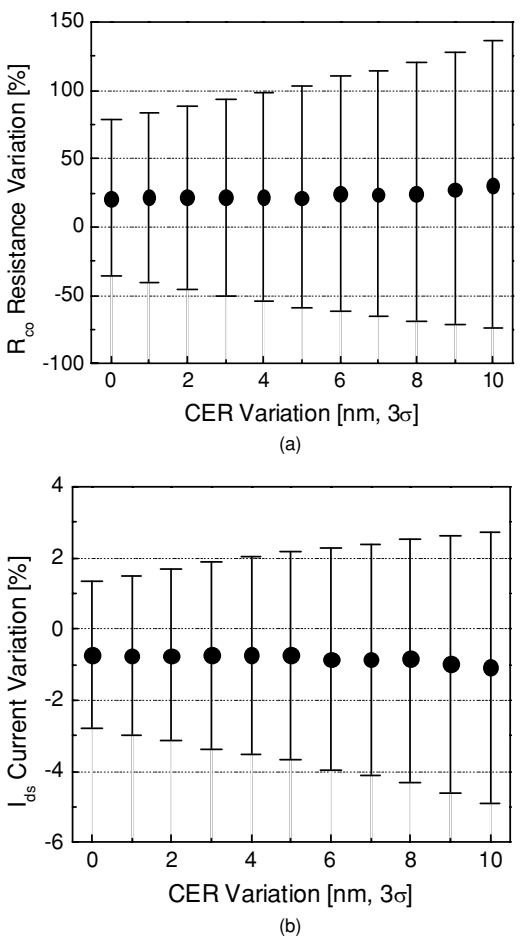

Fig. 12 The impact of CER on (a) the contact resistance and (b) the saturation current when we consider the best ($+3\sigma$) and the worst (-3σ) lithographic process corners.

6 Conclusion

We propose a CER model and a new S/D contact extraction model to electrically analyze S/D contact with CER. Our contact extraction model is based on the contact shape and displacement weighting factor, and is well matched with a rigorous TCAD simulation. Experimental results show that the portion of the random CER in parametric variation is considerable in sub-32-nm standard cells. We believe a flow that is capable of characterizing CER variability will demonstrate significant advantages in terms of understanding the impact of CER and improving systematic and parametric yields as a result of reducing design-to-manufacturing miscorrelations.

Acknowledgments

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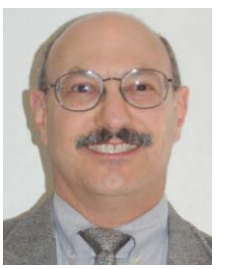

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