Modeling of Layout Aware Line-Edge Roughness and Poly Optimization for Leakage Minimization

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***Abstract*—Line-edge roughness (LER) highly affects the device saturation current and leakage current, which leads to serious device performance degradation. In this paper, we propose the first layout-aware LER model where LER is highly related to the lithographic aerial image fidelity and neighboring geometric proximity. With our new LER model, we perform robust LER aware poly layout optimization to minimize the degradation of device performance, in particular leakage current. The results on 32-nm node standard cells show average 91.26% reduction of leakage current and 4.46% improvement of saturation current at the worst case process corner despite 8.86% area penalty.**

***Index Terms*—Design for manufacturing, layout optimization, leakage, line-edge roughness (LER), lithographic variation, VLSI design.**

I. Introduction

As SEMICONDUCTOR device nodes continue to shrink down to 32 nm and below, the complexity of designs is significantly increasing due to process variation. Among sources of process variation, lithographic printability variation is one of the most fundamental challenges because it directly impacts on yield and performance. Despite of advances in resolution-enhancement techniques (RET) such as optical proximity correction (OPC), phase-shifting mask (PSM), off-axis illumination (OAI), etc., lithographic variation still continues to be a challenge [1]. Two types of lithography variations which result in undesirable performance mismatch in identically designed transistor are: 1) *systematic lithography variation* and 2) *random lithography variation*.

The systematic lithography variation is introduced due to deterministic pattern proximity by the limitation of the lithography equipment where 193-nm wavelength are still used even for sub-32-nm technology nodes. Layout geometries such as neighboring gates, convex and concave corners, jogs, and line-ends result in the systematic variation. To address the problem of systematic lithography variation from a design perspective, several authors have proposed lithography-aware characterization methods [2]–[4]. In [2], the authors proposed a gate slicing and effective gate length (EGL) method to calculate the impact of nonrectangular gate shapes. Another work [3] proposed a modeling card to combine different EGLs from look-up tables of driving current and leakage current.

The second type of lithography variation is caused by random uncertainties in the fabrication process such as line-edge roughness (LER). At the same time, many nonlithographic sources of variation such as dopant variation [5], [6] and gate dielectric thickness (T_{ox}) variation [7], [8] are also the result of aggressive scaling. Among them, LER was regarded as a small fraction of the statistical variability in the past since the critical dimensions (CD) of MOSFET was much larger than LER. However, as the aggressive scaling continues into the nanometer regime, LER does not scale accordingly and becomes an increasingly larger fraction of the gate length [9], [10]. For channel lengths above 32 nm the random dopants are the dominant source of fluctuations, but below this channel length LER takes over and becomes a major fluctuation source [7]. Thus it can be one of the performance limiting components for technologies 32 nm and below.

LER is mainly caused by erosion of polymer aggregates at the edge of photo-resist (PR) during development process [11]. To address LER impact, many works have been proposed in a simulation manner [12]–[15]. The work of [6] and [16] presented the impact of LER on the variation of threshold voltage with statistical timing analysis. Even if many works on LER modeling have been performed, these works have been focusing on process level and unit device level simulation. According to our experiments, LER is highly related to lithography image fidelity which is mainly driven by lithography process and layout proximity. Since each device in a cell might have different LER due to different layout proximity, there is great demand to study on a cell level LER model which considers neighboring pattern proximity due to lithography to analyze the impact of LER on circuit performance, in particular leakage current.

Standard cells are pervasively used in digital designs as basic circuit blocks. Since a large amount of identical cells will be used repeatedly, any small changes to reduce gate length variation in standard cells can result in significant improvements at the design level [17]. There are a lot of layout patterns in a standard cell, and each pattern may have a different patterning fidelity and different LER impact. Thus a new LER model considering both aerial image fidelity and neighboring pattern proximity is required.

In this paper, we propose a LER-aware layout optimization to minimize leakage current in a cell. Our approach is mainly based

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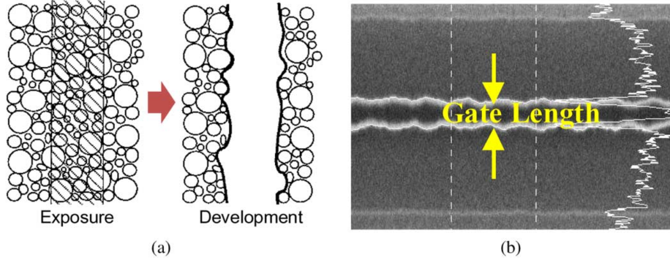

Fig. 1. Random LER lithography variation. (a) LER generation [18]. (b) SEM of gate LER [9].

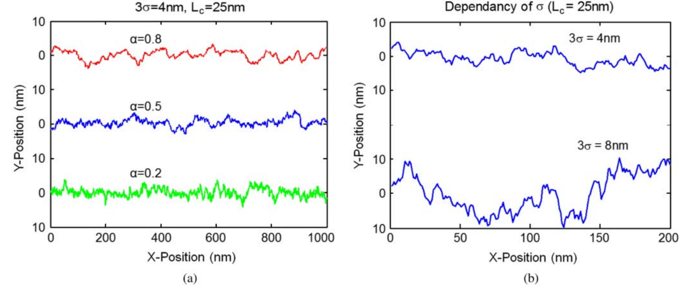

Fig. 2. Demonstration of LER with α and σ. (a) LER simulation with α. (b) LER simulation with σ.

on a new LER model where the root mean square (rms) roughness of LER depends on layout proximity in lithography. The objective of the proposed optimizations is to enhance standard cell layouts for improved parametric yield and reduced LER variations with minimal or no penalty on area constraints. The major contributions of this paper include the following.

- This is the first study on a layout dependent LER model which is a function of neighboring patterns and image fidelity. The idea is based on the fact that different gates might have different LER values due to pattern proximity and lithography process variation.
- We analyze the impact of LER on both device saturation current and leakage current in a standard cell. In particular, leakage current dramatically increases as LER increases. A nonrectangular gate extraction approach is used for calculating the effective gate length due to LER and lithography proximity, meanwhile each gate could have a different effective gate length due to LER.
- We propose poly layout optimization by considering LER in a standard cell in an early design stage. Since the relationship between LER and layout proximity shows a convex form, we find a globally optimal design where the layout is robust from LER, lithography process variation, and even circuit performance variation.

The rest of the paper is organized as follows. Section II describes a LER model and its impact on device currents. Section III presents the layout dependent LER model. Section IV proposes the formulation and algorithm of the poly layout optimization. Experimental results are shown in Section V, followed by conclusions in Section VI.

II. Preliminary of LER

A. Modeling of LER

LER, one of the dominant random variations, is caused by the interaction of light and thermal bombardment with the molecular nature of photoresist materials in the acid generation, the acid diffusion and development process in chemically amplified resists (CAR) [18], [19] in Fig. 1(a). As shown in Fig. 1(b), the severe CD variation is evolved at the line edges even if the line structure in layout is straight. LER is a random fluctuation in the gate length and has influence on both edges of the gate.

LER is often expressed by the power spectral density (PSD) which is theoretically the Fourier transform of the autocorrelation function [12], [13], [20], [21]. Let us define $z(x)$ as a one-dimensional distribution of edge locations. PSD, $S(f)$, is mathematically defined as

$$S(f) = \lim_{L\to\infty} \frac{1}{L} \left| \int_{-L/2}^{L/2} z(x)\exp(2\pi i f x)dx \right|^2. \quad (1)$$

Therefore the autocorrelation function of $z(x)$, $R(\tau)$, is formulated as

$$R(\tau) = \mathbb{F}^{-1}\{S(f)\} = \lim_{L\to\infty} \frac{1}{L} \int_{-L/2}^{L/2} z^*(x)\cdot z(x+\tau)dx. \quad (2)$$

The rms roughness, σ, is often defined in terms of $z(x)$ as

$$\sigma^2 = \lim_{L\to\infty} \frac{1}{L} \int_{-\infty}^{\infty} |z(x)|^2 dx = 2\int_{0}^{\infty} S(f)df. \quad (3)$$

Thus the autocorrelation function, $R(\tau)$, follows an exponential function by the distance r for line edge as the following:

$$R(r) = \sigma^2 \exp^{-\left(\frac{r}{L_c}\right)^{2\alpha}} \quad (4)$$

where L_c is the correlation length, σ is the standard deviation of line edge, and α is related to the fractal dimension D ($\alpha = 2 - D$). Therefore, PSD is approximated as the following equation [12]:

$$S(k) = \frac{2\sigma^2 L_c}{(1 + k^2 L_c^2)^{0.5+\alpha}} \quad (5)$$

where $k = 2\pi f$, $f = i(1/N\Delta z)$, and $0 \le i \le (N/2)$, N is the number of points along the line. Hence, the LER for a large number of resists can be characterized by three numbers, σ, L_c, and α. With the magnitude information provided by $S(k)$, we can reconstruct random line edges by applying a random phase to each frequency component of the PSD to form a unique signal in the frequency domain. A line edge with roughness can be simulated by doing an inverse Fourier transform of this signal.

Fig. 2(a) shows LER profiles from (5), with $L_c = 25$ nm, $3\sigma = 4$ nm and $\Delta z = 1$ nm at three different values for α of 0.2, 0.5, and 0.8. α is related to the high-frequency fluctuations of LER [12]. Higher α shows less high-frequency fluctuation and smoother line edge, whereas the lower α signifies more high-frequency fluctuation and rough line edge. Meanwhile σ, rms

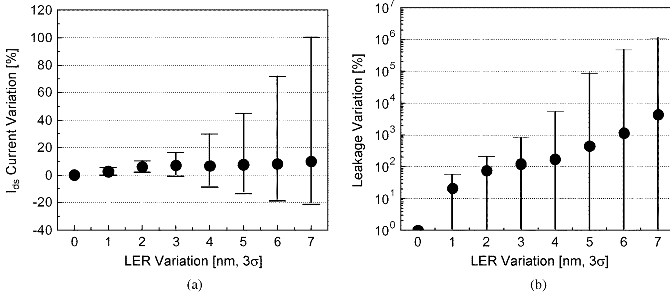

Fig. 3. LER impact on $I_{\rm on}$ and $I_{\rm off}$. (a) LER impact on $I_{\rm on}$. (b) LER impact on $I_{\rm off}$.

TABLE I
EFFECTIVE GATE LENGTH $L_{\rm eff}$ DUE TO LER

LER	L_{eff} for I_{on}			L_{eff} for I_{off}		
	$+3\sigma$	nominal	-3σ	$+3\sigma$	nominal	-3σ
0		30.00			30.00	
2	29.74	29.28	28.81	29.94	29.30	28.67
4	31.22	29.20	27.18	31.27	28.81	26.35
5	31.96	29.10	26.25	31.83	28.11	24.40
7	33.60	28.86	24.11	32.50	26.50	20.51

amplitude, is the most important parameter for LER. Fig. 2(b) shows two simulated roughness profiles with different values of σ. σ corresponds to the transversal magnitude to the line, and the larger σ shows greater roughness of the line. Among the major LER parameters, L_c and α are highly dependent on the photoresist type and relatively less critical than σ [20]. Thus in this paper we are focusing on presenting LER with regard to σ.

B. Impact of LER on Device Currents

Based on (5), we directly generated LER on a gate line and investigated device saturation current and leakage current variation with the amount of LER in a 32-nm inverter cell. Fig. 3(a) shows the impact of LER on saturation current of a conventional NMOS device. The black circled dot represents the average of the variation, and the small bars show the upper and lower bound of the variation. The upper and lower bound are equivalent to $+3\sigma$ and -3σ from the nominal value. As shown in the result of saturation current, the deviation between the upper bound and the lower bound is highly increased as LER increases while the average values are slightly increased.

The impact of LER on gate leakage current is much more critical than that of saturation current as shown in Fig. 3(b). As LER increase, both the upper bound and the average leakage current are dramatically increased. Table I shows why the average current due to LER is slightly increased for $I_{\rm on}$ and exponentially escalated for $I_{\rm off}$. As LER increases the nominal effective gate length, $L_{\rm eff}$, for saturation current becomes smaller which makes the nominal $I_{\rm on}$ slightly larger. Meanwhile, the $L_{\rm eff}$ for leakage current is more highly decreased, and the $L_{\rm eff}$ deviation for leakage current is also much wider than the $L_{\rm eff}$ of saturation current. For example, when the rms 3σ LER is 7 nm, the standard deviation, σ, of on-current $L_{\rm eff}$ is 1.45 nm while the σ of off-current $L_{\rm eff}$ is 2.07 nm. Fig. 3 reveals that when the rms LER value is 7 nm from its gate edge, the worst case saturation current and leakage current are as much as 100% and more than ten thousand times compared to the nominal current, respectively.

C. Our Contributions

Leakage power is a significant portion of the total power consumed in sub-30 nm devices. Moreover, leakage is one of the critical factors which prevent semiconductor devices from continuously shrinking. As shown in the results of Fig. 3, small LER on gate causes huge amount of leakage current. In other words, small improvement of gate LER can greatly reduce leakage current. This illustrates that the poly layout optimization by considering the impact of LER on devices current, in particular leakage current is crucial for sub-32-nm node devices. Even though the final OPC stage might also reduce any trivial LER variation, we can significantly minimize the impact of LER at the early design stage.

Even though a conventional LER model generates a physically meaning edge shape, it does not describe any dependency of neighboring pattern proximity. In a standard cell, there are a lot of patterns having various aerial image contrasts. Even in a single line, LER might be different with regard to layout positions where aerial image quality could be nonidentical. In order to analyze the impact of LER on device performance, we should use a layout dependent LER model which considers both aerial image fidelity and neighboring pattern proximity.

Our goal in this paper is: 1) to propose a new LER model which considers both neighboring pattern proximity and lithography process robustness; 2) to optimize poly layouts by minimizing the total amount of LER in an early design stage; and 3) to eventually reduce device leakage current in a cell. To the best of our knowledge, our work is the first attempt to abstract out the impact of LER from the process simulation realm into the gate level and to apply the new LER model to poly layout optimization for leakage minimization.

III. LAYOUT DEPENDENT LER MODEL

LER is a strong function of aerial image quality because a higher aerial image contrast results in a smaller transition region in photo-resist (PR) polymer dissolution behavior [14]. It implies that LER does not always follow random characteristic while it can be modeled in a systematic approach. ILS (*image log-slope*) is a single metric which is capable of explaining aerial image quality due to lithography proximity such as pitch, line width, exposure dose, focus, and so on.

The slope of the aerial image intensity, I, as a function of position, x, measures the steepness of the image in the transition from bright to dark of aerial image light as shown in Fig. 4. To be useful it must be normalized to the threshold aerial image ($I_{\rm th}$) which is the image intensity at the desired level. Dividing the slope by the intensity will normalize out this effect. ILS is defined as follows:

$$\text{ILS} = \frac{1}{I_{\rm th}}\frac{dI}{dx} = \frac{dln(I)}{dx} \qquad (6)$$

where ILS is measured at the nominal line edge as shown in Fig. 4. The higher ILS means the better image fidelity. ILS is used to evaluate the lithographic usefulness of an aerial image [22]. That is because ILS directly represents an aerial

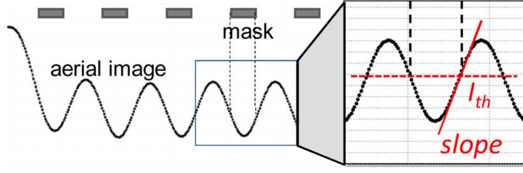

Fig. 4. Illustration of ILS (image log-slope).

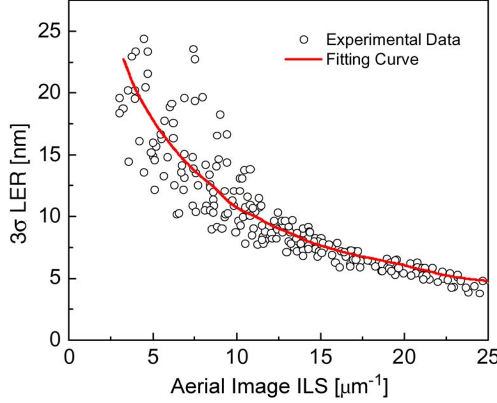

Fig. 5. Relation between LER and ILS (data from [23]).

image fidelity. According to [23], the rms magnitude of LER is highly related to ILS as shown in Fig. 5. As ILS decreases, the magnitude of LER increases. In the same way, LER decreases and becomes saturated to a certain level as ILS increases. The LER trend might vary due to lithography process conditions. The point is that LER is a strong function of image fidelity in lithography.

Thus we characterize the resulting LER as a function of ILS of the aerial image by sweeping the pitch of gate poly from 80 to 230 nm. Note that the nominal gate pitch is usually three or four times larger than the gate length in a standard cell layout. Since the nominal gate length (≈ CD of polyline) in our design is 30 nm, 80-nm poly pitch means 50-nm space between two poly lines. We used Calibre–Workbench to get ILS values for various poly pitches [24]. Our optical parameters are wavelength $(\lambda) = 193$ nm, numerical aperture $(\mathrm{NA}) = 1.25$ immersion lithography, and dipole unpolarized illumination $\sigma = 0.9/0.7$. The thickness of PR is 150 nm.

As shown in Fig. 6, as the poly-to-poly space increases, ILS is larger and has a zenith at around 100 nm space, then the value of ILS is decreased. This is because at the dense pitch (≈ smaller space) the aerial image is distorted due to approaching the lithography resolution limit. Meanwhile at the sparse region (≈ larger space) the aerial image is also degraded due to the neighboring light proximity. That is the reason that sub-resolution assist features (SRAF) are used for sparse patterns to prevent from degrading aerial image in an industrial lithography process. Another observation in Fig. 6 is that as ILS increases, the layout is less affected from lithography process variation, which implies that the pitch having the minimum LER is more robust from process variation.

From the results of Figs. 5 and 6, we can get the relationship between the rms magnitude of LER and poly space as shown

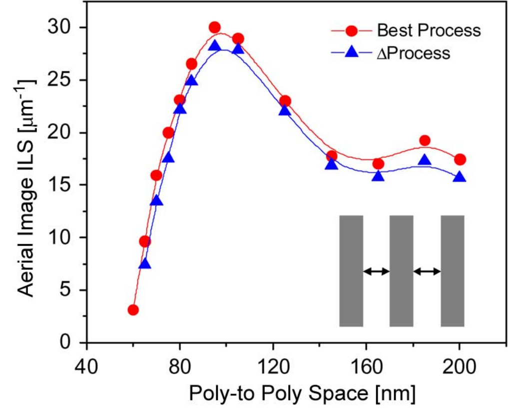

Fig. 6. Relation between ILS and Pitch.

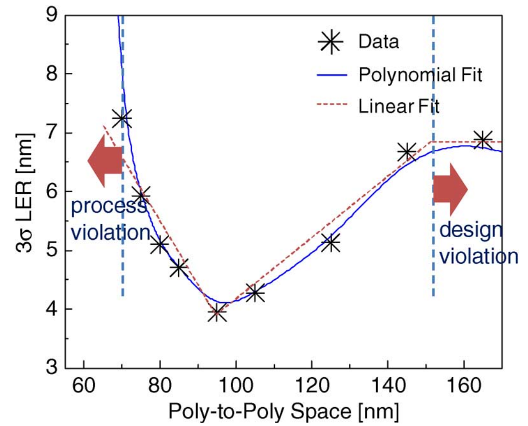

Fig. 7. Relation between LER and Pitch.

in Fig. 7. Since the rms roughness, σ, is represented as a polynomial function or a piece-wise linear function which considers the impact of pattern pitch on lithography process, we can get a new PSD function which takes the neighboring pattern pitch into consideration as

$$S(k) = \frac{2\sigma(x)^2 L_c}{(1+k^2L_c^2)^{0.5+\alpha}}$$

where

$$\sigma(x) = \sum_{i=0}^{N} a_i x^i, \quad i = 0, \ldots, N$$

or

$$\sigma(x) = \begin{cases} -\alpha_1 \cdot x + \beta_1, & \text{if } x \le x_{p1} \\ \alpha_2 \cdot x - \beta_2, & \text{if } x \ge x_{p1} \\ \beta_3, & \text{if } x \ge x_{p2} \end{cases}$$
$$x > \mathcal{P}, \text{where } \mathcal{P} \text{ is process violation}$$
$$x < \mathcal{D}, \text{where } \mathcal{D} \text{ is design violation} \qquad (7)$$

where N is a nonnegative integer, x is a distance variable of poly space, x_{p1} is a position where LER has the minimum value, x_{p2} is a position where LER becomes saturated, a_i is a fitting parameter for a polynomial function and α and β are fitting parameters for a piecewise-linear function. The constraint of x is

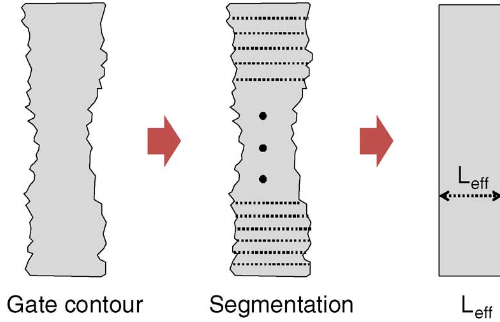

Fig. 8. Nonrectangular gate extraction.

to keep the poly-to-poly space x to be within given process tolerance $\mathcal{P}$ and layout design tolerance $\mathcal{D}$. The process tolerance, $\mathcal{P}$, defines the limitation of lithography patterning for poly layer. In other words, we can not get a proper gate patterning image below a certain pitch of poly. Meanwhile the design tolerance, $\mathcal{D}$, is defined by the maximal allowable pitch of poly lines which represents the area constraints of a cell. It are defined in an early design stage based on required drive strength and design specification. Thus a poly space beyond a certain design tolerance is not allowed in a standard cell.

The space of poly lines in a standard cell might differ from the neighboring pattern. Moreover a gate line might suffer from severe LER due to complex pattern proximity which should be considered at the layout optimization step. By calculating the polygon space of poly lines, we can get the rms amount of LER on poly edges which is directly implemented into printed images for gates in a cell.

We extract the effective gate length for nonrectangular gates having LER noise using a gate segmentation technique [2], [3], [15]. To extract the print-image, we first construct lookup tables for on-current (I_{on}) and off current (I_{off}) which are obtained using H-Spice simulation tool [25]. Next, as shown in Fig. 8, we segment the gate region by a set of equal width rectangular polygons. The device current for each segment is computed using the nominal current from the rectangular device. The equivalent or total current for the gate region is computed by summing all these segment currents. From the total current of the nonrectangular gate, we can get the equivalent gate lengths which are used for calculating the driving current and the leakage current in a cell.

IV. LER-Aware Poly Optimization

A. Problem Definition

Since the minimum pitch of poly layer has been approaching the theoretical resolution limit, the poly layer is usually drawn with simple one dimensional line and space (L/S) type *regular design approach* for sub-32-nm node design [26], [27]. Then the poly layout optimization is performed by identifying opportunities to enforce as many recommended design rules (RDR) as practically feasible. Since the poly layout is formed with a straight L/S type, the poly layer does not seem likely to show any systematic lithography variation due to its simplicity. However we could see large LER even in a simple L/S type poly pattering because the current RDR usually does not consider the impact of LER despite its criticality and because each transistor in a cell might have a different pitch and LER.

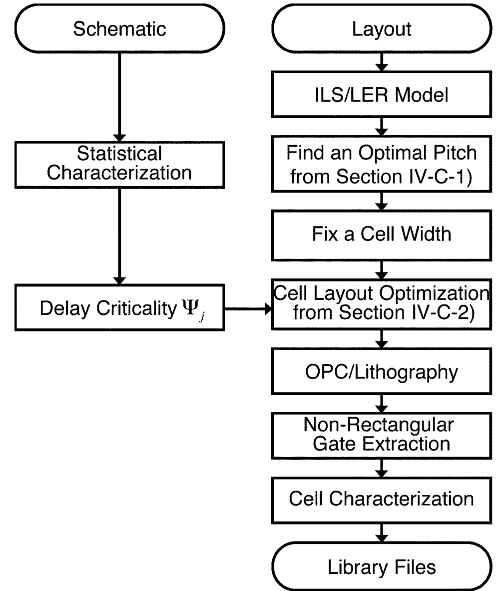

Fig. 9. LER-aware cell optimization flow.

Let us revisit the goal of poly layout optimization for standard cells—the basic objective is to improve parametric yield or reducing systematic variability in cell current and leakage power. Our layout optimization is done in an early design stage rather than at the final mask synthesis step. As we mentioned in Section I, the impact of LER has highly increased below 32-nm node. Thus, it is required to reflect lithographic LER in the design stage. Consequently, there are three issues with the current poly layout optimization approach for standard cells.

- Design rules are applied to all devices and all layers without any consideration of the impact of LER.
- There is no good mechanism of LER to quantify the improvement due to optimization of the standard cells in terms of its performance.
- It is difficult to quantify the impact of LER on device performance, in particular current and leakage power.

As we mentioned at Section II-B, since LER highly degrades device leakage current, consideration of LER at design stage is crucial for sub-30-nm node design.

B. LER-Aware Optimization Flow

Fig. 9 illustrates the flow of our LER-aware poly layout optimization. The flow is mainly divided into three steps.

1) **Define Cell Width**: In order to optimize drawn cell layouts at the design stage, we first calculate the optimum poly pitch for minimum LER value which is used for a cell design as a base-line pitch. Then, we define the cell width by multiplying by the optimum pitch and the number of poly grid lines. The dummy poly lines are placed on the left and right edges of a cell to reduce the gate proximity from neighboring cells.
2) **Assign Device Criticality**: The devices within a cell can be ranked based on their sensitivity contribution because

different transistors have inherently different performance sensitivity to the same amount of gate length variation due to LER [28].

3) **Minimize LER**: Despite finding an optimal pitch, some poly lines might have different neighboring geometry due to detoured poly lines, contact alignment, etc. Thus, we finely optimize the poly lines by minimizing the total weighted amount of LER in a cell. Since LER polynomial shows a convex shape within a design tolerance, we can get the globally optimal positions of the devices in a cell.

C. Formulation and Algorithm

1) Find an Optimal Poly Pitch: As shown in Fig. 7, the rms magnitude of LER is highly dependant on poly layout pitch. Although the input optical conditions for poly patterning might be different from poly design and devices specification, the poly patterning generally shows a trend in which the ILS of aerial image has the maximal value, as shown in Fig. 6, and in which the poly layout is the most robust from the lithography process variation. Therefore, from the results of Fig. 7, we can mathematically formulate an optimal pitch of poly lines with *the minimal LER impact* as follows:

$$\mathbf{min}: \quad \sigma(x_L) + \sigma(x_R)$$

where

$$\sigma(x) = \sum_{i=0}^{N} a_i x^i, \; i = 0, \ldots, N \tag{8}$$

where $\sigma(x_L)$ is the rms roughness of the left edge (x_L) of a line, and $\sigma(x_R)$ is one of the right edge (x_L). The rms roughness $(\sigma(x))$ of a line edge is formulated by an Nth-order polynomial function as shown in (7). Since the distances from both left and right poly are same, both line edges usually have a same amount of LER value.

The objective is to minimize rms edge roughness on both the left and right edge of a line. In this formulation, we assume that there is a globally optimized pitch within process and design constraints as shown in Fig. 7. These assumptions are reasonable because of the following two reasons: 1) the LER trend has a remarkable global minimum and then it is saturated for large pitch; 2) furthermore all other local minimal points can be ignored due to area design constraint. Thus the LER polynomial shows a convex shape within allowable process and design constraints. Due to the convexity, we can obtain the globally optimal position of gate poly layer for minimal leakage current.

As shown in Fig. 10, we can minimize LER impact on poly layer by using our poly layout optimization. By optimizing the poly layout, we can get smaller LER on gate patterning despite cell area penalty. Poly optimization does not always increase the poly pitch, whereas certain poly pitches in a cell can be decreased for a minimal LER magnitude.

The changed poly pitch might vary the poly printed image, and device's channel stress and performance. If optimal poly pitch is smaller than the original design, the cell area could be reduced. Yet, its reduced poly pitch may affect the device's channel stress which might degrade the devices performance [29]. However, the optimal poly pitch is found at the best position where poly patterning shows the most robust on lithography process, which compensate the device saturation current degradation by improving gate LER value. Meanwhile if optimal poly pitch is larger than the original pitch, the cell area might be increased, which, however, enhances device's channel stress on dual stress liner [29], [30]. Most of all, even though there happens small degradation on the device saturation current due to the optimization of poly pitch, the leakage current is highly decreased for both cases because small reduction of LER induces huge amount of leakage improvement.

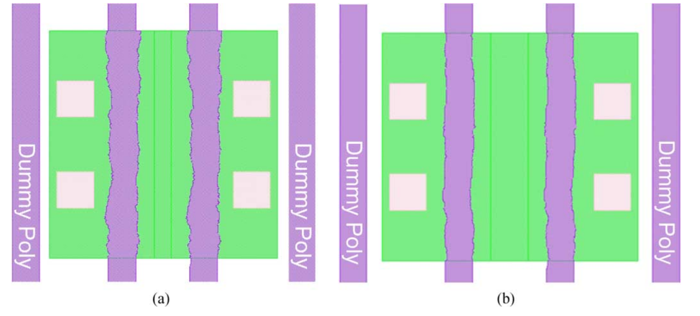

Fig. 10. Pitch optimization to minimize LER. (a) LER 3σ 6 nm; (b) LER 3σ 4 nm.

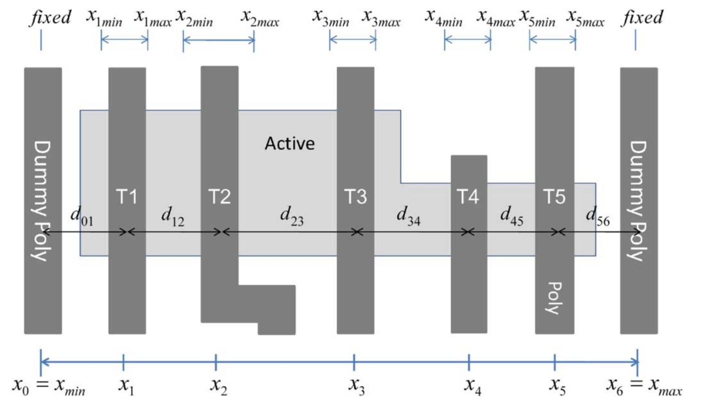

Fig. 11. LER aware poly layout optimization in a standard cell.

2) Cell Layout Optimization: Generally in a standard cell there are several transistors, as shown in Fig. 11. Since the position of each transistor correlates neighboring transistors, we should find the optimal positions for all transistors in order to minimize LER. Let T be the set of geometrically coupled transistors (indexed by j), x_j be the x-directional position in a cell. The optimization for x_j can be done as shown in (9) where the objective is to minimize the total amount of LER by finding the optimal positions of all transistors in T. Note that the cell width (W_{cell}) is first defined based on the optimal pitch information from the result of (8); the position of dummy poly lines are fixed,

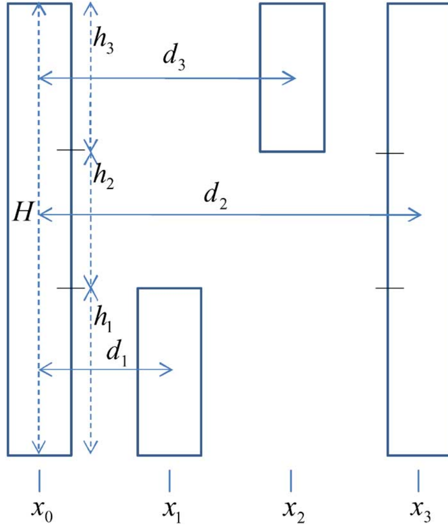

Fig. 12. LER calculation for neighboring proximity.

and the all transistors are just allowed to change their position within design tolerance from $x_{j_{\min}}$ to $x_{j_{\max}}$

$$\textbf{min}: \quad \sum_{j=1}^{M} \Psi_j \left\{\sigma(x_L) + \sigma(x_R)\right\}_j | \quad \forall j \in T$$

where

$$\begin{aligned}
&\sigma(x_{L,j}) = \sum_{i=0}^{N} a_i (d_{L,j})^i \quad \forall j \in T \\
&\qquad \sigma(x_{R,j}) = \sum_{i=0}^{N} a_i (d_{R,j})^i \quad \forall j \in T \\
&\qquad d_{L,j} = x_j - x_{j-n} \\
&\qquad d_{R,j} = x_{j+n} - x_j \\
\textbf{s.t.}: &\qquad x_{j_{\min}} \le x_j \le x_{j_{\max}} \quad \forall j \in T \\
&\qquad x_{\max} - x_{\min} = W_{\text{cell}}
\end{aligned} \tag{9}$$

where n is a positive integer, $d_{L,j}$ and $d_{R,j}$ are distances from the edge of the jth poly line to poly lines located in the left and right side, respectively. Ψ_j is a device criticality of jth transistor to gate length variation in a cell.

As a general principle, the current and delay variation is different from the input timing arcs. Some devices have significant impact on falling arcs while the other devices have significant impact on rising arcs. It implies that each transistor has different delay sensitivity due to gate length variation, in particular LER. Therefore, we should ensure that highly sensitive devices from gate length variation due to LER be given higher priority during layout optimization while less sensitive devices can allow relatively larger amount of LER. The devices within a cell can be ranked based on their sensitivity contributions to the cell's delay sensitivity [28].

Since every transistor might have difference proximity due to neighboring patterns, we should consider the impact of neighboring patterns in a cell. As shown in Fig. 12, to take the neighboring proximity into account we divided an edge into multiple segments, which is similar to a method of a conventional model-based OPC. Thus each segment might have different LER due to the distances of the neighboring patterns. Assume as shown in Fig. 12 where a gate edge consists of three segments, S_1, S_2, and S_3, their heights and distance from neighboring patterns are h_1, h_2, h_3 and d_1, d_2, d_3, respectively.

The LER contributions of three segments in a polynomial-type LER function are given by the following equations:

$$\sigma_j(x) = \sum_{i=0}^{N} a_i d_j^i = \sum_{i=0}^{N} a_i (x_j - x_0)^i \,|_{j=1,2,3}. \tag{10}$$

Since the total LER contribution on an edge of a gate is defined by the average of all contributions of segments, the effective LER value on a gate edge is as follows:

$$\sigma(x) = \frac{h_1}{H}\sigma_1(x) + \frac{h_2}{H}\sigma_2(x) + \frac{h_3}{H}\sigma_3(x) \tag{11}$$

where H is the total gate height. Generally, if there are P number of segments in an edge, we can calculate the LER value of the edge as follows:

$$\begin{aligned}
\sigma(x) &= \frac{1}{H}\left\{h_1 \cdot \sum_{i=0}^{N} a_i d_1^i + \ldots + h_P \cdot \sum_{i=0}^{N} a_i d_P^i\right\} \\
&= \sum_{i=0}^{N} \frac{a_i}{H}\left\{h_1 \cdot d_1^i + h_2 \cdot d_2^i + \ldots + h_P \cdot d_P^i\right\}
\end{aligned} \tag{12}$$

where all d_Ps are distances from the edge of a jth gate, which can be represented by x_j positions.

If we fit the relationship between LER and poly pitch with a piece-wise linear model, (12) should be shown with a simpler linear function in terms of position, x_j. Even though a conventional polynomial function can have a lot of local minimum according to the index, the LER trend fitted form of the experimental data usually has a global minimum within a certain design range. Since the rms edge roughness shows a convex form or a simple linear form given poly space and the total LER is a linear sum of the LER of all gates, we can find the optimal position of each transistor in a cell in a polynomial time.[1]

We describe our LER-aware layout optimization in Algorithm 1. The inputs are a set of standard cells, lithography conditions, and device criticality which is predefined at the circuit level cell characterization. Then, as in line 3, we first define the optimal poly pitch where LER on poly line shows a minimal value. Based on the result of the poly pitch, a cell width is fixed in line 5. Dummy poly lines are also placed at both sides of a cell to prevent boundary poly lines from interferences of neighboring cells in line 6. Then, as in line 12–14 we calculate the amount of LER of each gate by considering neighboring pattern proximity which is multiplied with the factor of device criticality. Finally, as in line 16 we find optimal positions of all transistors using a convex/linear optimization. After separately optimizing the position of NMOS and PMOS devices, we reroute the poly line to connect between NMOS and PMOS devices.

[1]http://www.gurobi.com/

TABLE II
IMPROVEMENT OF I_{on} SATURATION CURRENT

Cell	Before Optimization (α)			After Optimization (β)			Improve (β:α)(%)[c]			Area
	Best (A)	Norm (A)	Worst (A)	Best (A)	Norm (A)	Worst (A)	Best[a]	Norm[a]	Worst[b]	%
INV	3.59E-04	2.95E-04	2.39E-04	3.56E-04	2.93E-04	2.50E-04	-0.78	-0.71	4.81	7.60
NAND2	1.85E-04	1.54E-04	1.26E-04	1.84E-04	1.53E-04	1.32E-04	-0.70	-0.65	4.60	8.55
NAND3	1.23E-04	1.03E-04	8.52E-05	1.22E-04	1.02E-04	8.90E-05	-0.73	-0.58	4.39	9.12
NOR2	7.17E-04	5.89E-04	4.78E-04	7.12E-04	5.85E-04	5.01E-04	-0.78	-0.68	4.84	8.55
NOR3	1.08E-03	8.84E-04	7.17E-04	1.07E-03	8.78E-04	7.51E-04	-0.74	-0.69	4.83	9.12
MUX2	5.62E-05	1.99E-05	1.30E-05	4.54E-05	1.97E-05	1.35E-05	-19.33	-1.16	3.30	10.20
average							-3.84	-0.75	4.46	8.86

[a] We measured the current improvement of the after optimization. Negative value corresponds to the decreased saturation current. The smaller current denotes the better variation at the best process corner.
[b] Positive value represents an increased current from the current of the before optimization. The larger current means the better variation at the worst process corner.
[c] Overall we reduced the current variation between $+3\sigma$ and -3σ corners. The improvement of the saturation current from LER-aware layout optimization is not so big in the entire cases.

Algorithm 1 LER-aware Poly Optimization

1: **Require:** A set of standard cells ($cell$), lithography inputs ($litho$), and device criticality (Ψ)
2: Read $litho$ and minimum poly length
3: Find an optimal pitch for poly lines from Eq. (8)
4: **for** each $cell\ C \in$ Library **do**
5: Repositioning of poly lines
6: Insertion of dummy poly lines
7: $gate = poly \cap active$
8: $nmos = gate \cap nwell$
9: $pmos = gate - nmos$
10: convex/linear form $f(x) \leftarrow 0$
11: **for** each $nmos\ N \in C$ **do**
12: LER function ($\sigma(x)$) for each device from Eq. (12)
13: Multiplying Ψ
14: $f(x) += \Psi \times \sigma(x)$
15: **end for**
16: $nmos$ optimization from Eq. (9)
17: **for** each $pmos\ P \in C$ **do**
18: Same sequence as $nmos$
19: **end for**
20: $pmos$ optimization from Eq. (9)
23: Poly re-routing between $nmos$ and $pmos$
22: **end for**

V. EXPERIMENTAL RESULTS

We implemented LER on gate printed images and the poly layout optimization in Tcl and Perl script language and tested with Nangate 45 nm open cell library [31]. To apply to 32-nm standard cell, we shrank 45-nm node standard cell library into 32-nm dimension where the poly-to-poly pitch is 190 nm for the 45-nm original cells and 114 nm for the 32-nm shrunken cells, respectively. Furthermore we put dummy poly lines beside the main poly to prevent the poly patterning from the proximity of neighboring cells as industrial cells are adopted for 32-nm node logic design [32]. The nominal gate length is 30 nm for all standard cells.

We directly implemented LER on poly printed images made by OPC and lithography simulation where we applied LER just on gate region ($\approx$ poly on active) to save computational resources. We generated more than one thousand LER patterns for a particular rms value of LER so that the results are shown as a distribution similar to a normal distribution. For the 32-nm circuit simulation, we used 32-nm predictive technology model (PTM) [33].

Using these LER impact on the device currents, we optimized the poly layout of standard cells, as shown in Tables II and III. The poly-to-poly space of the nonoptimized cell is 84 nm and the corresponding 3σ LER is 4.80 nm. Meanwhile we found that the best poly-to-poly space for LER minimization is 97 nm where the minimum 3σ LER is 3.95 nm. The gate length variation due to LER follows a distribution which has the upper bound corner and the lower bound corner. The variation due to LER is defined for three different conditions: 1) a nominal condition; 2) $+3\sigma$; and 3) -3σ variations. The $\pm 3\sigma$ variations result in the lower ($\sim$thinner line) and upper ($\sim$thicker line) bounds. The ***best*** condition occurs when the gate length due to LER has the minimum value which makes the I_{on} of a cell increased, meanwhile the ***worst*** condition represents the maximal gate length and the minimal saturation current for I_{on}. Whereas, when the gate length due to LER has the minimum value and the gate leakage is maximized, the ***worst*** corner for leakage current I_{off} is happened. In a point of optimization, we should maximize the worst case I_{on} and minimize the worst case I_{off} current. The area increment is correlated with the number of input gates. Meanwhile, the maximum area penalty is as much as 11.4% regardless of the number of input gates in a cell.

Table II compares I_{on} currents between before and after optimized cases. It shows that the cell currents at the nominal and the best cases are slightly decreased on average 0.75%, 3.84% after optimization, respectively. This is because the gate printed image before optimization has larger LER value, such that the more current is induced through the smaller gate length regions due to LER. Meanwhile, the saturation current at the worst case after optimization is somewhat increased on average 4.46%. It can be shown that the MUX2 has relatively large current variation compared to other cells. That is because the poly layout of MUX2 is more irregular than other cells, hence LER of MUX2 is relatively larger than others. We entirely reduced the saturation current variation between $+3\sigma$ and -3σ corners. However the LER-aware layout optimization does not highly improve the saturation current in our experiments. Even though it has low

TABLE III
IMPROVEMENT OF $I_{\rm off}$ LEAKAGE CURRENT

Cell	Before Optimization (α)			After Optimization (β)			Improve (β:α)(%)[c]			Area
	Best (A)	Norm (A)	Worst (A)	Best (A)	Norm (A)	Worst (A)	Best[a]	Norm[b]	Worst[b]	%
INV	2.76E-08	4.18E-07	8.10E-05	3.59E-08	2.21E-07	4.45E-06	-30.15	47.21	94.50	7.60
NAND2	1.55E-08	1.38E-07	2.10E-05	1.93E-08	8.33E-08	9.40E-07	-24.32	39.70	95.51	8.55
NAND3	1.42E-08	1.13E-07	1.19E-05	1.75E-08	7.03E-08	6.61E-07	-23.29	37.74	94.44	9.12
NOR2	5.51E-08	8.35E-07	1.62E-04	7.18E-08	4.41E-07	8.91E-06	-30.19	47.20	94.51	8.55
NOR3	8.27E-08	1.25E-06	2.43E-04	1.08E-07	6.62E-07	1.34E-05	-30.16	47.21	94.50	9.12
MUX2	7.76E-07	3.19E-06	1.91E-04	8.05E-07	2.47E-06	4.95E-05	-3.74	22.48	74.12	10.20
average							-23.64	40.26	91.26	8.86

[a]Negative value corresponds to the increased leakage current. The larger leakage current denotes the better variation at the best process corner.
[b]Positive value represents the decreased leakage current. The smaller leakage current means the better variation at the worst process corner.
[c]The overall improvement of the leakage current from LER-aware layout optimization is so huge in the entire cases.

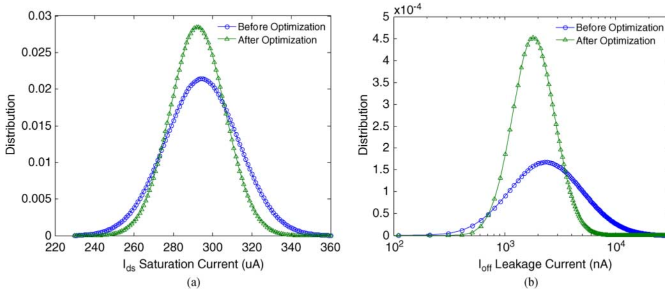

Fig. 13. Improvement $I_{\rm on}$ and $I_{\rm off}$ variation. (a) $I_{\rm on}$ distribution. (b) $I_{\rm off}$ distribution.

impact, the results show that the optimized layout is more robust to LER variation.

In Table III, we presented leakage current between before and after optimization. After optimizing cell layouts, the nominal leakage is decreased by up to 47% and on average 40%. It implies that small reduction of $L_{\rm eff}$ causes a huge amount of leakage decrease. The result of leakage current at the worst case is more interesting. The leakage current shoots up from the small reduction of $L_{\rm eff}$. As shown in the results, the worst case leakage after optimization is dramatically reduced by 91.26%. This is because the leakage is exponentially increased due to LER in the worst case as shown in Fig. 3(b).

The experimental results in Table II and III depict that our LER-aware layout optimization make cell layouts robust from LER process variation. Fig. 13 shows the improvement of current variations after poly layout optimization with a normal distribution for $I_{\rm on}$ and with a log-normal distribution for $I_{\rm off}$. The results explain that the variation of the saturation current is somewhat reduced, meanwhile the leakage current is marvelously decreased after layout optimization.

VI. CONCLUSION

We have proposed a layout-aware LER model which considers various LER value due to layout proximity. Based on the proposed LER model, we have optimized poly layer in standard cell library to maximize the worst case saturation current as well as to minimize leakage current. Our approach practically and effectively improves the circuit performance and hence yield. Experimental results with 32-nm node standard cells show that our layout optimization with the new LER model can substantially improve the device performance, in particular leakage current. As a future work, we can extend the framework into metal layer optimization for improving metal delay and reliability.

REFERENCES

[1] M. Cho, K. Yuan, Y. Ban, and D. Z. Pan, "ELIAD: Efficient lithography aware detailed router with compact post-opc printability prediction," in *Proc. Design Automat. Conf.*, Jun. 2008, pp. 504–509.
[2] W. Poppe, L. Capodieci, J. Wu, and A. Neureuther, "From poly line to transistor: Building BSIM models for nonrectangular transistors," in *Proc. SPIE*, 2006, p. 61560P.
[3] S. Shi, P. Yu, and D. Z. Pan, "A unified non-rectangular device and circuit simulation model for timing and power," in *Proc. Int. Conf. Comput. Aided Design*, Nov. 2006, pp. 423–428.
[4] Y. Ban and D. Z. Pan, "Compact modeling and robust layout optimization for contacts in deep subwavelength lithography," in *Proc. Design Automat. Conf.*, Jun. 2010, pp. 408–411.
[5] M. Chiang, J. Lin, K. Kim, and C. Chuang, "Random dopant fluctuation in limited-width FinFET technologies," *IEEE Trans. Electron Devices*, vol. 54, no. 8, pp. 2055–2060, Aug. 2007.
[6] V. Wang and D. Markovic, "Linear analysis of random process variability," in *Proc. Int. Conf. Comput. Aided Design*, Nov. 2008, pp. 292–297.
[7] A. Asenov, S. Kaya, and A. Brown, "Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1254–1260, May 2003.
[8] E. Wu, E. Nowak, R. Vollertsen, and L. Han, "Weibull breakdown characteristics and oxide thickness uniformity," *IEEE Trans. Electron Devices*, vol. 47, no. 12, pp. 2301–2309, Dec. 2000.
[9] M. Chandhok, S. Datta, D. Lionberger, and S. Vesecky, "Impact of line width roughness on Intel's 65 nm process devices," in *Proc. SPIE*, 2007, p. 65191A.
[10] K. Patel, T. Liu, and C. Spanos, "Impact of gate line edge roughness on double-gate FinFET performance variability," in *Proc. SPIE*, 2008, p. 69251.
[11] C. Mack, "Stochastic modeling in lithography: Autocorrelation behavior of catalytic reaction.diffusion systems," *SPIE J. Microlithogr., Microfabricat. Microsyst.*, vol. 8, p. 029701, 2009.
[12] V. Constantoudis, G. P. Patsis, L. H. A. Leunissen, and E. Gogolides, "Line edge roughness and critical dimension variation: Fractal characterization and comparison using model functions," *J. Vac. Sci. Technol.*, vol. 22, no. 4, pp. 1974–1981, 2004.
[13] Y. Ma, H. Levinson, and T. Wallow, "Line edge roughness impact on critical dimension variation," in *Proc. SPIE*, 2007, p. 651824.
[14] T. Schnattinger and A. Erdmann, "A comprehensive resist model for the prediction of line-edge roughness material and process dependencies in optical lithography," in *Proc. SPIE*, 2008, p. 69230R.
[15] Y. Ban, S. Sundareswaran, R. Panda, and D. Pan, "Electrical impact of line-edge roughness on sub-45 nm node standard cell," in *Proc. SPIE*, 2009, p. 727518.
[16] Y. Ye, F. Liu, S. Nassif, and Y. Cao, "Statistical modeling and simulation of threshold variation under dopant fluctuations and line-edge roughness," in *Proc. Design Automat. Conf.*, Jul. 2008, pp. 900–905.
[17] D. Pawlowski, L. Deng, and M. Wong, "Fast and accurate OPC for standard-cell layouts," in *Proc. Asia South Pacific Design Automat. Conf.*, Jan. 2007, pp. 7–12.

[18] H. Namatsu, M. Nagase, T. Yamaguchi, K. Yamazaki, and K. Kurihara, "In uence of edge roughness in resist patterns on etched patterns," *J. Vac. Sci. Technol.*, vol. 16, no. 6, pp. 3315–3321, 1998.
[19] V. Constantoudis, G. Kokkoris, P. Xydi, E. Gogolides, E. Pargon, and M. Martin, "Line-edge-roughness transfer during plasma etching: Modeling approaches and comparison with experimental results," *SPIE J. Microlithogr., Microfabricat. Microsyst.*, vol. 8, no. 043004, 2009.
[20] K. Patel, T. Wallow, H. Levinsoc, and C. Spanos, "Comparative study of Line Width Roughness (LWR) in Next-Generation Lithography (NGL) processes," in *Proc. SPIE*, 2010, p. 76400T.
[21] Y. Ban, Y. Ma, H. Levinson, Y. Deng, J. Kye, and D. Z. Pan, "Modeling and characterization of contact edge roughness for minimizing design and manufacturing variations in 32-nm node standard cell," in *Proc. SPIE*, 2010, p. 76410D.
[22] C. Mack, *Fundamental Principles of Optical Lithography*. New York: Wiley, 2007.
[23] A. Pawloski, A. Acheta, S. Bell, B. Fontaine, T. Wallow, and H. Levinson, "The transfer of photoresist LER through etch," in *Proc. SPIE*, 2006, p. 615318.
[24] *"Calibre Workbench User's and Reference Manual"* ver. 2008.2 [Online]. Available: http://www.mentor.com/
[25] *"HSPICE User Guide: Simulation and Analysis"* ver. B-2008.09 [Online]. Available: http://www.synopsys.com/
[26] V. Kheterpal, T. Hersan, V. Rovner, D. Motiani, Y. Takagawa, L. Pileggi, and A. Strojwas, "Design methodology for IC manufacturability based on regular logic-bricks," in *Proc. Design Automat. Conf.*, Jun. 2005, pp. 353–358.
[27] T. Jhaveri, I. Stobert, L. Liebmann, P. Karakatsanis, V. Rovner, A. Strojwas, and L. Pileggi, "OPC simplification and mask cost reduction using regular design fabrics," in *Proc. SPIE*, 2009, p. 727417.
[28] Y. Ban, S. Sundareswaran, and D. Pan, "Total sensitivity based DFM optimization of standard library cells," in *Proc. Int. Symp. Phys. Design*, Mar. 2010, pp. 113–120.
[29] A. Chakraborty and D. Pan, "On stress aware active area sizing, gate sizing, and repeater insertion," in *Proc. Int. Symp. Physical Design*, Mar. 2009, pp. 35–41.
[30] V. Joshi, B. Cline, D. Sylvester, D. Blaauw, and K. Agarwal, "Stress aware layout optimization," in *Proc. Int. Symp. Physical Design*, 2008, pp. 168–174.
[31] Nangate 45 nm Open Cell Library [Online]. Available: http://www.nangate.com/index.php
[32] A. Kahng, S. Muddu, and C. Park, "Auxiliary pattern-based OPC for better printability, timing and leakage control," *SPIE J. Microlithogr., Microfabricat. Microsyst.*, vol. 7, no. 1, p. 013002, 2008.
[33] Predictive Technology Model ver. 1.2 [Online]. Available: http://ptm.asu.edu/

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